



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁷ : B24B 37/04, B24D 3/32, 13/14	A1	(11) International Publication Number: WO 00/02708 (43) International Publication Date: 20 January 2000 (20.01.00)
(21) International Application Number: PCT/US99/15629 (22) International Filing Date: 8 July 1999 (08.07.99) (30) Priority Data: 09/114,003 10 July 1998 (10.07.98) US (71) Applicant: CABOT CORPORATION [US/US]; 75 State Street, Boston, MA 02109-1806 (US). (72) Inventors: ANJUR, Sriram, P.; 4027 Tansy Road, Aurora, IL 60504 (US). SEVILLA, Roland, K.; 3733 Edgebrook Court, Aurora, IL 60504 (US). KAUFMAN, Frank, B.; 721 Easton Avenue, Geneva, IL 60134 (US). (74) Agent: LANDO, Michelle, B.; Cabot Corporation, 157 Concord Road, Billerica, MA 01821-7001 (US).	(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published With international search report.	

(54) Title: POLISHING PADS FOR A SEMICONDUCTOR SUBSTRATE



(57) Abstract

A polishing pad for polishing a semiconductor wafer which includes an open-celled, porous substrate having sintered particles of synthetic resin. The porous substrate is a uniform, continuous and tortuous interconnected network of capillary passage. The pores of the porous substrate have an average pore diameter of from about 5 to about 100 microns which enhances pad polishing performance.