

capacitors CS2 and CS3 are decoupled from non-switched S-capacitor CS1 and establish a minimum S-capacitance value.

A control circuit 61 includes a microprocessor 208 that is responsive to a data signal 209a generated in a frequency-to-data signal converter 209. Signal 209a has a numerical value that is indicative of the frequency of a synchronizing signal HORZ-SYNC or deflection current i_y . Converter 209 includes, for example, a counter that counts the number of clock pulses, during a given period of signal HORZ-SYNC and generates word signal 209a in accordance with the number of clock pulses that occur in the given period. Microprocessor 208 generates a control data signal 208a that is coupled to an input of D/A converter 201. The value of signal 208a is determined in accordance with the horizontal rate of signal HORZ-SYNC. D/A converter 201 generates, in accordance with data signal 208a, analog control signal 60a at a single terminal 61a. Signal 60a is at a level that is determined by signal 208a, in accordance with the frequency of signal HORZ-SYNC. Alternatively, the value of signal 208a may be determined by a signal 209b that is provided by a keyboard, not shown.

A non-switched, clamp circuit 300 includes a capacitor CD1 coupled in series with a parallel arrangement of a rectifying diode DD1 and a damping resistor RD1. Clamp circuit 300 is coupled between terminal 25 of capacitor CS1 and ground or across S-capacitor CS1. Clamp circuit 300 is an in-circuit clamp at each horizontal scan frequency of signal 103a selected from the range of $1f_H$ to $2.4f_H$. Diode DD1 of clamp circuit 300 rectifies peaks of the horizontal rate voltage component at terminal 25 of S-capacitor CS1. The rectification occurs mainly when vertical scanning is at approximately the top third of the display screen. The R-C component values of clamp circuit 300 are selected to provide optimized damping, when the frequency of horizontal deflection current i_y is equal to or greater than $2f_H$.

When the operation frequency is at the lower frequency, $1f_H$, the horizontal deflection supply voltage B+ is reduced to 70V from a higher level in the vicinity of 140V. Therefore, the rectification provided by diode DD1 of clamp circuit 300, renders a lower voltage. The result is that the power

dissipated in resistor RD1 drops to about 25% of that at $2f_H$. Consequently, disadvantageously, at the lower frequency $1f_H$ circuit 300 may not provide sufficient damping to prevent ringing.

Advantageously, a switched, clamp circuit 303 is coupled to terminal 25 and includes a capacitor CD2 coupled in series with a parallel arrangement of a rectifying diode DD2 and a damping resistor RD2. A terminal CD2a of capacitor CD2 that is remote from terminal 25 is coupled to supply voltage B+ via a relay contact RB and a relay contact RA of a relay 302. Coil LR of relay 302 is coupled between a supply voltage of 15V and the collector terminal of a relay control transistor Q4. The base terminal of transistor Q4 is coupled to terminal 61a.

When the horizontal frequency is equal or greater than $2f_H$, signal 60a at terminal 61a is at the higher level causing coil LR of relay 302 to be energized via transistor Q4. This results in decoupling contact RA from contact RB. On the other hand, when the horizontal frequency is equal to $1f_H$, signal 60a is at the lower level and causes transistor Q4 to turn off in a manner to couple capacitor CD2 to the terminal where voltage B+ is developed. Thus, clamp circuit 303 and trace capacitor CS2 are in-circuit elements when the selected horizontal scan frequency is $1f_H$.

The component values of clamp circuit 303 are selected to supplement the damping provided by circuit 300 for providing the desired damping, when the frequency of horizontal deflection current i_y is equal to $1f_H$. Advantageously, both clamp circuits 300 and circuit 303 provide together the required clamping for eliminating ringing, when the frequency of horizontal deflection current i_y is equal to $1f_H$. Similarly to capacitor CS2, clamp circuit 303 has no effect at higher frequencies than $1f_H$.

Had capacitor CD2 of clamp circuit 302 been coupled to ground as capacitor CD1, it would have differentiated the E-W pincushion correction parabolic voltage component developed at terminal 25 of the in-circuit S-shaping capacitors. This is so because supply voltage B+ that determines the voltage at terminal 25 varies at a vertical rate parabolic manner. Such differentiation could have resulted in an undesirable sawtooth current

component that varies at vertical rate in current i_y of horizontal winding L_y . Disadvantageously, the undesirable sawtooth current component could have caused the sides of the raster to tilt.

Advantageously, in contrast to clamp capacitor CD1, terminal CD2a of clamp capacitor CD2 that is remote from terminal 25 is DC coupled to supply voltage B+ via relay contacts RB and RA, instead of to ground. Each terminal of capacitor CD2 develops the same amplitude and phase of the vertical rate parabola component of voltage B+. Consequently, the voltage difference developed between the terminals of clamp capacitor CD2 excludes any vertical rate parabola voltage difference. Thus, the rectified peaks of the voltage in S-capacitor CS2, for example, and the supply voltage B+ modulation are approximately equal in magnitude. Therefore, vertical rate variations in supply voltage B+, advantageously, have no effect on the damping function.

The extent of damping required is greater when the frequency of horizontal deflection current i_y is equal to $1 f_H$, than when the frequency of horizontal deflection current i_y is higher. Therefore, coupling capacitor CD1 to voltage B+ is not as important as in the case of capacitor CD2.



What is claimed is:

1. A video display deflection apparatus operating at multi-scan horizontal frequencies, comprising:

a source of an input signal (107a) at a frequency related to a selected horizontal deflection frequency (horizontal);

a first switch (104), responsive to said input signal (107a) and coupled to a horizontal deflection winding (LY) and to a retrace capacitance (105), for generating a horizontal deflection current in said horizontal deflection winding at the selected horizontal deflection frequency, said horizontal deflection winding being coupled to an S-shaping capacitance (CS1, CS2, CS3) for generating an S-shaping voltage (voltage at terminal 25) that provides horizontal linearity distortion correction; characterized in that

a first clamp circuit selectable (DD2, CD2) in accordance with the selected horizontal deflection frequency for clamping said S-shaping voltage, during a portion of a horizontal period; and

a second switch (302) responsive to said input signal and coupled to said first clamp circuit for selecting said first clamp circuit, when the selected horizontal deflection frequency is within a first range ($\leq f_H$), and for de-selecting said first clamp circuit, when the selected horizontal deflection frequency is within a second range ($> f_H$).

2. A video display deflection apparatus according to Claim 1, characterized in that said S-shaping capacitance (CS1, CS2, CS3) comprises, a plurality of S-shaping capacitors (CS1, CS2, CS3) for selecting one of said S-shaping capacitors (CS2), when the selected horizontal deflection frequency is within one (f_H) of said first and second ranges, and for de-selecting said one S-shaping capacitor, when the selected horizontal deflection frequency is within the other one ($> 2f_H$) of said first and second ranges.



3. A video display deflection apparatus, further characterized by, a second clamp circuit (DD1, CD1) for clamping said S-shaping voltage (at terminal 25) during a portion of said horizontal period.

4. A video display deflection apparatus according to Claim 3, wherein said second clamp circuit (DD1, CD1) clamps both, when the selected horizontal deflection frequency is within the first range ($\leq f_{H1}$), and when the selected horizontal deflection frequency is within the second range ($> f_{H1}$).