ABSTRACT

The present technology relates to a memory device and a method of operating the memory device. The memory device includes a memory block including a plurality of memory cells corresponding to a plurality of word line groups, a source line driver configured to apply an erase voltage to a source line of the memory block during an erase operation, a voltage generation circuit configured to apply an operation voltage increasing from a first operation voltage to a second operation voltage to the plurality of word line groups during the erase operation, and a control logic configured to control the source line driver and the voltage generation circuit to perform a suspend operation of stopping the erase operation.

FIG. 5