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PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO ELECTRONIC TIMEPIECES

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese company, of 31-1, 6-chome, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to electronic timepieces and has, for its main object, to provide improved digital time displaying electronic timepieces which have displays which are such that the user can easily and readily correct the time while reading, without doubt or ambiguity, the part of the display which is being corrected.

In a conventional digital electronic timepiece in which at least part of the display is utilisable to display different items of information, for example in a digital electronic timepiece having (among other things) a seconds/date display, it being possible to change the second display into a date display and vice-versa—there is the practical disadvantage that, when the date continues to be displayed, a change in the seconds display cannot be seen directly. Since any display up to 31 in the seconds/date display could be either seconds or a date there may be confusion in the mind of the operator causing him difficulty if he wants to correct the seconds display. In a timepiece in which the operation of counting up to 30 or 31 seconds (and disregarding the rest of the count up to 59) is used to provide a whole number for indicating the date, confusion and difficulty is particularly prone to occur.

As will be seen later the invention provides improved digital electronic timepieces in which the above disadvantage is avoided.

An object of the invention is to provide improved digital electronic timpieces in which if seconds correction is required to be made at a time when the date is being indicated, the initiation of seconds correction causes the seconds/date display to be automatically changed over from a display of date to a display of seconds.

According to this invention there is provided in an electronic timepiece having at least an hours digital display portion, a minutes digital display portion, and a date/seconds digital display portion, arranged to display either seconds or date at will, and means for correcting displayed time, means actuated automatically when time correction is effected for causing the last mentioned display portion to display seconds.

Preferably the timepiece has 12-hour time counting means, and 24-hour time counting means.

The timepiece may be provided with means, responsive to a fall in the voltage of the driving battery of the timepiece below a predetermined minimum value, for indicating the occurrence of such fall on at least one of the aforesaid displays at least a predetermined intervals of time. The said indication may be given by flashing a display and there may be provided manually operable switch means for bringing said voltage fall responsive means into operation at will at any time.

The timepiece may include inspection or checking means and said means may comprise an inspecting terminal connected to a time standard circuit of the timepiece.

An embodiment of the invention is illustrated in the accompanying drawings in which:

Figure 1 is a simplified diagram of the embodiment; and

Figure 2 is a face view of a wristwatch embodying the invention and shows a convenient lay out for the displays—hours, minutes, day of the week, and date/seconds—provided.

Referring to Figure 1, reference 1 is a manually operable switch which determines whether the display includes a digital display of the date or a digital display of seconds. One terminal of this switch is con-

nected to the relatively high voltage level terminal (indicated as earth) of the supply battery (not shown) and the other is connected to an anti-chatter circuit 5 (for eliminating effects of switch chatter) the output terminal Q of which is connected to the trigger input terminal T of a set, reset and triggering flip-flop (RS.T.FF) 35. The output lead S/D CONT of this RS.T.FF is connected to the control terminal CONT of an electronic switch group 81.

2 is a manually operable safety and reset switch. This is a two-position switch constructed mechanically to hold the state into which it was last moved. This switch 2 has one terminal connected to the relatively high voltage level point and the other connected to an anti-chatter circuit 6, the output terminal Q of which is connected through an inverter 86 to one input of a NAND gate 10, and to one input of each of two NOR gates 12 and 13. The said output terminal Q is also connected directly to one input of a NAND gate 33 and to the input of a wave shaping circuit 14 designed to secure constancy of the output pulse width from the anti-chatter circuit 6 and to produce an output signal timed in accordance with the opening of the switch 2. The output terminal of the wave shaping circuit 14 is connected to the reset terminal R of a function shift register 18 and to the DATA input terminal of an electronic switching circuit 17.

3 is a manually operable digit selecting switch for use in the correction of displayed time, this switch being employed to select the digits to be corrected, e.g. month digits, day of the week digits, hour digits, minutes digits and so on. One terminal of this digit selecting switch 3 is connected to the relatively high voltage level point and the other is connected to the input terminal of an anti-chatter circuit 7 the $\overline{Q}$ output terminal of which is connected to one input of a NAND gate 9, one input of an OR gate 11 and the remaining input of the NOR gate 12.

4 is a manually operable fast feed input switch for time correction and the operation of which advances the digit selected for time correction by the digit selecting switch 3. One terminal of this switch 4 is connected to the relatively high voltage level point and the other is connected to the input of an anti-chatter circuit 8 and $\overline{Q}$ output terminal of which is connected to remaining inputs of the NAND gate 9, the OR gate 11 and the NOR gate 13.

The output terminal of the NAND gate 9 is connected to the remaining input of the NAND gate 10.

The output of the NOR gate 12 is applied to the input of a wave shaping circuit 15, which is also designed to achieve constancy of pulse width, and the output of which is applied to the clock input terminal C of the function shift register 18. This is a 5-bit shift register having five output terminals N, D/M, D/W, H and M which are, respectively, Normal; Day/Month; Day/Week; Hour; and Minute output terminals. As will be more fully appreciated, one of these five output terminals is selected to assume HIGH logic level "H".

The electronic timepiece is in its normal time counting state when the output terminal N is at the HIGH logic level "H". This output terminal N is connected to the input terminal CONT of the electronic switch 17, to the remaining input of the NAND gate 33 and to one each of the input terminals of four OR gates 29, 30, 31 and 32.

When the output terminal D/M is at the HIGH logic level "H" correction of the day digit can be effected and the day digit is indicated. this output terminal D/M is connected to one each of the inputs of two NAND gates 27, 28, to the reset terminal R of the T type flip-flop (T.FF) 35 and to one input of a three-input OR gate 32.

Correction of the day of the week display can be effected when the output of the output terminal D/W is at the HIGH logic level "H" and the day of the week digit is indicated. This output terminal D/W is connected to one each of the input terminals of NAND gates 25, 26 and to the remaining input terminal of the OR gate 31.

Correction of the hour digit can be effected when the output of the output terminal H is at the HIGH logic level "H" and the hour digit is indicated. This output terminal H is connected to one each of the input terminals of NAND gates 23, 24 and to the remaining input of the OR gate 30.

Correction of the minute digit can be effected when the output of the output terminal M is at the HIGH logic level "H" and the minutes and seconds are indicated. This output terminal M is connected to one each of the inputs of the NAND gates 21, 22, to the remaining input of the OR gate 29, to a second input of the OR gate 32 and, through an inverter 87, to the remaining input of a NAND gate 34.

The final output or set terminal S of the function register 18 is connected to a terminal 19 at which appears a signal when the outputs at the terminals N, D/M, D/W, H and M are all at the HIGH logic level "H".

The output of the NAND gate 33 is applied to the other input terminal of the NAND gate 34, the output of which is connected to the set terminal S of the T.FF 35.

The output terminal of NAND gate 10 is connected to the clock input terminal T of a T.FF 20, the output terminal Q of which is connected to the reaming input terminals of the NAND gates 22, 24, 26, 28 and to the control terminals CONT of a group of electronic switches 55, 64, 72 and 80. The $\overline{Q}$ output of the T.FF 20 is connected to the remaining input terminals of the NAND gates 21, 23, 25, 27.

The output terminal of the NOR gate 13 is connected to the input terminal of a wave shaping circuit 16, the output terminal of which is connected to the inputs of electronic switches 51, 52, 59, 60, 68, 69, 76 and 77.

The output terminal of the NAND gate 21 is connected to the control terminal CONT of the electronic switch 51; the output terminal of the NAND gate 22 is connected to the control terminal CONT of the electronic switch 52; the output terminal of the NAND gate 23 is connected to the control terminal CONT of the electronic switch 59; the output terminal of the NAND gate 24 is connected to the control terminal CONT of the electronic switch 60; further the output terminal of the NAND gate 25 is connected to the control terminal CONT of the electronic switch 68; the output terminal of the NAND gate 27 is connected to the control terminal CONT of the electronic switch 76; and the output terminal of the NAND gate 28 is connected to the control terminal CONT of the electronic switch 77.

An oscillator circuit diagrammatically represented as including an amplifying inverter 43 and a crystal vibrator 44, constitutes the time standard oscillation generator of the electronic timepiece and the oscillations therefrom are applied to a frequency divider 45 the output from which is applied through a level shifting circuit 46 to one input of an OR gate 47 the other input of which is connected to a terminal 48 and the output from which is applied to a further frequency divider 49 producing a signal of (in the present example) 1Hz.

This 1Hz signal from divider 49 is applied to the clock input terminal C of a seconds counter 50. The binary signal output of the seconds counter 50 is applied to the input terminals IN_1 of an electronic switch group 81.

The Q output of the seconds counter 50 is applied directly to one input of an OR gate 38, and to one input of a NAND gate 42 and also, through an inverter 39, to one input of an OR gate 37a.

The one-minute signal output of the counter 50 is applied to the respective input terminals I_1, I_2 of the electronic switches 51 and 52.

The output terminal of the electronic switch 17 is connected to the reset terminal R of the seconds counter 50.

The timepiece has a minutes counter, an hours counter, a day of the week counter and a date counter and, as will be seen later, the binary counter outputs are selected by electronic selective switch means for utilisation for driving the display device *via* decoder and driver circuits.

There is a 12-hours displayed time circuit which consists of counting circuits 53, 61, 62, 70 and 78. There is also a 24-hours displayed time circuit which consists of the counting circuits 54, 63, 71 and 79.

The display is arranged to indicate always either the contents of the 12-hours displayed time circuit or the contents of the 24-hours displayed time circuit.

The output of the electronic switch 51 is applied to a minutes counting circuit 53 the Q output of which, namely a one-hour signal, is applied at input terminal I_2 to an electronic switch 59. The binary outputs of the said counting circuit 53 are applied to the input terminals IN_1 of an electronic switch 55.

The Q output of the electronic switch 59 is applied to the input terminal C of an hour-counting circuit 61 and the binary outputs of the said hour-counting circuit 61 are applied to the input terminal IN_1 of an electronic switch 64.

The output of the hour-counting circuit 61 at its terminal CA is a 12-hour signal and this is applied to the AM/PM counting circuit 62, the output of which, at its terminal CA, is applied to the input terminals I_2 of electronic switches 68 and 76 and also to one input of the OR gate 41. The Q output of the electronic switch 68 is applied to the input terminal C of a day of the week-counting circuit 70 and the Q output of the electronic switch 76 is applied to the input terminal C of a date-counting circuit 78.

The binary outputs of the day of the week-counting circuit 70 and the date counting circuit 78 are applied to the input terminals IN_1 of electronic switches 72 and 80 respectively.

The arrangement above described is a 12-hour time counting arrangement.

The Q output terminal of the electronic switch 52 is connected to the input terminal C of a minutes counting circuit 54, the binary output of which is applied to the input terminals IN_2 of the electronic switch 55. The Q output of said minute-counting circuit 54 appearing at its terminal CA is a one-hour signal and this is applied to the input terminal I_2 of the electronic switch 60. The Q output of this switch 60 is applied to the input terminal C of an hour-counting circuit 63, the binary output of which is a date signal which is applied to the input

terminals I_2 of the electronic switch 64. The output at the terminal CA of the counting circuit 63 is applied to the terminals I_2 of the electronic switches 69 and 77. The Q output of the electronic switch 69 is applied to the input terminal C of the day of the week-counting circuit 71, the binary output of which is applied to the input terminals IN_2 of electronic switch 72.

The output of the electronic switch 77 is applied to the input terminal C of the day of the week-counting circuit 79 the binary content of which is applied to the input terminal IN_2 of electronic switch 80. Output from this electronic switch 80 is applied to an electronic switch 81 the purpose of which is to alternate the date-information for the day-information.

The outputs of the electronic switches 55, 64, 72 and 81 are fed respectively to decoder-driver circuits 56, 65, 73 and 82, which drive the display elements of, respectively, a minutes display 57, an hours display 66, a day of the week display 74 and a date and seconds display 83 in the display device of the timepiece.

The control terminals of the decoder-driver circuits 56, 65, 73 and 82 are indicated by the reference CONT. Each of these drivers is arranged to produce its appropriate display when its control terminal is at the HIGH logic level "H".

The control terminals CONT of the decoder-drivers 56, 65, 73 and 82 are fed respectively from the outputs of AND gates 58, 67, 75 and 84 each of which has one input connected to the output of the NAND gate 42.

The remaining input of AND gate 58 is connected to the output of the OR gate 29; the remaining input of the AND gate 67 is connected to the output of the OR gate 30; the remaining input of the AND gate 75 is connected to the output of the OR gate 31; and the remaining input of AND gate 84 is connected to the output of the OR gate 32.

The output of the OR gate 11 is connected to the remaining input of the OR gate 41, the output terminal of which is connected through wave shaping circuit 40 to the remaining inputs of the OR gate 37a and 38. The output terminal of the OR gate 37a is connected to the control terminal CONT of a battery voltage detecting circuit 36 the purpose of which is to respond when the power supply battery (not shown) is near the end of its useful life. The output terminal Q of the battery voltage detecting circuit 36 is connected to the set input terminal S of an R—S flip-flop 37. The output of the OR gate 38 is connected to the reset input terminal R of said R—S flip-flop 37, the output terminal Q of which is connected to the remaining input of the NAND gate 42. The set terminals S of the counting circuits 50, 53, 54, 61, 62, 63, 70, 71, 78 and 79 are connected to the terminal 85.

The operation of the timepiece will now be described.

In the normal state, with the switches 1, 2, 3 and 4 OFF, what is displayed is determined by the output logic states of the trigger flip-flop 20 and the R—S flip-flop 35.

Assuming that the Q output terminal of the trigger flip-flop 20 is at the logic state "H", the respective binary outputs of the counting circuits 53, 61, 70 and 78 are applied *via* the terminals IN_1 of the respective electronic switches 55, 64, 72 and 80 to the respective decoder-driver circuits 56, 65, 73 and 82, and accordingly, there is a 12-hour time display with minutes given by the display 57, hours by the display 66 and day by the display 74. Also assuming that the Q output terminal of the R—S trigger flip-flop 35 is at the logic state level "H", the display 83 will indicate seconds since the output of the seconds counter 50, applied to the input terminals IN_1 of the electronic switch 81 will be passed *via* 81 and 82 to the display 83. If, however, the Q output terminal of the R—S flip-flop 35 is at the logic state level "L" (the LOW level) the display 83 will indicate the date as given by the content of the date-counting circuit 78 and passed by switch 80, and terminals IN_2 of the switch 81 to the decoder-driver 84.

Assuming, however, that the Q output terminal of the flip-flop 20 is at the LOW logic level state "L", a 24-hour display is given.

The above change over from date display to seconds display or vice versa is made by operating the switch 1 to change it from On to OFF or vice versa and thus correspondingly to change the Q output level state of the flip-flop 35. In this way either a display of minutes, hours, day and seconds or minutes, hours, day and date will be given, depending on the state of the switch 1.

If, however, either the switch 3 or the switch 4 is put ON, the output level state of the NAND gate 9 becomes "H" because one of its inputs is made "L". If, at this time, the switch 2 is OFF, the output of the NAND gate 10 becomes "L" because the Q output terminal of the anti-chatter circuit 6 is "L". This, of course, changes the output level state of the trigger flip-flop 20. A 12-hour display or a 24-hour display can be selected when the switch 2 is OFF and the switch 3 or the switch 4 is ON. When the flip-flop 20 is at "H" level, the terminals IN_1 of the respective electronic switches 55, 64, 72 and 80 are selected. Accordingly the display 57 for minutes and the display 66 for

hours are connected respectively to the counters 53 and 61, the former being a 60-counter and the latter being a 12-hour counter. The displays 57 and 66 provide a 12-hour (AM/PM) display. When the Q output of the flip-flop 20 is at "L" level, the 60-counter for minutes and the 24-hour counter 63 are connected through the IN_2 terminals of the electronic switches 55 and 64 to display 57 and display 66 respectively. Thus the logic state of the Q output terminal of flip-flop 20 determines the selection of the 12 hour or the 24 hour manner of display. The output levels of the NOR gates 12 and 13 will be "L" when the Q output terminal of the anti-chatter circuit 6 is "L" and operation of the switches 3 and 4 does not affect this. Moreover, as regards the functional shift register 18, the output at its output terminal N will be of logic level "H" and the outputs at its other output terminals will be "L". Therefore, the output states of the NAND gates 21, 22, 23, 24, 25, 26, 27 and 28 will be "H" and the levels at the control terminals CONT of the electronic switches 51, 52, 59, 60, 68, 69, 76 and 77 will all be "H". These switches will therefore pass the signals applied to their I_2 input terminals.

The counting circuits 53, 54, 61, 62, 63, 70, 71, 78 and 79 count the signals applied thereto and function as normal time counting circuits.

The outputs of the OR gates 29, 30, 31 and 32 are at logic level "H" and therefore this level exists at one input of each of the AND gates 58, 67, 75 and 84.

Assuming that the battery voltage detecting circuit 37 is not set as a result of the battery voltage having fallen too low, the output level at its Q output terminal will be "L" and the output level of the NAND gate 42 will be "H". Also all the inputs of the AND gates 58, 67, 75 and 84 will be "H" and the control input terminal CONT of the decoder-driver circuits 56, 65, 72 and 82 will be "H". Accordingly the decoder-driver circuits function normally and time is displayed either in the 12 hour-mode or in the 24 hour mode.

If, however, the battery voltage falls too low, the output of the battery voltage detecting circuit 36 causes the flip-flop 37 to be set, the Q output signal thereof becomes "H", and the NAND gate 42 passes the inverted signals from the seconds counter 50 to the control terminals CONT of the decoder-driver circuits 56, 65, 73 and 82 thus causing the display to flash in synchronism with these inverted signals and warning the user of the timepiece that the battery voltage is low and the battery should be changed.

In order to effect time adjustment or correction, the switch 2 is closed. This makes the Q output terminal of the anti-chatter circuit 6 assume logic level "H" and the output of NAND gate 34 becomes "H" since the level at the output terminal N of the function shift register 18 is "H" and its other terminals are all at "L". Accordingly, the R—S trigger flip-flop 35 is set and its Q output terminal becomes of logic level "H" and the seconds and data display 83 displays seconds.

Because the control terminal CONT of the electronic switch 17 is at logic level "H" when the switch 2 is changed from OFF to ON, the pulse from the wave shaping circuit 14 causes the seconds counter 50 to be reset. If the count in the seconds counter was 29 seconds or less the minutes counter 53 does not receive an input signal but if said count is 30 seconds or more the said minutes counter receives the output signal produced from the seconds counter before it was reset. Thus time adjustment within ±30 seconds is readily made.

If, now, with the switch 2 ON and the switch 3 is also changed to ON, a signal is applied to the clock input terminal C of the function shift register 18 through the NOR gate 12 and the output terminal D/M of said functional shift register 18 becomes of logic level "H", the other output terminals becoming "L". The set-reset trigger flip-flop T.FF 20 resets, and the data and seconds display 83 changes from displaying the seconds to displaying the date automatically. Now only the decoder-driver circuit 82 operates normally, the other decoder-driver circuits 56, 65 and 73 being inhibited from provided outputs. This occurs because the output of the OR gate 32 becomes "H" whereas the outputs of the OR gates 29, 30 and 31 are at level "L". Accordingly, only the data is displayed.

Also, the NAND gates 27 and 28 each have one input at logic level "H" and another at logic level "L" in accordance with the logic states at the output terminals Q, $\overline{Q}$ of the flip-flop 20.

Assuming now that the outputs of the NAND gates 27, 28 are at logic level "L", the control terminal CONT of the electronic switch 76 becomes of logic level "L" and therefore the input signal at the input terminals I_1 of the electronic switch 76 appears at its Q output terminal. In this condition operation of the switch 4 ON and OFF will produce signals which are applied to the date-counting circuit 78 through the said electronic switch 76 so that the said date-counting circuit 78 receives the signals of a number corresponding to the number of times the switch 4 is operated.

Next, if the switch 3 is put ON again, the shift register 18 assumes the logic level "H" at its terminal D/W. In this condition advancement of the day count is possible

with no display other than that of the day of the week being present.

In generally similar manner any display can be selected for correction by repeatedly closing switch 4 which gives an advancement of one unit at each closure, only the particular display selected appearing while the operation of correction is taking place.

Again, in generally similar manner, correction can be effected in the 12-hour counting circuits and in the 24-hour counting circuits if the output at the output terminal Q of the trigger flip-flop 20 is maintained at logic level "H".

Referring now to a function which is of use in inspecting or testing the timepiece there is provided a terminal 48 which is used for inspection or checking purposes and at which the relatively high frequency of the quartz crystal oscillation appears.

The output from the quartz crystal oscillator circuit is divided by the dividing circuit 45 and is applied to one input of NOR gate 47 through level shifting circuit 46.

A useful advantage which follows from supplying the high oscillating frequency (e.g. 32768 Hz) of the quartz oscillator circuit to the terminal 48 used for inspection is that the operating speed of inspection is high since this oscillating frequency is not divided down by the dividing circuit 45 before being so supplied.

The terminal 85 is a terminal for setting a predetermined time, i.e. for setting the contents of each of the counting circuits 50. 53, 54, 61, 62, 63, 70, 71, 78 and 79 to a specified time.

If, for example, the set time is 59 seconds, 59 minutes, 23 hours (11 p.m.), the day is Saturday and the date is the 31st, the respective counting circuits are set at the above preset time when the terminal 85 is at the logic level "H", the respective displayed contents of the counting circuits indicating 00 seconds, 00 minutes, 0 hour (12 o'clock), Sunday and date the 1st after 1 second has elapsed. As will be seen it is an easy matter, during inspection and checking, to check the production of outputs of the respective counting circuits.

The terminal 19 is the set terminal for the functional shift register 18 and the terminals N, D/M, D/W, H and M are set at logic level "H" by setting the terminal 19 at the logic level "H".

As will now be appreciated, the output signals at the terminals N, D/M, D/W, H and M of the shift register 18 are applied to the NAND gates 21, 22, 23, 24, 25, 26, 27 and 28 and are controlled by the output from the flip-flop 20. It will also be seen that all the counting circuits whether used in the 12-hour time counting or 24-hour time counting can be rapidly increased as to their count contents for time correction. For such time correction the switch 2 is put ON and the switch 4 is moved ON and OFF alternatively to increase the count contents of the respective counting circuit. Time correction can thus be very quickly and easily effected.

In the particular embodiment illustrated the battery voltage detecting circuit 36 operates automatically once per day, since it receives the output of the AM and PM counting circuit 62. However, when the switches 3, 4 are put ON, the output of the OR gate 11 becomes of logic level "H" and the battery voltage detecting circuit 35 is operated by the output signal from said OR gate 11. Thus checking of the battery voltage can be readily effected at any time. Ordinarily the user of the timepiece will not close both switches 3 and 4 except to check the state of the battery, but he can do so at any time and thus check the battery state even is he has missed seeing an indication of a low voltage (flashing of the display) given automatically.

Because the date is displayed by the date and seconds display (83) when the date is being adjusted, and seconds are displayed automatically thereby when seconds are being adjusted, the user of the timepiece is never in doubt as to what is displayed when he is effecting adjustment and adjustment is thus greatly facilitated.

Figure 2, which is largely self explanatory, shows one convenient arrangement of the displays. In Figure 2, 83 is the date/seconds display, 74 is the day of the week display, 66 is the hours display and 57 is the minutes display.

WHAT WE CLAIM IS:—

1. An electronic timepiece having at least an hours digital display portion, a minutes digital display portion, a date/seconds digital display portion arranged to display either seconds or date at will, and means for correcting the displayed time, wherein means, actuated automatically when time correction is effected, are provided for causing the last mentioned display portion to display seconds.

2. A timepiece as claimed in claim 1 and having 12-hour time counting means, and 24-hour time counting means.

3. A timepiece as claimed in claim 1 or 2 and comprising means, responsive to a fall in the voltage of the driving battery of the timepiece below a predetermined minimum value, for indicating the occurrence of such fall on at least one of the aforesaid displays at least at predetermined intervals of time.

4. A timepiece as claimed in claim 3 wherein the indication is given by flashing a display.

with no display other than that of the day of the week being present.

In generally similar manner any display can be selected for correction by repeatedly closing switch 4 which gives an advancement of one unit at each closure, only the particular display selected appearing while the operation of correction is taking place.

Again, in generally similar manner, correction can be effected in the 12-hour counting circuits and in the 24-hour counting circuits if the output at the output terminal Q of the trigger flip-flop 20 is maintained at logic level "H".

Referring now to a function which is of use in inspecting or testing the timepiece there is provided a terminal 48 which is used for inspection or checking purposes and at which the relatively high frequency of the quartz crystal oscillation appears.

The output from the quartz crystal oscillator circuit is divided by the dividing circuit 45 and is applied to one input of NOR gate 47 through level shifting circuit 46.

A useful advantage which follows from supplying the high oscillating frequency (e.g. 32768 Hz) of the quartz oscillator circuit to the terminal 48 used for inspection is that the operating speed of inspection is high since this oscillating frequency is not divided down by the dividing circuit 45 before being so supplied.

The terminal 85 is a terminal for setting a predetermined time, i.e. for setting the contents of each of the counting circuits 50. 53, 54, 61, 62, 63, 70, 71, 78 and 79 to a specified time.

If, for example, the set time is 59 seconds, 59 minutes, 23 hours (11 p.m.), the day is Saturday and the date is the 31st, the respective counting circuits are set at the above preset time when the terminal 85 is at the logic level "H", the respective displayed contents of the counting circuits indicating 00 seconds, 00 minutes, 0 hour (12 o'clock), Sunday and date the 1st after 1 second has elapsed. As will be seen it is an easy matter, during inspection and checking, to check the production of outputs of the respective counting circuits.

The terminal 19 is the set terminal for the functional shift register 18 and the terminals N, D/M, D/W, H and M are set at logic level "H" by setting the terminal 19 at the logic level "H".

As will now be appreciated, the output signals at the terminals N, D/M, D/W, H and M of the shift register 18 are applied to the NAND gates 21, 22, 23, 24, 25, 26, 27 and 28 and are controlled by the output from the flip-flop 20. It will also be seen that all the counting circuits whether used in the 12-hour time counting or 24-hour time counting can be rapidly increased as to their count contents for time correction. For such time correction the switch 2 is put ON and the switch 4 is moved ON and OFF alternatively to increase the count contents of the respective counting circuit. Time correction can thus be very quickly and easily effected.

In the particular embodiment illustrated the battery voltage detecting circuit 36 operates automatically once per day, since it receives the output of the AM and PM counting circuit 62. However, when the switches 3, 4 are put ON, the output of the OR gate 11 becomes of logic level "H" and the battery voltage detecting circuit 35 is operated by the output signal from said OR gate 11. Thus checking of the battery voltage can be readily effected at any time. Ordinarily the user of the timepiece will not close both switches 3 and 4 except to check the state of the battery, but he can do so at any time and thus check the battery state even is he has missed seeing an indication of a low voltage (flashing of the display) given automatically.

Because the date is displayed by the date and seconds display (83) when the date is being adjusted, and seconds are displayed automatically thereby when seconds are being adjusted, the user of the timepiece is never in doubt as to what is displayed when he is effecting adjustment and adjustment is thus greatly facilitated.

Figure 2, which is largely self explanatory, shows one convenient arrangement of the displays. In Figure 2, 83 is the date/seconds display, 74 is the day of the week display, 66 is the hours display and 57 is the minutes display.

WHAT WE CLAIM IS:—

1. An electronic timepiece having at least an hours digital display portion, a minutes digital display portion, a date/seconds digital display portion arranged to display either seconds or date at will, and means for correcting the displayed time, wherein means, actuated automatically when time correction is effected, are provided for causing the last mentioned display portion to display seconds.

2. A timepiece as claimed in claim 1 and having 12-hour time counting means, and 24-hour time counting means.

3. A timepiece as claimed in claim 1 or 2 and comprising means, responsive to a fall in the voltage of the driving battery of the timepiece below a predetermined minimum value, for indicating the occurrence of such fall on at least one of the aforesaid displays at least at predetermined intervals of time.

4. A timepiece as claimed in claim 3 wherein the indication is given by flashing a display.

5. A timepiece as claimed in claim 3 or 4 and comprising manually operable switch means for bringing said voltage fall responsive means into operation at will at any time.

6. A timepiece as claimed in any of the preceding claims and provided for inspection or checking purposes, an inspection terminal connected to a time standard circuit of the timepiece.

7. Electronic timepieces substantially as herein described with reference to the accompanying drawings.

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