

1 VOLTAGE CONTROLLED OSCILLATOR

The present invention relates to voltage controlled oscillators.

U.S. Patent No. 4,020,500 - Harwood discloses a synchronized oscillator of a general type which has been
5 subject to widespread use as the color reference oscillator in color television receivers. The oscillator employs a non-inverting amplifier, with feedback via a crystal filter linking the output and input of the non-inverting amplifier. A quadrature phase shift network coupled to the filter
10 output supplies phase shifted signals to an additional controlled amplifier. A phase detector, responsive to received color synchronizing bursts of reference oscillations and to signals from the non-inverting amplifier, develops control voltages representative of the magnitude
15 and sense of the difference, if any, from a desired quadrature phase relationship between its inputs. The additional amplifier supplies phase shifted signals to the non-inverting amplifier's load of a polarity and magnitude determined by the control voltages so as to minimize the
20 aforesaid difference.

In an integrated circuit realization of the circuitry shown in the aforesaid U.S. Patent No. 4,020,500 unwanted phase shift may be associated with the load shared by the non-inverting amplifier and the controlled
25 amplifier of phase shifted signals. This is due to the cumulative effect of parasitic capacitances appearing at the respective collector electrodes of the plurality of transistors coupled to the shared load. Without suitable compensation therefor, such phase shift can interfere with
30 attainment of optimum tuning of the oscillator's free-running frequency and can introduce undesired asymmetry to the phase control characteristic employed for synchronization purposes. U.S. Patent No. 4,095,255

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1 discloses a cascode technique for isolating the collector electrodes of the controlled amplifier from the shared load that lessens the aforementioned unwanted phase shift. U.S. Patent No. 4,249,199 discloses a phase shift
5 compensation technique which can satisfactorily eliminate adverse effects of the aforementioned undesired phase shift on the ability to attain proper tuning of the oscillator's free-running frequency.

An embodiment of the present invention is directed to an
10 improvement over the arrangement disclosed in the aforesaid U.S. Patent No. 4,249,199, which ensures attaining symmetry of the phase control characteristic for the controlled oscillator, as well as elimination of the adverse effects on the ability to attain proper tuning of the free-running
15 frequency.

In accordance with an illustrative embodiment of the present invention, the output of the quadrature phase shift network in an oscillator synchronizing system of the general type shown in the aforementioned U.S. Patent
20 No. 4,020,500 is matrixed with signals directly derived from the non-inverting amplifier thereof to form resultant signals of a phase intermediate the phases of the respective matrixed signals. These resultant signals are subject to an amplification which is controlled in a manner determined
25 by the phase comparator's control voltage output. The sense of the difference from the desired quadrature phase relationship between the comparator's input determines whether the amplification is accompanied by phase inversion or not. The magnitude of the difference determines the degree of amplification.
30 The controlled amplifier shares the load resistor of the oscillator's non-inverting amplifier. An additional inverting amplifier is also responsive to the resultant signals produced by the aforesaid matrixing and develops a phase inverted version of the resultant signals of
35 substantially fixed magnitude across the shared load resistor.

The matrixing parameters and the gain of the inverting amplifier are chosen in relation to the undesired phase shift associated with the shared load resistor so

1 that: (1) the combination of (a) the signals developed
across the shared load resistor by the inverting amplifier,
and (b) the signals developed across the shared load
resistor by the non-inverting amplifier, comprises signals
5 which are substantially in phase with the signals appearing
at the input of the non-inverting amplifier; and (2) the
effect of the undesired phase shift associated with the
shared load resistor on the output of the controlled
amplifier developed thereacross is to place the phase
10 thereof substantially in quadrature with the phase of the
aforesaid combination.

Illustratively, the controlled amplifier includes
first and second transistors disposed with interconnected
emitter electrodes connected to a common current source.
15 The base electrode of the first transistor is responsive
to the resultant signals formed by the aforementioned
matrixing, while the base electrode of the second transistor
is maintained at a predetermined bias potential. First and
second amplifying means have signal inputs coupled
20 respectively to the collector electrodes of the first and
second transistors, are provided with interconnected
outputs, and are subject to differential gain control in
accordance with the phase comparator's control voltage
output.

25 The inverting amplifier illustratively comprises
a third transistor having its base-emitter path in shunt
with the base-emitter path of the first transistor, and its
collector electrode coupled to the shared load resistor.
To preserve symmetry of operation of the controlled
30 amplifier in the instance of such a circuit arrangement
for the inverting amplifier (i.e., wherein it shares a
current source with the controlled amplifier), a fourth
transistor is desirably disposed with its base-emitter path
in shunt with the base-emitter path of the second transistor,
35 and with its collector electrode connected to a supply
terminal of fixed potential.

In the accompanying drawing, the sole figure
illustrates, partially schematically and partially block
representation, a portion of a color television receiver

- 1 incorporating a color reference oscillator of a voltage controlled form in accordance with an embodiment of the present invention.

In the color television receiver portion

- 5 illustrated in the drawing, a non-inverting amplifier 10 is provided with sufficient positive feedback via a bandpass filter linking its output and input to enable it to operate as an oscillator at an operating frequency lying within the filter's passband.
- 10 Amplifier 10 includes a pair of NPN transistors 11 and 13, disposed in a differential amplifier configuration with their emitter electrodes interconnected. The collector electrode of the input transistor (11) of the differential amplifier is directly connected to the
- 15 positive terminal $+V_{CC}$ of an operating potential supply, while the collector electrode of the output transistor (13) of the differential amplifier is connected to the $+V_{CC}$ terminal via a load resistor 14. The interconnected emitter electrodes of transistors 11 and 13 are returned to the
- 20 negative terminal (e.g., ground) of the operating potential supply via the collector-emitter path of an NPN current source transistor 15 in series with its emitter resistor 16.

- Signals are applied from the amplifier input terminal I to the base electrode of the input transistor 11
- 25 via the base-emitter path of an NPN emitter-follower transistor 21. Signals are applied from the collector (at terminal S) of output transistor 13 to the amplifier output terminal O via the base-emitter paths of a pair of NPN emitter-follower transistors 31 and 33, which are
- 30 interconnected by a resistor 32 linking emitter electrode of transistor 31 to the base electrode of transistor 33. The emitter electrode of transistor 33 is returned to ground via resistor 34. The collector electrodes of emitter-follower transistors 21, 31, 33 are each directly connected
- 35 to the $+V_{CC}$ supply terminal.

Bias for the base electrode of output transistor 13 is established by an NPN emitter-follower transistor 25, disposed with its collector electrode directly connected to the $+V_{CC}$ supply terminal, with its base electrode connected

1 via a resistor 26 to the positive terminal (+5.2V.) of a
bias supply, and with its emitter electrode directly
connected to the base electrode of output transistor 13.
The quiescent current drawn by emitter-follower transistor
5 25 is determined by an NPN current source transistor 27,
disposed with its collector electrode directly connected
to the emitter electrode of transistor 25 and its emitter
electrode returned to ground via resistor 28. The quiescent
current drawn by the emitter-follower transistor 21 at the
10 amplifier input is similarly determined by an NPN current
source transistor 23, disposed with its collector electrode
directly connected to the emitter electrode of transistor 21
and its emitter electrode returned to ground via resistor
24. A resistor 22 couples the base electrode of transistor
15 21 to the +5.2V. bias supply terminal. The base electrodes
of current source transistors 15, 23 and 27 are each
directly connected to the positive terminal (+1.2V.) of an
additional bias supply.

Amplifier output terminal O is linked to the
20 amplifier input terminal I by the series combination of a
piezoelectric crystal 35, a fixed capacitor 36, and a
resistor 38. Illustratively, crystal 35 is cut so as to
exhibit series resonance at a frequency in the immediate
vicinity of, but slightly below, the color subcarrier
25 frequency (e.g., 3.579545 MHz.) of the color television
signals to which the receiver responds. Accordingly,
crystal 35 appears inductive at the color subcarrier
frequency. The value of the fixed capacitor 36 is chosen
so that the series combination of elements 35 and 36
30 nominally exhibits series resonance at the color subcarrier
frequency, with the Q of the resonant system determined by
the resistance value of the series resistor 38 to establish
a suitable bandwidth (e.g., 1000 Hz.) for the bandpass
filter characteristic of the feedback path. A capacitor 39,
35 coupled between terminal I and ground, cooperates with
resistor 38 to provide significant attenuation for harmonics
of the desired operation frequency to substantially prevent
the sustaining of oscillations at such higher frequencies.
The bandpass characteristic provided by elements 35 and 36

1 allows positive feedback of an oscillation-sustaining
magnitude in the immediate vicinity of the color subcarrier
frequency. A precise match of the free-running operating
frequency to the color subcarrier frequency may not be
5 assured, however, because of practical tolerances associated
with elements 35 and 36. As will be subsequently described,
the system of the drawing includes additional apparatus
permitting adjustment of the free-running operating
frequency to a desired precise frequency.

10 For the purpose of synchronizing the above-
described oscillator in frequency and phase with a color
subcarrier reference of incoming color television signals,
the system of the drawing includes a phase comparator 54.
The local input to phase comparator 54 comprises
15 oscillations derived from terminal F at the base electrode
of input transistor 11. A chrominance amplifier 50 is
responsive to the chrominance component of incoming signals,
appearing at terminal C and inclusive of periodic
synchronizing bursts of oscillations of color subcarrier
20 frequency and a reference phase. An output of chrominance
amplifier 50 is supplied to a burst separator 52, which
delivers separated color synchronizing bursts to the other
input of phase comparator 54.

Phase comparator 54 functions to develop a control
25 voltage output having a magnitude and polarity indicative
of the magnitude and sense of whatever departure from a quadrature
phase difference may exist between the respective comparator inputs.
Illustratively, phase comparator 54 is of the type
developing push-pull outputs, providing complementary
30 control voltages at respective output terminals CV and CV'.
These control voltages are used to control the operation of
a phase shifted signal amplifier which shares load resistor
14 with the non-inverting amplifier 10.

-Phase shifted signals are derived from the output
35 terminal (P) of a phase shifter 40, 42, 41. The phase
shifter includes an inductor 40 connected between the
amplifier input terminal I and the phase shifter output
terminal P, and the series combination of resistor 42 and
capacitor 41 connected between terminal P and ground. The

1 values of the phase shifter elements are chosen so that a
lagging phase shift (equal to substantially 90° at the color
subcarrier frequency) is imparted to oscillations supplied
from terminal I. The phase shifted oscillations appearing
5 at the phase shifter output terminal P are coupled to a
matrix input terminal E via the base-emitter path of an NPN
emitter-follower transistor 43, disposed with its collector
electrode directly connected to the $+V_{CC}$ terminal, with
its base electrode directly connected to terminal P and
10 with its emitter electrode directly connected to terminal E.
The quiescent current drawn by transistor 43 is determined
by an NPN current source transistor 45, disposed with its
collector electrode directly connected to terminal E,
with its base electrode directly connected to
15 the +1.2V. bias supply terminal and with its emitter
electrode connected to ground via resistor 46.

A controlled amplifier, responsive to the control
outputs of comparator 54, includes a pair of NPN transistors
61 and 62, which are disposed as a differential amplifier
20 with interconnected emitter electrodes returned to ground
via the collector-emitter path of NPN current source
transistor 63 in series with its emitter resistor 64. The
base electrode of transistor 63 is directly connected to
the +1.2V. bias supply terminal. Phase shifted signals
25 from terminal E are applied to the base electrode of
transistor 61 via a matrixing resistor 56. Signals from
terminal F, at the input of the non-inverting amplifier 10,
are also applied to the base electrode of transistor 61
via a matrixing resistor 58. Bias is applied to the base
30 electrode of transistor 62 from terminal G (at the base
of transistor 13).

The collector electrode of transistor 61 supplies
an inverted version of the matrixed signals appearing at the
base electrode of transistor 61 to the interconnected
35 emitter electrodes of NPN transistors 65 and 66 via a
direct connection thereto. The collector electrode of
transistor 62 supplies a non-inverted version of the
matrixed signals appearing at the base electrode of
transistor 62 to the interconnected emitter electrodes of

1 NPN transistors 67 and 68 via a direct connection thereto.
The control potential output appearing at output terminal CV
of the phase comparator 54 is supplied to the base
electrodes of transistors 65 and 67, while the complemen-
5 tarily varying control potential output appearing at output
terminal CV' is supplied to the base electrodes of
transistors 66 and 68.

The collector electrodes of transistors 66 and 67
are directly connected to the $+V_{CC}$ supply terminal, while
10 the collector electrodes of transistors 65 and 68 are
directly connected to the collector electrode of transistor
13 so as to develop outputs across the shared load resistor
14. Also developing an output across resistor 14 is an
additional NPN transistor 70, disposed with its base-emitter
15 path directly in shunt with the base-emitter path of the
differential amplifier transistor 61, and with its
collector electrode directly connected to terminal S. The
base-emitter path of differential amplifier transistor 62
is directly shunted by the base-emitter path of a further
20 NPN transistor 72, which is disposed with its collector
electrode directly connected to the $+V_{CC}$ supply terminal.

In operation, when a color signal is being received,
a departure of one sense from a desired quadrature phase relationship
between the received synchronizing bursts and oscillations from terminal
25 F unbalances the control voltages at terminals CV and CV'
in a direction elevating the potential at the base
electrodes of transistors 65 and 67, while depressing the
potential at the base electrodes of transistors 66 and 68.
Under such circumstances, the magnitude of an inverted
30 version of the controlled amplifier input passed by
transistor 65 exceeds the magnitude of a non-inverted
version thereof passed by transistor 68. Conversely, a
departure of the opposite sense from the desired quadrature phase
relationship unbalances the control voltages in the opposite direction,
35 whereby the magnitude of the non-inverted version passed by transistor
68 exceeds the magnitude of the inverted version passed by
transistor 65. In each instance, the consequent injection
of phase-shifted signals into the oscillator loop alters
the oscillator's frequency in the particular direction.

1 appropriate to reduce the departure from the desired quadrature
phase difference between comparator inputs so as to produce the desired
synchronization.

It will be noted that the sharing of load resistor
14 by the non-inverting amplifier 10 and the controlled
5 amplifier of phase shifted signals results in a plurality
of collector electrodes being directly connected thereto.
Load resistor 14 is thus effectively shunted by parasitic
capacitances associated with each collector. In aggregate
this results in introduction of an undesired lagging
10 phase shift of sufficient magnitude to pose tuning range
and/or phase control asymmetry problems that require
correction if optimum performance is desired.

The matrixing of signals from terminals E and F
to form the signal input for the controlled amplifier is
15 part of the correction technique of the present embodiment
The ratio of resistance values for the matrixing resistors
56 and 58 is selected so that the resultant of matrixing
is shifted in phase in the leading direction, relative to
the phase of the quadrature phased signal at terminal E.

20 The magnitude of phase shift in the leading direction
substantially matches the magnitude of lagging phase
shift associated with the load circuit of non-inverting
amplifier 10. Additionally, the magnitude of the inverted
version of the matrixing resultant, which is injected by
25 the inverting amplifier 70 into the shared load, is
selected so that the vector sum of (a) such injected
signals and (b) the signal components delivered to the
shared load by the non-inverting amplifier's output
transistor 13, comprises signals substantially identical
30 in phase with the signals appearing at the base of the
non-inverting amplifier's input transistor 11.

By virtue of the above-described injection of
compensating signals from inverting amplifier 70, the
phase lag associated with the load circuit of the non-
35 inverting amplifier 10 has substantially no effect on the
free-running operation of the oscillator. For symmetry of
phase control action for the synchronizing loop, however,
compensation for the effect of the phase lag associated with
the shared load on the controlled amplifier's output must

1 additionally be provided. Such compensation is provided
through the lead introduction provided for the controlled
amplifier's input by the matrix 56, 58. The net effect of
this lead introduction and the lag associated with the
5 shared load is that the injected components from the
controlled amplifier will bear either a lagging quadrature
relationship or a leading quadrature relationship (as
appropriate to the adjustment required for synchronization)
to the (continuously present) resultant of the contributions
10 from transistors 70 and 13, whereby symmetry of control
action is assured.

In the specific arrangement shown in the drawing,
the inverting amplifier transistor 70 shares a current
source (transistor 63) with the differential amplifier
15 formed by transistors 61 and 62. Symmetry of operation of
the differential amplifier is preserved, in the presence
of such current source sharing, by the addition of
transistor 72 (desirably matched in structure to transistor
70) to additionally share the common current source, while
20 entrained (by virtue of its base connection to the base of
transistor 62) to vary its current in a manner complementary
to the variations of current drawn by transistor 70.
Attainment of the proper magnitude of compensating signal
injection by transistor 70 is readily achieved by selection
25 of appropriate emitter dimensions therefor (with transistor
72 suitably matched therewith).

As previously mentioned, it is desirable in
systems of the illustrated type to provide a facility for
adjustment of the free-running frequency of the color
30 reference oscillator, so that it may be set precisely to
a desired color subcarrier frequency. One known technique
for providing such a facility is employment of a variable
capacitor in the oscillator's feedback filter, as shown,
for example, in the aforementioned U.S. Patent No.
35 4,020,500.

In the system illustrated in the accompanying
drawing, however, a different technique (explained in detail
in U.S. Patent Application Serial No. 383,303 of R. Shanley et
al., entitled "Oscillator Synchronizing System Incorporating

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- 1 DC control of "Free-Running Frequency and filed May 28
1982, is employed. That U.S. Patent Application corresponds
to British Patent Application 8314409.

Phase shifted signals from terminal E are applied
5 as the signal input to an additional controlled amplifier
47, the output of which is coupled to terminal A at the
base electrode of the output emitter follower transistor
33 of the oscillator. An adjustable DC voltage from the
moveable tap of the potentiometer 48 (with fixed end
10 terminals connected respectively to the $+V_{CC}$ supply
terminal, and to ground) is supplied to the control
input terminal FR of amplifier 47. Amplifier 47 injects
into the oscillator loop phase shifted signals of a
magnitude and polarity dependent upon the magnitude and
15 sense of the departure of the potentiometer's tap position
from a balance setting. The injected component is a leading quadrature
component when upward adjustment from the free-running
frequency of the balance setting is desired, and a lagging
quadrature component when downward adjustment from the
20 free-running frequency of the balance setting is desired.

The embodiment of the invention described with
reference to the drawing includes a voltage controlled
oscillator incorporating compensation for adverse effects
of parasitic capacitance in a advantageous manner. This
25 permits attainment of a symmetrical phase control
characteristic for use in synchronization of the oscillator
with external reference oscillations.



1 CLAIMS:

1. A voltage controlled oscillator comprising

5 a non-inverting signal amplifier having an input terminal, a load resistor across which an output of said amplifier appears, and an output terminal coupled to said load resistor;

10 a band pass filter coupled between said output terminal and said input terminal of said non-inverting amplifier;

a phase shifter having an input terminal coupled to receive signals from said non-inverting amplifier and having an output terminal;

15 a phase comparator, having a first input terminal coupled to receive signals from said non-inverting amplifier, and a second input terminal coupled to receive a reference oscillatory signal, said phase comparator developing a control voltage having an amplitude and polarity indicative of the magnitude and sense of the departure, if any,
20 from a quadrature phase relationship between the respective signals appearing at its input terminals;

means for matrixing first signals appearing at said output terminal of said phase shifter with second signals derived directly from said non-inverting amplifier
25 to form resultant signals exhibiting a phase intermediate the phases of said first and second signals;

an inverting amplifier responsive to said resultant signals formed by said matrixing means for developing a phase-inverted version of said resultant
30 signals across said load resistor of a substantially fixed magnitude; and

controlled amplifier means, responsive to said resultant signals formed by said matrixing means and to said control voltage, and developing its output across said
35 load resistor, for subjecting said resultant signals to amplification with inversion when a departure of one sense occurs between the respective signals appearing



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1 Claim 1 continued:

at the input terminals of said phase comparator, and for
subjecting said resultant signals to amplification without
inversion when a departure of the opposite sense

5 occurs between the respective signals appearing at the
input terminals of said phase comparator, with the degree
of said amplification of said resultant signals being
dependent upon the magnitude of said departure from said
quadrature phase relationship.

10

2. Oscillator in accordance with claim 1 wherein
said phase shifter introduces a phase lag substantially
equal to 90° at the operating frequency of said oscillator.

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3. Oscillator in accordance with claim 2 wherein
stray capacitance associated with said load resistor impart
a phase lag to signal components developed across said
load resistor, by said non-inverting amplifier, and wherein
20 the parameters of said matrixing means and the gain of said
inverting amplifier are such that (1) the combination of
(a) said inverted version of said resultant signals
developed across said load resistor by said inverting
amplifier, and (b) said signal components developed across
25 said load resistor by said non-inverting amplifier, comprises
signals of substantially the same phase as the signals
appearing at said input terminal of said non-inverting
amplifier; whereas (2) the phase of the signals developed
across said load resistor by said controlled amplifier
30 means bears a substantially quadrature phase relation to
the phase of said signals appearing at said input terminal
of said non-inverting amplifier.



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- 1 4. Oscillator in accordance with claims 1 or 3,
 wherein said controlled amplifier means includes:
 first and second transistors disposed with
interconnected emitter electrodes;
5 a common current source coupled to said inter-
connected emitter electrodes;
 the base electrode of said first transistor
being responsive to the output of said matrixing
means;
10 means for maintaining the base electrode of said
second transistor at a predetermined bias potential;
 first amplifying means having a signal input
coupled to the collector electrode of said first transistor;
 second amplifying means having a signal input
15 coupled to the collector electrode of said second transistor;
 means, responsive to the control voltage output of
said phase comparator, for differentially varying the gain
of said first and second amplifying means; and
 means for combining the outputs of said first
20 and second amplifying means.

5. Oscillator in accordance with claim 4 wherein
said inverting amplifier comprises a third transistor
25 having a base-emitter path connected in shunt with the
base-emitter path of said first transistor, and having a
collector electrode connected to said load resistor.

- 30 6. Oscillator in accordance with claim 5 also
including a fourth transistor having a base-emitter path
connected in shunt with the base-emitter path of said
second transistor.

- 35 7. A voltage controlled oscillator substantially
as hereinbefore described with reference to the drawing.
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