function for reproducing content by a plurality of video information reproduction devices in synchronization with each other. The first synchronization signal processor 150 generates a first counter value Vcount1. The first counter value Vcount1 is a value incremented (counted up) by one at the timing of the first vertical synchronization signal Vsync1 sent from the first decoder 130. That is, the value of the first counter value Vcount1 is incremented each time the first vertical synchronization signal Vsync1 is output from the first decoder 130. In the first embodiment, for example, the first counter value Vcount1 has 8 bits (the number of bits is fixed to 8 bits) and is a value counted from 0 to 255. The first synchronization signal processor 150 sends the first vertical synchronization signal Vsync1 and the first counter value Vcount1 to the first control unit 110. If the first video information reproduction device 10 of a plurality of video information reproduction devices functions as a master device (a master), the first video information reproduction device 10 generates a phase synchronization signal Psync (PsyncOut in FIG. 1) containing the first vertical synchronization signal Vsync1 and the first counter value Vcount1 and sends it to a video information reproduction device as a slave device (a slave). If the first video information reproduction device 10 functions as the slave device, the first video information reproduction device 10 receives the phase synchronization signal Psync (PsyncIn in FIG. 1) sent from the video information reproduction device as the master device. At this time, the first synchronization signal processor 150 notifies the first clock generator 140 of clock correction information Fsync based on the phase synchronization signal Psync.

[0021]

FIG. 2 is a block diagram schematically showing a

first counter value Vcount, and a phase synchronization signal Psync in the first synchronization signal processor 150 of the first video information reproduction device 10 as the master device. The first vertical synchronization signal Vsync1 is a synchronization signal output from the first decoder 130. The first frequency divided clock signal Vclk1s is a clock signal obtained by frequency-dividing the first video clock signal Vclk1 output from the first decoder 130. The first counter value Vcount1 is an 8-bit counter value incremented at the timing of the first vertical synchronization signal Vsync1. The first counter value Vcount1 is held in a register or the like and is referred to by the first control unit 110. The phase synchronization signal Psync is generated by superimposing the first counter value Vcount1 on the first vertical synchronization signal Vsync1, and it is notified from the first synchronization signal processor 150 to the second synchronization signal processor 250 of the second video information reproduction device 20 as the slave device.

[0030]

The first synchronization signal processor 150 increments the first counter value Vcount1 each time a falling edge of the first vertical synchronization signal Vsync1 is detected on the basis of the first frequency divided clock signal Vclk1s. Next, the first synchronization signal processor 150 generates the phase synchronization signal Psync by superimposing the first counter value Vcount1 on the detected first vertical synchronization signal Vsync1 in a period of 8 clocks of the first frequency divided clock signal Vclk1s. In other words, the phase synchronization signal Psync has a waveform generated by obtaining a waveform by extending a "L" (low) section of the first vertical synchronization signal Vsync1 by 8 clocks of the frequency divided clock signal Vc1k1s and by adding, to the

8-clock-extended waveform section (a period indicated by a double-headed arrow in FIG. 3), a waveform of 8 bits which is information on the first counter value Vcount1. FIG. 3 shows that sections A1, A2, A3, and A4 respectively contain 0, which is "00000000" in binary (in FIG. 3, the bits are shown in reverse order), 1, which is "00000001" in binary (in FIG. 3, the bits are shown in reverse order), 2, which is "00000010" in binary (in FIG. 3, the bits are shown in reverse order), and 255, which is "11111111" in binary (in FIG. 3, the bits are shown in reverse order), as the first counter value Vcount1. After reaching "255", the first counter value Vcount1 returns to "0" and is incremented again.
[0031]

FIG. 4 is a timing chart showing signals in the second video information reproduction device 20 as the slave device according to the first embodiment. FIG. 4 schematically shows an example of a second frequency divided clock signal Vclk2s, the phase synchronization signal Psync, and a second counter value Vcount2 in the second synchronization signal processor 250 of the second video information reproduction device 20 as the slave device. The second frequency divided clock signal Vclk2s is a clock signal obtained by frequency-dividing the second video clock signal Vclk2 output from the second decoder 230. The phase synchronization signal Psync is a signal whose notification is sent from the first video information reproduction device 10 as the master device. The second counter value Vcount2 is an 8-bit counter value incremented at the timing of the second vertical synchronization signal Vsync2. The second counter value Vcount2 is stored in the register or the like and is referred to by the second control unit 210. In the first embodiment, however, the second video information reproduction device 20 works as the slave device. For this reason, the second counter value Vcount2 is not a value

incremented at the timing of the second vertical synchronization signal Vsync2 and is changed to a value of the first counter value Vcount1 extracted from the phase synchronization signal Psync.

[0032]

After the falling edge of the phase synchronization signal Psync is detected on the basis of the second frequency divided clock signal Vclk2s, the second synchronization signal processor 250 receives data of 8 clocks of the second frequency divided clock signal Vclk2s from the phase synchronization signal Psync, extracts the first counter value Vcount1 to be superimposed on the phase synchronization signal Psync, and stores it as the second counter value Vcount2 in a register or the like. Here, there is a difference of 8 clocks of the second frequency divided clock signal Vclk2s between a case where the second counter value Vcount2 is generated after the falling edge of the phase synchronization signal Psync is detected on the basis of the second video clock signal Vclk2 and another case where the second counter value Vcount2 is generated by extracting the first counter value Vcount1 from the phase synchronization signal Psync. For this reason, the second synchronization signal processor 250 provides a read prohibition period corresponding to 8 clocks of the second frequency divided clock signal Vclk2s, in the second counter value Vcount2, as shown in FIG. 4. Here, if the second control unit 210 tries to refer to the second counter value Vcount2 in the read prohibition period, the second control unit 210 cannot refer to the counter value. For this reason, it can be configured so that an indefinite value is set for the read prohibition period by the second synchronization signal processor 250 and the second control unit 210 accesses again if the second control unit 210 accesses in the read prohibition period.

[0033]

ahead of the "preparation time of No. (i+1)" in time, where i is an integer not smaller than 1. That is, i satisfying

$$\text{Preparation time of No. } i < \text{Acquired first current time} < \text{Preparation time of No. } (i+1)$$

is searched for. Consequently, the first control unit 110 determines that the content to be reproduced is the "content of No. i". Next, the first control unit 110 judges whether the "acquired first current time" is after the "preparation time of No. i" (step S33). If the "acquired first current time" is after the "preparation time of No. i" (YES in step S33), the first control unit 110 judges whether the "acquired first current time" is after the "reproduction time of No. i" (step S34). If the "acquired first current time" is after the "reproduction time of No. i," (YES in step S34), the first control unit 110 performs reproduction resume processing of "content of No. i" (step S35). If the "acquired first current time" is not after the "reproduction time of No. i" (NO in step S34), the first control unit 110 performs pre-reproduction processing for the first decoder 130 (step S36) and has the first decoder 130 prepare for content reproduction.

[0063]

As described above, in the first embodiment, the second decode reference clock signal Dclk2 in the second video information reproduction device 20 is compared with the decode reference clock signal Dclk1 in the first video information reproduction device 10, the frequency of the second decode reference clock signal Dclk2 is changed, and thus the second decode reference clock signal Dclk2 can be synchronized with the decode reference clock signal Dclk1. Moreover, the first current time in the second video information reproduction device 20 is synchronized with the first current time in the first video information reproduction device 10, and then the second video information

For example, if the video information reproduction system is configured by two video information reproduction devices, as shown in the first and second embodiments, and if each video information reproduction device stores content data in a storage unit (e.g., the first storage unit 100 and the second storage unit 200), the load on the network is light, and the time correction processing can be performed at short intervals. For this reason, in this case, each video information reproduction device sets the number of bits of the counter value (e.g., the number of bits of the first counter value Vcount1 and the number of bits of the second counter value Vcount2) to 4 bits.

[0079]

If the video information reproduction system is configured by more than two video information reproduction devices, and if streaming reproduction is performed, for example, the load on the network is heavy, and performing the time correction processing frequently is not preferable because it would increase the load on the network further. For this reason, in this case, each video information reproduction device sets the number of bits of the counter value to 10 bits.

[0080]

As described above, in the video information reproduction system according to the third embodiment, the number of bits of the counter value can be changed depending on the load on the network. For this reason, in the video information reproduction system according to the third embodiment, the time correction processing can be performed at appropriate intervals depending on the load on the network.

[0081]

<4> Fourth Embodiment

FIG. 16 is a block diagram schematically showing a configuration of a video information reproduction system

perform the time correction processing, receiving time correction information T_info whose notification is made by the first control unit 110 of the first video information reproduction device 10. The third time measurement unit 320 generates third time information of the third video information reproduction device 30. The third time information is referred to as the third current time by the third control unit 310. In the time correction processing, if the third control unit 310 sends a notification of a request to update the third time information, the third time measurement unit 320 changes (adjusts) the third time information and generates a third current time based on the changed third time information.

[0085]

The third decoder 330 receives the content data sent from the third control unit 310 as an input and generates a digital video signal VS3 on the basis of the third decode reference clock signal Dclk3 generated in the third clock generator 340. Here, the digital video signal VS3 includes at least a third video clock signal Vclk3, a third vertical synchronization signal Vsync3, and a horizontal synchronization signal Hsync3 as well as RGB data in the third video signal. The third decoder 330 outputs the digital video signal (video signal and the like), the third vertical synchronization signal Vsync3, and the horizontal synchronization signal Hsync3 to the third display unit 31 on the basis of the third video clock signal Vclk3. If the digital video signal VS3 is received, the third display unit 31 displays the content on a frame-by-frame basis on the basis of the third vertical synchronization signal Vsync3.

[0086]

The third synchronization signal processor 350 has a function for reproducing content by the third video information reproduction device 30, the first video