What is claimed is:

1. A method of controlling on-die termination (ODT) in a multi-rank memory system including a plurality of memory ranks, the method comprising:

enabling ODT circuits of the plurality of memory ranks into an initial state when the multi-rank memory system is powered on;

enabling the ODT circuits of a write target memory rank and non-target memory ranks among the plurality of memory ranks during a write operation; and

disabling the ODT circuit of a read target memory rank among the plurality of memory ranks while enabling the ODT circuits of non-target memory ranks among the plurality of memory ranks during a read operation,

wherein, enabling ODT circuits of the plurality of memory ranks into an initial state when the multi-rank memory system is powered on comprises electrically coupling termination resistor units to data input-output pins of the plurality of memory ranks,

wherein each of the ODT circuits of the plurality of memory ranks has a first resistance value in the initial state, and

wherein enabling the ODT circuits during the write operation comprises electrically coupling a termination resistor unit of the write target memory rank to a data input-output pin of the write target memory rank, and further comprises: changing a resistance value of the ODT circuit of the write target memory rank from the first resistance value to a second resistance value different from the first resistance value during the write operation.

2. The method of claim 1, wherein the second resistance value is greater than the first resistance value.

3. The method of claim 1, wherein enabling the ODT circuit of non-target memory ranks during the read operation comprises:

maintaining the ODT circuits of the non-target memory ranks in the initial state to have the first resistance value during the read operation.

4. The method of claim 1, wherein the ODT circuits of the plurality of memory ranks are configured to terminate the data input-output pins of the plurality of memory ranks.

5. The method of claim 4, wherein the ODT circuits of the plurality of memory ranks maintain the initial state even while a data input-output operation through the data input-output pins is not performed.

6. The method of claim 1, wherein the ODT circuits of the non-target memory ranks among the plurality of memory ranks except the write target memory rank or the read target memory rank have a constant resistance value regardless of a memory access command from a memory controller.

7. The method of claim 6, wherein the constant resistance value of the non-target memory ranks is determined based on a value stored in a mode register of the multi-rank memory system.

8. The method of claim 1, wherein the write target memory rank or the read target memory rank is converted from a power-down mode to a normal operation mode to perform the write operation or the read operation, and the non-target memory ranks among the plurality of memory ranks except the write target memory rank or the read target memory

rank maintain the power-down mode during the write operation or the read operation.

9. A system comprising:

a plurality of memory ranks including a plurality of memory devices; and

a memory controller configured to control the plurality of memory ranks,

wherein on die termination (ODT) circuits of the plurality of memory ranks are enabled into an initial state when the system is powered on, the ODT circuits of the plurality of memory ranks are enabled during a write operation with respect to a write target memory rank and non-target memory ranks among the plurality of memory ranks, and the ODT circuit of a read target memory rank among the plurality of memory ranks is disabled while the ODT circuits of non-target memory ranks among the plurality of memory ranks are enabled during a read operation;

wherein termination resistor units are electrically coupled to data input-output pins of the plurality of memory ranks when the plurality of memory ranks are enabled into the initial state,

wherein the ODT circuits of the plurality of memory ranks have a first resistance value in the initial state; and

wherein, when the ODT circuits are enabled during the write operation, a termination resistor unit of the write target memory rank is electrically coupled to a data input-output pin of the write target memory rank, and further wherein a resistance value of the ODT circuit of the write target memory rank is changed from the first resistance value to a second resistance value different from the first resistance value during the write operation.

10. The system of claim 9, wherein the ODT circuits of the non-target memory

ranks among the plurality of memory ranks except the write target memory rank or the read target memory rank have a constant resistance value regardless of a memory access command from the memory controller.

11. The system of claim 9 or claim 10, wherein the second resistance value is greater than the first resistance value.

12. A system comprising:

a first memory rank comprising a plurality of first memory devices connected to a first on die termination (ODT) circuit, the first ODT circuit comprising a first termination resistor unit; and

a second memory rank comprising a plurality of second memory devices connected to a second ODT circuit, the second ODT circuit comprising a second termination resistor unit,

wherein the second termination resistor unit is electrically coupled to a second data input-output pin when the second ODT circuit is enabled,

wherein the first and second ODT circuits are enabled during a write operation of the first memory rank, and the first ODT circuit is disabled and the second ODT circuit is enabled during a read operation of the first memory rank;

wherein when the first ODT circuit is enabled during the write operation, the first termination resistor unit is electrically coupled to a first data input-output pin, and further the resistance value of the enabled first ODT circuit is changed from a first resistance value to a second resistance value different from the first resistance value during the write operation.

13. The system of claim 12, wherein each enabled ODT circuit provides termination impedance to a transmission line coupled to a data input-output pin of the corresponding memory rank.

14. The system of claim 12, wherein the first ODT circuit is disabled during the read operation only while read data corresponding to the read operation is output from the first data input-output pin.

15. The system of any of claims 12 to 14, wherein the second resistance value is greater than the first resistance value.

16. A method of operating a low power double data rate 5 (LPDDR5) dynamic random access memory (DRAM) in a multi-rank memory system including a plurality of memory ranks, the method comprising:

receiving a write command dedicated to a first memory rank among the plurality of memory ranks, wherein the write command conforms to an LPDDR5 standard and is not dedicated to a second memory rank among the plurality of memory ranks;

enabling a reception buffer in the first memory rank;

disabling a transmission driver in the first memory rank;

disabling a reception buffer and a transmission driver in the second memory rank;

receiving a data strobe signal pair;

enabling on-die terminal (ODT) circuits of the first memory rank and the second memory rank in response to the write command;

receiving data signals while the data strobe signal pair is toggled during the enabling

of the ODT circuits of the first memory rank and the second memory rank;

receiving a read command dedicated to the first memory rank, wherein the read command conforms to the LPDDR5 standard and is not dedicated to the second memory rank;

enabling the transmission driver in the first memory rank;

disabling the reception buffer in the first memory rank;

disabling the reception buffer and the transmission driver in the second memory rank;

disabling the ODT circuit of the first memory rank and enabling the ODT circuit of the second memory rank in response to the read command; and

sending data signals while the data strobe signal pair is toggled during the disabling of the ODT circuit of the first memory rank and the enabling of the ODT circuit of the second memory rank.

17. The method of claim 16, wherein the first memory rank is a target memory rank and the second memory rank is a non-target memory rank.

18. The method of claim 17, wherein the ODT circuits of the plurality of memory ranks have a first resistance value in an initial state.

19. The method of claim 18, wherein the enabling of the ODT circuits of the first memory rank and the second memory rank in response to the write command comprises maintaining the ODT circuits of the plurality of memory ranks in the initial state to have the first resistance value.

20. The method of claim 18, wherein the enabling of the ODT circuits of the first memory rank and the second memory rank in response to the write command comprises storing the first resistance value in a mode register.

21. The method of claim 18, wherein the enabling of the ODT circuit of the second memory rank in response to the read command comprises maintaining the ODT circuits of the plurality of memory ranks in the initial state to have the first resistance value.

22. The method of claim 18, wherein the enabling of the ODT circuit of the second memory rank in response to the read command comprises storing the first resistance value in a mode register.