9800537-4
13-3-98
IPOS

SPECIFICATION

TITLE OF THE INVENTION

Semiconductor device and method of manufacturing the same

BACKGROUND OF THE INVENTION

The present invention relates to a technique effective when applied to a semiconductor device having a structure such that inner leads among leads are arranged on a circuit formation face of a semiconductor chip encapsulated in a package body.

There is a package having an LOC (Lead On Chip) structure as one of surface mount type LSI packages. The package has a structure such that inner leads among leads are arranged via a tape-shaped insulating film on the main surface of a semiconductor chip, that is, on a circuit formation face on which a plurality of semiconductor devices and bonding pads are formed and the inner leads and the bonding pads on the semiconductor chip are electrically connected by Au wires. The insulating film has a laminated structure obtained by coating an adhesive on both faces of a base film made of a heat-resisting resin such as polyimide. The packing having the LOC structure of this kind is described in, for example, Japanese Patent Application Laid-Open Nos. 61-218139, 61-236130, and the like.

On the other hand, since engineering workstations and personal computers of recent years require a memory

This Sheet Has Been Replaced EN

(RAM) of a large capacity in order to process a large amount of data at high speed, a technique of laminating a memory module is being examined.

As a specific example, a laminated-type memory module in which a plurality of thin LSI packages such as TSOPs (Thin Small Outline Packages) and TSOJs (Thin Small Outline J-lead Packages) are piled up and outer leads of the upper and lower packages are connected by soldering or the like and are fixed on a printed wiring board is known. For example, a technique is described in Japanese Patent Application Laid-Open No. 5-175406 such that outer leads of TSOJs are bent upward in the middle and a part of each of the outer leads is extended in the horizontal direction, thereby overlapping the leads of the upper and lower packages.

SUMMARY OF THE INVENTION

In the conventional package having the LOC structure, an insulating film having the thickness of about 50 μm is interposed between a semiconductor chip and inner leads, and it is one of the causes which prevent the thickness of the package from being reduced. Further, in case of manufacturing the laminated type memory module by using the conventional LOC structured package, the cause also disturbs reduction in thickness of the module.

The inventors have examined a technique of joining the inner leads and the semiconductor chip with an

This Sheet Has Been Replaced



EN

adhesive without using the insulating film. The following is not a known technique but is a technique examined by the inventors. The outline is as follows.

That is, when it is considered that the inner leads are joined to the circuit formation face of the semiconductor chip with the adhesive, if an insulating tape is adhered to a lead frame or the semiconductor chip, one joining process is necessary. On the contrary, in case of applying the adhesive to the inner lead parts, the adhesive has to be applied to each of the plurality of inner leads from a dispenser, so that the adhesive applying work takes time. Since the workability is not preferable, it is a problem in view of improvement in manufacturing efficiency of the semiconductor device having the LOC structure. Consequently, it is considered that the adhesive is not applied to all of the inner leads but is applied to some selected inner leads. In this case, since the joined area of the semiconductor chip and the lead frame is reduced as a whole, the semiconductor chip is deviated from the lead frame upon formation of the package body by resin encapsulation. A joining method which can hold joining strength of the semiconductor chip to the lead frame at the time of the resin encapsulation without applying the adhesive to all of the inner leads has been examined.

In case of joining the inner leads to the circuit formation face of the semiconductor chip by using an

This Sheet Has Been Replaced



adhesive, it is estimated that factors caused by temperature cycling or thermal cycling among the adhesive, the inner leads, and the semiconductor chip have to be considered more than a case of joining the inner leads to the circuit formation face by using the insulating tape. In case of using the insulating tape, since all of the inner leads are joined by the integral continuous insulating tape, thermal distortion caused by a difference in thermal expansion and contraction values of the inner leads, the semiconductor chip, and the insulating tape due to the temperature cycling can be absorbed by the integral continuous insulating tape. By contrast, in case of joining the inner leads to the semiconductor chip by using the adhesive having a coefficient of thermal expansion which is close to that of the insulating tape, the adhesive is applied in spots to the respective inner leads and the applied adhesive is separated and independent. It can be therefore considered that the thermal distortion cannot be absorbed as the insulating tape does. When the thermal distortion cannot be absorbed, stress is concentrated on the joining parts and a problem such that the parts are disconnected occurs, so that durability of the semiconductor device cannot be improved.

On the main face, that is, on the circuit formation face of the semiconductor chip, after forming a semiconductor integrated circuit on a silicon wafer, a

This Sheet Has Been Replaced EN

surface protective layer made of a resin is applied and formed in order to protect the circuit from radiation such as alpha-ray emitted to the circuit. In other words, the circuit formation face is covered by the surface protective layer made of a resin except for the bonding pads. In case of joining the circuit formation face to the inner leads, if the semiconductor chip is joined to the inner leads by using the adhesive applied near the outer peripheral edge of the semiconductor chip, it can be considered that the surface protective layer made of a resin is peeled off or rolled up from the outer periphery by the thermally distorted adhesive and inner leads. When the protective layer is peeled off from the edge part, it is assumed that a crack occurs along the inner lead in the package body made of a resin, that is, an inconvenience of so-called a resin crack occurs.

In case of joining the inner leads and the circuit formation face by using the insulating tape, the insulating tape has the thickness of about 50 μm. By contrast, in case of directly joining the inner leads to the circuit formation face with the adhesive, the thickness of the adhesive can be suppressed to about 10 μm. Although an advantage that the thickness of an LSI package can be reduced can be considered, occurrence of a problem due to a fact that the inner leads are close to the circuit formation face of the semiconductor chip can be considered. The semiconductor chip is

This Sheet Has Been Replaced



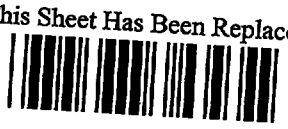
manufactured in such a manner that a semiconductor wafer is formed, and after that, the semiconductor wafer is cut along scribing lines in a dicing process into semiconductor chips. Since dummy elements and metal wiring used for an evaluation pattern are formed in the scribing lines, a group of circuit wiring made of metals such as aluminum remains as remnants in a part around each semiconductor chip substrate. If the remnants occur, since the remnants have the height of about 10 μm from the circuit formation face in the outer peripheral part of the semiconductor chip, it is feared that the remnants are brought into contact with the inner leads and the remnants and the inner leads are short-circuited.

The occurrence of the remnants is not a problem when the semiconductor chip and the inner leads are joined by using the insulating tape having the thickness of about 50 μm. In case of directly joining the semiconductor chip and the inner leads by using only the adhesive of the thickness of about 10 μm, however, it is assumed that the above-mentioned problem occurs when the inner leads approach the circuit formation face.

It can be considered that if those problems exist, it is difficult to manufacture a high-quality semiconductor device of the LOC structure with a good yield.

It is, therefore, an object of the present invention to provide a technique which can promptly

This Sheet Has Been Replaced



EN

manufacture a semiconductor device of the LOC structure and efficiently improve manufacturing efficiency of the semiconductor device.

It is another object of the present invention to provide a technique which can manufacture a high-quality semiconductor device having the LOC structure with a good yield.

The above and other objects and novel features of the present invention will become apparent from the following description of the specification and the accompanying drawings.

Among inventions disclosed in this application, the outlines of representative ones will be briefly described as follows.

According to the present invention, there is provided a semiconductor device in which a plurality of inner leads are arranged on a circuit formation face of a semiconductor chip encapsulated with a resin, and external terminals (bonding pads) formed on the circuit formation face and the inner leads are electrically connected. Only the inner leads arranged on both ends of the semiconductor chip among the plurality of inner leads are selectively joined to the circuit formation face of the semiconductor chip with the adhesive.

According to the present invention, a semiconductor chip is connected to at least four inner leads positioning on both end parts of the semiconductor

This Sheet Has Been Replaced

chip without joining all of inner leads and the semiconductor chip, so that the area in which the adhesive is applied is reduced and the adhesive can be promptly applied. Further, in case of forming the package body by using a resin, a semiconductor package is stably held by a lead frame in a molding die. Consequently, a high-quality semiconductor device can be manufactured with a good yield.

The semiconductor device of the present invention has a feature such that a plurality of inner leads includes inner leads having joining parts which are joined to a circuit formation face of a semiconductor chip with an adhesive and a bent part for absorbing stress at the time of temperature cycling is formed in each inner lead having the joining part.

According to the present invention, even when stress is concentrated on the joining part of the inner lead and the chip, the stress is absorbed by the bent part. Consequently, it is prevented that large stress or distortion occurs in the circuit formation face or the inner leads, and further, the surface protective layer covering the circuit formation face is prevented from being peeled off.

Further, according to a semiconductor device of the present invention, a plurality of inner leads include inner leads having joining parts to be joined to the circuit formation face of the semiconductor chip with

This Sheet Has Been Replaced

an adhesive. A gap between the circuit formation face and a part of each of the inner leads having the joining parts, which is over the outer peripheral edge of the semiconductor chip is set to be higher than the height of remnants occurring in the outer periphery of the semiconductor chip.

According to the present invention, even when the thickness of the adhesive used to join the inner leads to the chip is as thin as about 10 μm, it is avoided that the remnants which may occur in the outer peripheral edge of the semiconductor chip come into contact with the inner leads.

In the present invention, the inner lead may have the joining part and the bent part. The joining part can be also formed in the inner lead connected to a bus bar (power source lead).

A method of manufacturing a semiconductor device of the present invention comprises the steps of: preparing a lead frame having a plurality of inner leads and a plurality of outer leads continuous to the inner leads, respectively; preparing a semiconductor chip having a square-shaped circuit formation face on which a semiconductor integrated circuit is formed; applying an adhesive to the inner leads arranged on both ends of the semiconductor chip among the inner leads; joining the semiconductor chip to the lead frame with the adhesive; electrically connecting electrodes arranged

This Sheet Has Been Replaced

on the circuit formation face of the semiconductor chip and the inner leads; and forming a resin encapsulating body by arranging the lead frame to which the semiconductor chip is joined in a resin molding die, and after that, injecting a melt encapsulation resin into the resin molding die in a state where the semiconductor chip is held by the lead frame at the both end parts.

According to the present invention, when the inner leads positioning on both ends of the semiconductor chip are joined and the package body is formed by using the resin, the encapsulation resin in a melted state is injected into the resin molding die in a state where the semiconductor chip is held at the both ends by the lead frame. Consequently, the semiconductor chip is not deviated from the lead frame in the die and a high-quality semiconductor device can be therefore manufactured.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a plan view illustrating a main part of a semiconductor package as a first embodiment of the present invention;

Figs. 2(A) and 2(B) are cross sections taken on lines 2-2 and 2'-2' of Fig. 1, respectively;

Fig. 3 is a cross section taken on line 3-3 of Fig. 1;

Fig. 4(A) is a plan view partially and enlargedly showing a part around an inner lead 12Aa shown in Fig.1,

This Sheet Has Been Replaced

Fig. 4(B) is a cross section taken on line A-A of Fig. 4(A), and Fig. 4(C) is a cross section showing a modification of Fig. 4(B);

Fig. 5 is a plan view showing a main part of a lead frame for manufacturing the semiconductor device shown in Fig. 1;

Fig. 6 is a plan view showing a state in which an adhesive is applied to inner lead parts positioning on the outermost sides of the lead frame shown in Fig. 5;

Fig. 7 is a plan view showing a state in which a chip is joined to the lead frame shown in Fig. 6;

Fig. 8 is a plan view illustrating a state in which wires are connected between bonding pads and the inner leads in the lead frame shown in Fig. 7;

Fig. 9 is a plan view showing a state in which a chip is encapsulated with a resin in the lead frame shown in Fig. 8;

Fig. 10 is a plan view illustrating a state in which dam bars and outer leads are cut in the lead frame shown in Fig. 9;

Fig. 11 is a plan view illustrating a state in which leads are formed in the lead frame shown in Fig.10;

Fig. 12 is a plan view illustrating a state in which suspension leads are cut in the lead frame shown in Fig. 11;

Fig. 13 is a cross section illustrating a molding die for molding a resin encapsulating body of the package

This Sheet Has Been Replaced

shown in Fig. 1;

Fig. 14 is a plan view showing a main part of a semiconductor package as a second embodiment of the present invention;

Fig. 15(A) is a plan view partially and enlargedly illustrating a part around an inner lead 12Aa shown in Fig. 14, and Fig. 15(B) is a cross section taken online A-A of Fig. 15(A);

Fig. 16(A) is a plan view enlargedly showing a main part of a semiconductor package as a modification of the second embodiment of the present invention, and Fig. 16(B) is a cross section taken on line A-A of Fig. 16(A);

Fig. 17 is a plan view showing a main part of a semiconductor package as a third embodiment of the present invention;

Fig. 18 is a plan view partially and enlargedly illustrating a part around an inner lead 12Aa shown in Fig. 17;

Fig. 19 is a plan view showing a main part of a semiconductor package according to a fourth embodiment of the present invention;

Fig. 20 is a plan view partially and enlargedly illustrating a part around an inner lead 12Aa shown in Fig. 19;

Fig. 21 is a plan view showing a main part of a semiconductor package as a fifth embodiment of the present invention;

This Sheet Has Been Replaced

Fig. 22 is a plan view showing a main part of a semiconductor package as a sixth embodiment of the present invention;

Fig. 23 is a cross section of a main part of a semiconductor package as a seventh embodiment of the present invention; and

Figs. 24(A) and 24(B) are cross sections of a semiconductor device having a laminated memory module structure as an eighth embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be described in detail hereinafter with reference to the drawings.

Fig. 1 is a plan view illustrating a semiconductor device according to an embodiment of the present invention. Figs. 2(A) and 2(B) are cross sections taken on lines 2-2 and 2'-2' of Fig. 1, respectively. Fig. 3 is across section taken on line 3-3 of Fig. 1.

The illustrated semiconductor device is a TSOP as a kind of the surface mount type LSI package. In a resin encapsulating body 10 made of an epoxy resin formed by transfer molding, a semiconductor chip (hereinafter, simply called a "chip") 11 made of a single crystal silicon on which a memory LSI such as a DRAM (Dynamic Random Access Memory) is formed is encapsulated. Each

This Sheet Has Been Replaced

of the chip 11 and the resin encapsulating body 10 has a rectangle shape having two long sides which are in parallel and two short sides which are in parallel. The long and short sides make right angles. The TSOP includes a plurality of leads12 having outer lead parts 12B projecting from the resin encapsulating body to the outside and inner lead parts 12A arranged on the main face, that is, a circuit formation face of the chip 11. The leads 12 are made of a Cu or Fe alloy and are electrically connected to a number of bonding pads 15 serving as external terminals formed in a line in the central part of a circuit formation face 14 of the chip 11 via Au wires 13.

According to the TSOP, the thickness of the chip 11 is 0.28 mm, the plate thickness of the lead 12 is 0.07 to 0.125 mm, and the thickness of the resin encapsulating body 10 is about 0.6 to 1.0 mm.

The inner lead parts 12A are arranged on the circuit formation face 14 so as to extend from the long sides of the chip 11 toward the bonding pads 15 and are arranged at predetermined intervals in a direction parallel to the line of the bonding pads 15, that is, in the longitudinal direction of the chip 11. That is, on the inner side of each of inner lead parts 12Aa positioning on both ends of the chip 11 (that is, positioning on the outermost sides of the chip 11), another inner lead part 12Ab neighboring the inner lead part 12Aa with a gap is

This Sheet Has Been Replaced

positioned. Further, on the inner side of each inner lead part 12Ab, another inner lead part 12Ac neighboring the inner lead part 12Ab with a gap is positioned. In this manner, a predetermined number of inner lead parts 12A are arranged in the direction along the line of the pads of the chip 11 with gaps. The inner lead part 12Aa serves as a power source lead (fixed potential lead) for supplying a power source potential and an earth potential and the inner lead parts 12Ab and 12Ac serve as signal leads.

In the TSOP, four inner lead parts 12Aa positioning on the outermost sides and the chip 11 are joined with an adhesive 21 as shown in Figs. 2(A) and 2(B) without using an insulating tape for joining all of the inner lead parts 12A to the circuit formation face 14 of the chip. As the adhesive 21, for example, thermoplastic polyimide resin is used.

The position to which the inner lead part 12Aa is bonded to the chip 11 with the adhesive 21 is slightly on the inner side of the edge of the chip 11. That is, the tip of each of the four inner lead parts 12Aa serves as a joining part 22 to be joined to the circuit formation face 14 with the adhesive 21. The joining parts 22 are shown by hatched parts in Fig. 1. Each of the wires 13 is connected onto a face of the inner lead part 12Aa opposite to the face on which the adhesive 21is applied.

Consequently, the chip 11 is joined to the four

This Sheet Has Been Replaced

inner lead parts 12A positioning on the outermost sides and the other inner lead parts 12Aa positioning on the inner sides are not joined on the chip 11 as shown in Fig. 3. Although the chip 11 shown in the diagram is bonded to the total four inner lead parts 12Aa positioning on both ends, the chip 11 may also be joined to a total of eight inner leads including the four inner lead parts 12Ab on the inner sides of the four inner leads 12Aa. Although the adhesive 21 is applied on spots in the illustrated case, the adhesive 21 can also be applied in a wider range or a whole part of the inner lead parts 12Aa which overlaps the circuit formation face 14.

As mentioned above, since the number of parts to which the adhesive 21 is applied is four or eight without joining all of the inner lead parts 12A to the chip 11, the joining area can be reduced. Since a work of applying the adhesive using an apparatus such as dispenser for applying the adhesive 21 can be promptly performed and a water amount absorbed by the adhesive can be reduced, manufacturing efficiency of the semiconductor device can be improved. Since the chip 11 is joined to the inner lead parts 12Aa on the outermost sides, in a resin forming step using a transfer molding apparatus for forming the resin encapsulating body 10, a desired resin shape can be formed and the chip 11 is not deviated from the lead frame or inclined by the pressure of injection of the resin even when the resin is injected into the cavity

This Sheet Has Been Replaced



of the die in a state where the chip 11 joined to the lead frame is arranged in the resin molding die.

Fig. 4(A) enlargedly shows one of the four inner lead parts 12Aa each having the joining part 22 shown in Fig. 1. The inner lead part 12Aa has a bent part 23 which is bent at an almost right angle with the joining part 22 along the circuit formation face 14 of the chip 11. When the illustrated TSOP as a semiconductor device is used, the semiconductor device is subjected to a thermal load by a change in temperature of the environment. In this case, since the materials of the chip 11, the inner lead parts 12A, the adhesive 21, and the encapsulating body 10 constructing the semiconductor device are different, the coefficients of thermal expansion of them are accordingly different. It can be therefore considered that the thermal expansion or thermal contraction does not occur uniformly in the whole semiconductor device but the thermal stress is concentrated on the joining part 22 by the temperature change, that is, the temperature cycling.

Since each inner lead part 12Aa having the joining part 22 includes the bent part 23, however, the thermal stress is absorbed by the bent part 23. Breakage of the inner lead part 12Aa can be therefore prevented. As a result, an effect such that the high-quality semiconductor device having excellent durability can be obtained while increasing the manufacturing efficiency

This Sheet Has Been Replaced



EN

of the semiconductor device.

In case of joining the inner lead part 12Aa to the chip 11 with the adhesive 21, the thickness of the adhesive 21 can be set to about 10μm which is thinner than that of the insulating tape. On the other hand, in case of manufacturing the chip 11, after semiconductor integrated circuits of the number corresponding to the predetermined number of chips are formed on a wafer, the wafer is cut on a chip unit basis in a dicing process. There is, however, a case that remnants occur in a part of the outer periphery edge E of the chip 11 at the time of cutting in the dicing process. The remnants are formed almost vertically from the edge E on the circuit formation face 14. It is found that the height of the remnant is about 10μm.

When the inner leads 12A including the joining parts 22 are extended in parallel on the circuit formation face 14, if remnants occur, the inner lead parts 12Aa come into contact with the remnants. If the remnants are those of a circuit wiring part made of a metal, the remnants and the inner leads 12 are short-circuited. If the remnants are those of the substrate part of the chip 11, the remnants and the substrate are short-circuited.

As shown in Fig. 4(B), a dimension between the circuit formation face 14 of the chip 11 and a part of the inner lead part 12Aa having the joining part 22, which is over the outer peripheral edge E of the chip 11 is

This Sheet Has Been Replaced

set to be higher than the height of the remnant which may occur on the chip outer periphery. In order to set the dimension, a step 24 inclined in the direction away from the circuit formation face 14 toward the outer lead part 12B is formed in the part which is over the outer periphery edge E in the inner lead part 12Aa. The illustrated step 24 is positioned on the inner side of the edge E of the chip 11. By forming the step 24 in this manner, even when the inner lead part 12Aa is joined to the chip 11 by using the thin adhesive 21, the contact of the inner lead part 12Aa and the remnants can be avoided. Thus, a high-quality semiconductor device can be obtained with a good yield.

As mentioned above, the effect of avoiding the contact between the inner lead part 12A and the remnants is obtained also in the case where all of the inner lead parts 12A have the joining parts 22 and the chip 11 and all of the inner lead parts 12A are joined.

Fig. 4(C) is a cross section showing a part which corresponds to that of Fig. 4(B) of a semiconductor device according to another embodiment of the present invention. In this case, in a manner similar to the case of the insulating tape, the adhesive 21 is applied thickly so that the thickness is about up to 50 μm. In this case, since a gap between the inner lead part 12A and the circuit formation face 14 is sufficiently larger than the height of the remnant which may occur, even the adhesive 21 is

This Sheet Has Been Replaced



thickly applied in this way, the effect that the contact between the inner lead part 12A and the remnants can be avoided is obtained without forming the step 24 as mentioned above.

In the semiconductor device shown in Fig. 1, although the bonding pads 15 serving as electrodes are formed in a line in the center part of the chip 11, the bonding pads 15 may be formed in two lines in the center part of the chip 11. In this case, the joining part 22 of the inner lead part 12Aa is positioned close to the long side of the chip 11 and the joining parts 22 of the four inner lead parts 12Aa are positioned at the four corners of the chip 11, so that the deviation or inclination of the chip 11 in the die can be certainly prevented upon formation of the encapsulation body 10. It is also possible that the joining parts 22 are positioned at the four corners of the chip 11 even if the bonding pads 15 are formed in a line as shown in the diagram.

The procedure for manufacturing the TSOP as the above-mentioned semiconductor device will be described. First, a lead frame LF having the shape as shown in Fig. 5 is prepared. The lead frame LF includes outer frames 12E and 12F, dam bars 12C connecting the leads 12, and suspension leads 12D. A structure in which about five or six lead frames LF are continuous is actually employed. Fig. 5 shows only a part corresponding to one of the

This Sheet Has Been Replaced

packages. The step 24 is formed only at the end part of each of the inner lead parts 12Aa on the outermost sides of the lead frame LF so as to be offset.

As shown in Fig. 6 corresponding to the back face of Fig. 5, the adhesive 21 is applied in spots on the back face of the four inner lead parts 12Aa on the outermost sides among the inner lead parts 12A in the lead frame LF, that is, on a surface facing the chip 11 by using a dispenser or the like. It is also possible that the adhesive 21 is applied to the whole part overlapping the circuit formation face 14 of the chip 11 among the inner lead parts 12Aa or an adhesive in a sheet state which is preliminarily cut in a size corresponding to the overlapped part may be joined to the joining parts 22 without using the dispenser.

The chip 11 has been prepared by predetermined processes and has a rectangular shape. As shown in Fig. 7, the chip 11 is positioned in a predetermined position of the lead frame LF so that the circuit formation face of the chip 11, that is, the main surface faces the rear face of the inner lead parts 12A. The joining parts 22 are brought into contact with the circuit formation face 14 and are joined with the adhesive 21. The chip 11 is joined to the four joining parts 22 which are arranged in such a manner that two each of the joining parts 22 correspond to each of both ends of the chip 11.

Fig. 8 shows a state in which the bonding pads 15

This Sheet Has Been Replaced

of the chip 11 and the inner lead parts 12A are bonded via the Au wires 13 in a wire bonding process and are electrically connected. The chip 11 is bonded and fixed in this manner, the lead frame LF to which the wires 13 are connected is conveyed to an encapsulating process, and the resin encapsulating body 10 is formed by a transfer molding apparatus, thereby encapsulating the chip 11 as shown in Fig. 9. After that, as shown in Fig. 10, the ends of the dam bars 12C connecting the outer lead parts 12B in the lead frame LF and the outer lead parts 12B which are exposed from the resin encapsulating body 10 as shown in Fig. 10 are sequentially cut. Subsequently, as shown in Fig. 11, the outer leads 12B are bent in a predetermined shape, for example, at lines G. The suspension leads 12D remain without being cut so that the package is not separated from the lead frame LF upon formation of the leads. After that, as shown in Fig. 12, by cutting the suspension leads 12D, the TSOP shown in Figs. 1 to 3 is completed.

Fig. 13 is a diagram showing a state in which the resin encapsulating body 10 is formed by the transfer molding apparatus. A cavity 33 corresponding to the shape of the resin encapsulating body 10 is formed by a first die 31 and a second die 32 of the molding apparatus. A melted epoxy resin 34 is injected into the cavity 33 from a gate 35 formed in the dies 31 and32 in correspondence to the center part of one of the short

This Sheet Has Been Replaced

sides of the chip 11. In this case, since the chip 11 is held by a total of four positions of two positions each on both sides of the lead frame LF, even when the injected resin 34 is injected into the chip side and the opposite side of the lead frame LF at different timing, the chip 11 is not deviated or inclined from the lead frame LF. Consequently, the chip 11 is encapsulated in a desired position in the lead frame LF, so that the high-quality semiconductor device can be manufactured with a good yield.

(embodiment 2)

Fig. 14 and Figs. 15(A) and 15(B) show a semiconductor device according to another embodiment of the present invention. Although the joining parts 22 are oriented in the width direction of the chip 11 in the foregoing embodiment, in this semiconductor device, they are oriented in the longitudinal direction of the chip 11. In this manner, the orientation of the joining parts 22 or the bent parts 23 can be set in arbitrary directions in accordance with the layout of the inner leads 12A. The step 24 formed in the inner lead parts 12Aa in this case is formed in the region of the chip 11. The step 24 may be formed in any position as long as a sufficient gap between the chip 11 and the remnants which may occur at the edge E of the outer periphery of the chip do not come into contact with the inner lead parts 12Aa can be obtained. Fig. 15(B) is across section

This Sheet Has Been Replaced

taken on line A-A of Fig. 15(A).

Fig. 16(A) is an enlarged view of a modification of the inner lead parts 12Aa shown in Fig. 14. Although the bent part 23 of the inner lead part 12Aa which is positioned on the outermost side of the chip 11 and has the bonding part 22 crosses the short side SE of the chip 11 in the embodiment of Fig. 14, the bent part 23 crosses the long side LE in Fig. 16(A). When lines of the bonding pads 15 are positioned relatively near the long side like the case where the bonding pads 15 are formed in two lines in the central part in the width direction of the chip 11, the bonding parts 22 are positioned near the long side as well, so that the inner lead parts 12Aa cross the long side.

Fig. 16(B) is a cross section taken on line A-A of Fig. 16(A) in which the encapsulating body 10 is omitted.

As shown in Fig. 16(A), the adhesive 21 is applied near the outer peripheral edge E of the chip 11 in the semiconductor device. The inner lead part 12Aa is joined near the chip outer peripheral edge E on the circuit formation face 14. The circuit formation face 14 of the chip 11 is formed by a surface protective layer made of a resin applied on the chip substrate in order to prevent an influence by radiation rays such as alpha-ray emitted to the circuit. The surface protective layer is peeled off when a strong peeling force is applied. Especially,

This Sheet Has Been Replaced



as shown in Fig. 16(A), in the case where the adhesive 21 is applied near the edge E, it can be considered that the surface protective layer is peeled off from the outer peripheral portion when the stress is concentrated on the joining parts 22 by the temperature cycling. When the bent part 23 is formed in the inner lead part 12Aa, the bent part 23 absorbs the stress occurring in the joining part 22 due to the temperature cycling. As a result, even when the adhesive 21 is applied near the edge E, the occurrence of the peeling of the surface protective layer is prevented. If the peeling occurs, a crack occurs in the resin encapsulating body 10 along the inner lead part 12Aa and outside air and water may enter the resin encapsulating body 10 through the crack. In the illustrated semiconductor device, such a matter can be avoided.

The adhesive 21 can be applied on the outermost side of the chip 11 while preventing the occurrence of the crack and an effect such that the chip 11 can be more stably held when the resin encapsulation is performed is obtained.

(embodiment 3)

Figs. 17 and 18 are diagrams showing a semiconductor device according to another embodiment of the present invention. The semiconductor device has bus bars 16. The bus bar 16 connects the inner lead parts 12Aa positioning on both ends of the chip 11 among the

This Sheet Has Been Replaced

plurality of inner lead parts 12A arranged on the long sides of the chip 11. Each of the four inner lead parts 12Aa having the bus bar 16 includes the joining part 22 and the bent part 23 at right angles with the joining part 22. The inner lead part 12Aa has a portion of a U shape in plan view made by the joining part 22 and the bent part 23. Fig. 18 is an enlarged view of one of the four inner lead parts 12Aa having the bus bar 16.

(embodiment 4)

Figs. 19 and 20 are diagrams showing a semiconductor device according to further another embodiment. In a manner similar to the case shown in Fig. 17, the semiconductor device has the bus bar 16. In this case, the joining part 22 is formed at a right angle with the inner lead part 12Aa. A part of the inner lead 12Aa, to which the joining part 22 is connected, serves as the bent part 23. The joining part 22 and a part continued from the joining part 22 form a U-shape in plan view.

As shown in Figs. 17 to 20, with respect to the semiconductor device of a type having the bus bar 16, although the example in which the step 24 is formed in the inner lead part 12Aa is shown, the contact with the remnants can be also avoided without forming the step 24 by applying the adhesive 21 thickly as shown in Fig.4(C). In case of using the bus bar 16, the bus bar 16 may also have the joining parts 22.

This Sheet Has Been Replaced

(embodiment 5)

Fig. 21 is a diagram showing a semiconductor device according to another embodiment of the present invention. In this case, each of the four inner lead parts 12Aa positioning on both ends of the chip 11 has the joining part 22 but does not have the bent part. The semiconductor device of this type is effective when a distortion in the adhesive 21 caused by the concentration of the stress by the temperature cycling can be ignored. Although the four inner lead parts 12Aa on the outermost sides have the joining parts 22, four inner lead parts 12Ab on the inner sides of them may have joining parts, respectively.

(embodiment 6)

Fig. 22 is a diagram showing a semiconductor device according to further another embodiment of the present invention. In this case, although the joining parts 22 shown in Fig. 21 are orientated in the width direction of the chip 11, the joining parts 22 are oriented in the longitudinal direction and the tips of the inner lead parts 12Aa are arranged so as to be over the edge SE of the chip 11. In this case, an effect similar to the case shown in Fig. 21 can be obtained.

(embodiment 7)

Fig. 23 is a diagram showing a semiconductor device as another embodiment of the present invention. In this case, the inner lead parts 12Aa of the leads 12 are

This Sheet Has Been Replaced

electrically directly connected to the Au bump electrodes 15a formed on the circuit formation face 14 of the chip 11 without using wires. The position of the bump electrode 15a and the position in which the adhesive 21 is applied are deviated. The other leads 12Ab and 12Ac are connected to the Au bump electrodes and the adhesive 21 is not applied.

(embodiment 8)

Figs. 24(A) and 24(B) are diagrams of semiconductor devices according to further other embodiments of the present invention. Fig. 24(A) shows a semiconductor device having a laminated type memory module structure obtained by laminating two TSOPs and soldering the outer lead parts 12B to electrodes 18 on a printed wiring board 17.

Each of the TSOPs of Fig. 24(A) is the same as the one shown in Figs. 2 and 3. The inclined part of the outer lead parts 12B of the upper TSOP is longer than that of the lower TSOP. In order to mount the TSOPs on the printed wiring board 17, solder plating is preliminarily performed to the outer lead parts 12B, solder paste is preliminarily printed on the surface of the electrodes 18, and the outer lead parts 12B are temporarily joined to the electrodes 18 by the adhesion of the solder paste. The temporary attachment may be also performed by melting the surface plating of solder of the outer lead part 12B by preliminary heating after

This Sheet Has Been Replaced

positioning the outer lead part 12B on the electrode 18. By reflowing the solder plating after the temporary attachment, the mounting operation is completed. In case of mounting one TSOP on the printed wiring board 17, a similar procedure is used.

Fig. 24(B) shows a semiconductor device of a laminated type having a memory module structure in which two TSOJ-type semiconductor devices are laminated and are arranged on the printed wiring board 17. The lower TSOJ is mounted by joining the outer leads 12B to the printed wiring board 17 in a manner similar to the case shown in Fig. 24(A). The upper TSOJ is mounted by connecting the outer leads 12B to the outer leads 12B of the lower TSOJ.

Although the invention made by the inventors of the present invention has been specifically described above on the basis of the embodiments, it is obviously understood that the present invention is not limited to the foregoing embodiments but can be variously changed within the scope not departing from the gist.

For example, the shape of the outer lead 12B is not limited to the illustrated TSOP and TSOJ types. The present invention can be applied to semiconductor devices of other types such as TQFP as long as the inner lead parts are arranged on the circuit formation face. In this case, inner leads are joined at four corners of the square chip. The present invention can be applied

This Sheet Has Been Replaced

not only to the package in which the memory LSI is encapsulated but also to a package in which a microcomputer and a logic LSI are encapsulated and a laminate type multichip module using such a package. By forming a light reflecting layer such as aluminium foil on the surface of the encapsulating body 10, also in the case where the encapsulating body 10 is very thinly formed, deterioration in characteristic such as data retention caused by light can be prevented.

Effects obtained by representative inventions among the present inventions disclosed in the application will be briefly described as follows.

Since the inner lead parts positioning on the outermost sides among the inner lead parts arranged on the circuit formation face of the chip have the joining parts and the joining parts are bonded to the chip, the portion in which the adhesive is applied is reduced and the semiconductor device can be promptly manufactured in a short time and the manufacturing efficiency is improved.

Since only the inner lead parts positioning on both ends among the inner lead parts are bonded, the chip is prevented from being deviated from the lead frame upon formation of the resin encapsulating body, so that the high-quality semiconductor device can be obtained while improving the manufacturing efficiency.

Since each of the inner lead parts bonded to the

This Sheet Has Been Replaced

chip has the bent part for absorbing the stress at the time of the temperature cycling, the breakage of the inner lead parts bonded to the chip can be prevented. Consequently, the high-quality semiconductor device having excellent durability can be obtained.

Since the stress is prevented from concentrating on the joining part by forming the bent part, the surface protective layer of the circuit formation face is prevented from being peeled off by the stress occurring in the joining parts and occurrence of a crack in the resin encapsulating body due to the peeling can be prevented, so that the semiconductor device having excellent durability can be obtained.

A gap is formed between a part, corresponding to the outer peripheral edge of the chip, of the inner lead bonded to the chip with the adhesive and the circuit formation surface. The gap is larger than the height of the remnant that may occur at the edge part. Even when the inner leads are bonded with the adhesive, the contact between the remnants and the inner leads is, therefore, avoided.

This Sheet Has Been Replaced

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor chip having a plurality of semiconductor elements and a plurality of bonding pads on its main face;

a first lead and a second lead each having an inner lead and an outer lead, a part of the inner lead of each of said first and second leads being arranged on the main face of said semiconductor chip;

wires for connecting the inner leads of said first and second leads and said plurality of corresponding bonding pads; and

a resin encapsulating body for encapsulating said semiconductor chip, the inner leads of said first and second leads, and said wires,

wherein said first lead is joined on the main face of said semiconductor chip with an adhesive interposed therebetween and

said second lead is not joined on the main face of said semiconductor chip with an adhesive.

2. A semiconductor device according to claim 1, wherein the inner lead of said first lead has a first part joined to the main face of said semiconductor chip with said adhesive and a second part arranged above the main face of said semiconductor chip in a position higher than said first portion, and the inner lead of said second lead is arranged in a position at almost the same height

This Sheet Has Been Replaced

* C L M S *

as that of the second part of the inner lead of said first lead.

3. A semiconductor device comprising:

a rectangular semiconductor chip having a plurality of semiconductor elements and a plurality of bonding pads on its main face, said plurality of bonding pads being arranged in the direction of the long sides of said semiconductor chip;

a plurality of leads each having an inner lead and an outer lead, a part of the inner lead of each of said plurality of leads being arranged on the main face of said semiconductor chip and said plurality of leads being arranged at predetermined intervals in said long-side direction;

wires for connecting the inner leads of said plurality of leads and said plurality of corresponding bonding pads; and

a resin encapsulating body for encapsulating said semiconductor chip, the inner leads of said plurality of leads, and said wires,

wherein a pair of first leads arranged on the outermost sides on the main face of said semiconductor chip among said plurality of leads are joined to the main face of said semiconductor chip with an adhesive interposed therebetween,

and wherein second leads arranged between said pair of first leads among said plurality of leads are

This Sheet Has Been Replaced

* C L M S *

not joined to the main face of said semiconductor chip with an adhesive.

4. A semiconductor device according to claim 3, wherein the inner lead of said first lead has a first part joined to the main face of said semiconductor chip with said adhesive and a second part arranged above the main face of said semiconductor chip in a position higher than said first portion, and the inner lead of said second lead is arranged at almost the same height as that of the second part of the inner lead of said first lead.

5. A semiconductor device according to claim 3, wherein there are provided four of said first leads which are arranged near the four corners of said semiconductor chip.

6. A method of manufacturing a semiconductor device, comprising the steps of:

a) preparing a semiconductor chip having a plurality of semiconductor elements and a plurality of bonding pads on its main face and a lead frame having a first lead and a second lead each including an inner lead and an outer lead;

b) arranging said lead frame on the main face of said semiconductor chip so that a part of each of the inner leads of said first and second leads is arranged on the main face of said semiconductor chip;

c) fixing the inner lead of said first lead to the main face of said semiconductor chip with an adhesive

This Sheet Has Been Replaced

* C L M S *

and arranging the inner lead of said second lead so as to have a gap from the main face of said semiconductor chip;

d) connecting the inner leads of said first and second leads to said plurality of corresponding bonding pads with wires; and

e) encapsulating said semiconductor chip, the inner leads of said first and second leads, and said wires with a resin.

7. A method according to claim 6, wherein the step a) includes a step of selectively applying an adhesive only to the inner lead of said first lead.

8. A method according to claim 7, wherein said resin is injected between the inner lead of said second lead and the main face of said semiconductor chip.

9. A method of manufacturing a semiconductor device, comprising the steps of:

preparing a lead frame having a plurality of inner lead parts and a plurality of outer lead parts which are continuous to the inner lead parts;

preparing a square-shaped semiconductor chip having a main face on which a semiconductor integrated circuit and a plurality of bonding pads are formed;

applying an adhesive to the inner lead parts at the positions corresponding to both ends of said semiconductor chip among said inner lead parts;

joining said semiconductor chip to said lead frame

This Sheet Has Been Replaced

* C L M S *

with said adhesive;

electrically connecting the bonding pads arranged on the main face of said semiconductor chip and said inner leads with wires; and

forming a resin encapsulating body by arranging said lead frame to which said semiconductor chip is joined in a resin molding die, and after that, injecting an encapsulating resin into said resin molding die.

10. A method of manufacturing a semiconductor device, comprising the steps of:

preparing a lead frame having a plurality of inner lead parts and a plurality of outer lead parts continuous to the inner lead parts, respectively;

preparing a square-shaped semiconductor chip having a main face on which a semiconductor integrated circuit and a plurality of bonding pads are formed;

applying an adhesive to the inner lead parts arranged near the four corners of the main face of said semiconductor chip;

joining said lead frame and the main face of said semiconductor chip with said adhesive;

electrically connecting the bonding pads arranged on the main face of said semiconductor chip and said inner lead parts with wires; and

forming a resin encapsulating body by arranging said lead frame to which said semiconductor chip is joined in a resin molding die, and after that, injecting an

This Sheet Has Been Replaced

* C L M S *

encapsulating resin into said resin molding die.

This Sheet Has Been Replaced

* C L M S *