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Description

INTEGRATED SEMICONDUCTOR CIRCUIT COMPRISING A
TRANSISTOR AND A STRIP CONDUCTOR

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The invention relates to an integrated semiconductor circuit comprising a transistor and an interconnect.

10 Semiconductor circuits are implemented, for example, as CMOS (complementary metal oxide semiconductor) circuits and have transistors produced in MOS technology which form inversion channels of electrons or holes underneath an interconnect. In this arrangement, two source/drain electrodes are formed opposite one another

15 on both sides of an interconnect as implantation areas in a semiconductor substrate. The interconnect is used as gate electrode in the area of the transistor and controls the formation or prevention of an inversion channel by means of its electrical potential. The

20 inversion channel extends closely underneath the semiconductor surface in the semiconductor substrate, to be precise underneath a gate oxide layer between the facing sides of the two source/drain electrodes of the transistor. The width of the channel in this case

25 extends over the width of both source/drain areas along the direction of the extent of the interconnect. Usually, both the length of the channel and the width of the channel in each case correspond to the optical limit of resolution F which can be achieved with the

30 lithographic exposure device used in each case.

The transistor described above can be used, in particular, as storage transistor in nonvolatile semiconductor memories. In this case, it has between

35 the interconnect and the semiconductor substrate a charge-storing layer which spatially binds electrical charges which are scattered into this layer during the

formation of an inversion channel and, as a result, can store digital information. In such storage circuits, there is a requirement for techniques which reduce the storage density, i.e. the number of storable
5 information items per unit of substrate area. The object of miniaturizing electrical circuits also presents itself in the case of logic circuits.

It is the object of the present invention to provide a
10 semiconductor circuit which exhibits a larger number of electrical components per substrate base area without reducing the optical limit of resolution. In particular, the number of inversion channels which can be formed in a semiconductor substrate is to be
15 increased by a factor of up to two, the substrate base area remaining the same.

According to the invention, this object is achieved by an integrated semiconductor circuit according to
20 claim 1 comprising a transistor (10) and an interconnect (11),

- the transistor (10) exhibiting a first (1) and a second source/drain electrode (2) which are arranged in a semiconductor substrate (20), and a gate electrode
25 (7),

- the interconnect (11) being electrically insulated from the semiconductor substrate (20) at least by a gate dielectric (14) and forming the gate electrode (7) in the area of the transistor (10),

30 - the interconnect (11) extending along a first direction (x) in the area of the transistor (10),

- the second source/drain electrode (2) being arranged offset with respect to the first source/drain electrode (1) in the first direction (x), and

35 - the transistor (10) exhibiting between the gate electrode (7) and the semiconductor substrate (20) a charge-storing layer (13) in which electrical charges (Q1, Q2) are locally bound.

According to the invention, a semiconductor circuit is proposed which exhibits a transistor, preferably in MOS construction, comprising two source/drain electrodes mutually offset in the direction of the extent of the interconnect, the interconnect, in the area of the transistor, forming its gate electrode. Conventional semiconductor transistors have two source/drain electrodes, both of which adjoin the same or largely identical interconnect sections so that the inversion channel essentially extends over the entire width of the two source/drain electrodes between them. The inversion channel thus has a width which corresponds to the optical limit of resolution.

In contrast, according to the invention, the first and the second source/drain electrode are mutually offset in the direction of the extent of the interconnect so that the inversion channel no longer takes up the entire width of both source/drain electrodes measured in the direction of the extent of the interconnect but only extends between mutually nearest adjacent corner areas of the first and the second source/drain electrode. Due to the lateral offset of the second source/drain electrode with respect to the first one, the shortest possible connection between the two electrodes is, for example, the line joining a right-hand corner area of the first electrode facing the second electrode and a left-hand corner area of the second electrode facing the first electrode; an inversion channel will no longer reach the edge areas of the source/drain electrodes adjoining these corner areas over the entire length of these edge areas but will essentially only short circuit the corner areas facing one another. Since such an inversion channel between the electrodes offset with respect to one another according to the invention takes up a much smaller substrate base area, the potential for saving

area on the semiconductor substrate is increased.

The inversion channel is essentially formed along the line joining the two mutually nearest adjacent corner areas of the source/drain electrodes. The other two corner areas adjoining the interconnect base area can be used for forming further inversion channels to other electrodes. Since the rectangular or square base area of a source/drain electrode has four corners, the density of transistors can be increased by a factor of up to two.

According to the invention, the transistor exhibits between the gate electrode and the semiconductor substrate a charge-storing layer in which electrical charges are locally bound. Such a transistor is suitable as storage transistor for non-volatile semiconductor memories; by scattering in highly energetic charge carriers from an inversion channel, locally bound charge states are created in the charge-storing layer above the first and/or to the second source/drain electrode. This storage mechanism is utilized with mirror bit technology. The storage density which can be created by this means can be doubled with the aid of the present invention since charges are now only stored at corner areas instead of edge areas of the source/drain electrodes in the charge-storing layer.

It is preferably provided that the second source/drain electrode is arranged offset with respect to the first source/drain electrode by a distance corresponding to the width of the first source/drain electrode along the first direction. The first and the second source/drain electrode thus adjoin two different successive sections of the interconnect; the second source/drain electrode begins on the first side of the interconnect where the first source/drain electrode ends on the second side of

the interconnect. Due to this offset, a number of source/drain electrodes can be alternately lined up on both sides of the interconnect. Between different inversion channels underneath the interconnect, a distance corresponding approximately to the optical limit of resolution exists in the direction of the extent of the interconnect.

It is preferably provided that the first and the second source/drain electrode have a rectangular base area in the semiconductor substrate and that, in the switched-on state, the transistor forms an inversion channel which extends only between a single corner area of the first source/drain electrode facing the second source/drain electrode and a single corner area of the second source/drain electrode facing the first source/drain electrode. Thus, two corner areas of the second source/drain electrode adjoining the interconnect in the direction and in the opposite direction of the extent of the interconnect can be used for forming one inversion channel each. In particular, the transistor forms an inversion channel which is narrower than half of the width of the first or of the second source/drain electrode measured in the direction of the extent of the interconnect.

Accordingly, it is provided that the transistor stores electrical charges in the charge-storing layer exclusively at the corner area of the first source/drain electrode facing the second source/drain electrode and/or at the corner area of the second source/drain electrode facing the first source/drain electrode. The storage of electrical charges exclusively at corner areas of source/drain electrodes is achieved by the fact that an electrical insulation layer between the semiconductor substrate and the charge-storing layer has a layer thickness which is of such a magnitude that the electrical insulation layer

can be tunneled through by electrical charges of an inversion channel only at corner areas of the source/drain electrodes.

- 5 A further development provides that the first and the second source/drain electrode can be optionally electrically biased positively or negatively with respect to one another. Between the electrodes, an inversion channel can then flow in both directions and, with a sufficiently high source-drain voltage, store in each case a digital information item at the corner area of the first or second electrode.

It is preferably provided that a third source/drain electrode is provided which is arranged on the same side of the interconnect as the first source/drain electrode and which is arranged offset with respect to the second source/drain electrode in the first direction. As a result, an inversion channel can be formed between a corner area of the second source/drain electrode facing the third source/drain electrode and a corner area of the third source/drain electrode facing the second source/drain electrode. The first and the third source/drain electrode are arranged on the side of the interconnect opposite to the second source/drain electrode and are arranged offset in mutually opposite directions relative to the second source/drain electrode, i.e. in the direction and in the opposite direction of the extent of the interconnect in the area of the second source/drain electrode. Thus, an inversion channel extending to the second source/drain electrode, and thus a separate transistor, can be formed between in each case one of the first and third source/drain electrodes. The inversion channels of both transistors in each case extend to different corner areas, adjacent to the interconnect, of the second source/drain electrode. The first and the third source/drain electrode are preferably at a distance

from one another which corresponds to the width of the second source/drain electrode in the direction of the extent of the interconnect, i.e. along the first direction.

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Preferably, a fourth source/drain electrode is provided which is arranged on the same side of the interconnect as the second source/drain electrode and is arranged offset with respect to the third source/drain electrode in the first direction. Thus, a further inversion channel can be formed between a corner area of the third source/drain electrode facing the fourth source/drain electrode and a corner area of the fourth source/drain electrode facing the third source/drain electrode. In this manner, both corner areas, adjacent to the interconnect, of the third source/drain electrode can be utilized for forming one transistor each analogously to the aforementioned embodiment. Analogously, further source/drain electrodes can be alternately lined up along the interconnect on both sides of it, as a result of which a particularly dense arrangement of transistors, particularly storage transistors, is produced.

25 It is preferably provided that the charge-storing layer is a nitride layer which is surrounded by electrical insulation layers on both sides. In particular, one oxide layer each can be provided on and underneath the nitride layer, the lower oxide layer simultaneously being used as gate dielectric.

A further development of the invention provides that the semiconductor circuit exhibits adjacently to the second source/drain electrode a further interconnect extending in parallel with the interconnect and a fifth source/drain electrode, the fifth source/drain electrode being arranged on the side of the further interconnect opposite to the second source/drain

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electrode and being arranged offset with respect to the second source/drain electrode in the first direction. As a result, a further inversion channel can be formed between a corner area of the second source/drain electrode facing the fifth source/drain electrode and a corner area of the fifth source/drain electrode facing the second source/drain electrode. Thus, those corner areas of the second source/drain electrode facing away from the first interconnect and being adjacent to a further second interconnect are also used for forming transistors. With the aid of additional interconnects and transistors formed on them, dense two-dimensional logic or storage circuits can be implemented.

It is preferably provided that a sixth source/drain electrode is provided which is faced by a corner area of the second source/drain electrode. With the aid of the first, the third, the fifth and the sixth source/drain electrode, up to four inversion channels can be formed which extend to in each case different corner areas of the second source/drain electrode. Whereas a maximum of two inversion channels can extend to one and the same source/drain electrode in conventional semiconductor circuits, up to 50% of the previously needed substrate surface is saved in accordance with the invention.

The semiconductor circuit is preferably a non-volatile memory circuit in which one digital information item each can be stored at each corner area of the second source/drain electrode. When mirror bit technology is used, one further digital information item each can be additionally stored at a corner area of a source/drain electrode adjacent to the second source/drain electrode by each of the inversion channels extending to the second source/drain electrode.

As an alternative, the semiconductor circuit can be a

logical part-circuit in which the first, the second and the fifth source/drain electrode and the two interconnects form two series-connected logic transistors.

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More complicated logic circuits can also be implemented with the aid of a two-dimensional network from transistors formed on interconnects.

10 In the text which follows, the invention will be described with reference to figures 1 to 10, in which:

figure 1 shows a cross-sectional view of a semiconductor circuit according to the invention
15 comprising one transistor,

figure 2 shows a top view of the semiconductor circuit from figure 1,

20 figures 3 and 4 show various alternatives of an electrical contact arrangement of the semiconductor circuit from figure 1,

figures 5 and 6 show further embodiments of the present
25 invention comprising a number of source/drain electrodes,

figures 7 and 8 show schematic views of a conventional semiconductor circuit and a semiconductor circuit
30 according to the invention, and

figures 9 and 10 show circuit diagrams of special logic circuits which in each case can be implemented by a conventional semiconductor circuit or a semiconductor
35 circuit according to the invention.

Figure 1 shows a transistor 10 comprising a first 1 and a second source/drain electrode 2 which are formed in a

semiconductor substrate 20. Between the two electrodes 1, 2, there is above the semiconductor substrate 20 an interconnect 11 which forms the gate electrode 7 in the area of the transistor 10. Between the interconnect 11 and the semiconductor substrate 20, a lower oxide layer 14 which, at the same time, forms the gate dielectric of the transistor, a charge-storing layer 13 and an upper oxide layer 15 are arranged. The charge-storing layer 13 spatially binds charges Q1, Q2 which are scattered into the charge-storing layer through the gate oxide layer 14, as a result of which digital information items can be stored as locally bound charge quantities Q1, Q2.

As shown in a top view in figure 2, the first and the second source/drain electrode 1, 2 are mutually offset in the direction of the extent of the interconnect 11, i.e. the first direction x. In the direction x, the base area G of the first electrode 1 has a width d. In a conventional transistor, the second electrode 2 would also be arranged along the interconnect section d of the interconnect 11. According to the invention, in contrast, the second electrode 2 is offset with respect to the first one in the direction x, preferably precisely by the distance d. As a result, the transistor channel K1 is not completely formed between the facing edge areas of the electrodes 1, 2 but only between a corner area 1a of the first electrode and a corner area 2a of the second electrode 2. The channel K1 formed between these mutually facing corner areas 1a, 2a is thus narrower than a conventional transistor channel and requires less substrate base area.

Figure 3 shows a possible circuit for a transistor according to the invention in nMOS construction (metal oxide semiconductor) in which the inversion channel K1 consisting of electrons flows from the first source/drain electrode 1 to the second source/drain

electrode 2 which is biased with a positive electrical potential $+V$ with respect to the first electrode 1 which, for example, is connected to ground 0. As a result, the electrons of the inversion channel K1 are
5 accelerated in the direction of the arrow shown and due to scattering, pass through the gate oxide layer into the charge-storing layer where they are spatially bound and form the charge quantity Q2. As shown in figure 3, the charge quantity Q2 is located in the charge-storing
10 layer adjacently to the corner area 2a of the second source/drain electrode 2.

In the circuit, shown in figure 4, of the nMOS transistor from figure 3, the first source/drain
15 electrode 1 is biased with a positive potential $+V$ with respect to the second 2, so that the electrons are accelerated in the direction of the first electrode 1 and are stored as charge quantity Q1 in the area of the corner area 1a of the first electrode 1 due to
20 scattering into the charge-storing layer. Depending on the direction of the current of the transistor channel, one charge each can thus be stored at a corner area 1a, 2a of the first or second source/drain electrode 1, 2. Only two corner areas 1a, 2a are involved in the
25 inversion channel.

As shown in figure 5, further inversion channels K2, K3 can be formed on the interconnect 11 with a third 3 and a fourth source/drain electrode 4. The electrodes are
30 alternately arranged offset with respect to one another on both sides of the interconnect 11. According to figure 5, an inversion channel K2 is formed between a corner area 2b of the second electrode which faces the third source/drain electrode 3, and its corner area 3a.
35 Analogously, a further inversion channel K3 extends between corner areas 3b, 4a of the third and of the fourth source/drain electrodes 3, 4. Further source/drain electrodes can be arranged on the

interconnect 11 and a further transistor channel can be formed per source/drain electrode.

Further corner areas of this source/drain electrode which face away from the interconnect 11 can also be used for forming further transistors. Thus, figure 6 shows, apart from the interconnect 11, a further interconnect 16 between which the second source/drain electrode 2 is located. The further interconnect 16 is formed in the same manner as the interconnect 11 and adjoins the second 2, the fourth 4 and a fifth 5 and a sixth source/drain electrode 6, these four source/drain electrodes also being arranged offset with respect to one another and in alternate sequence to the left and to the right of the further interconnect 16. As a result, two further inversion channels K5, K6 coming from the second source/drain electrode can be formed which extend between a corner area 2c of the second electrode 2 and a corner area 5a of the fifth source/drain electrode 5 and between a corner area 2d of the second electrode and a corner area 6a of the sixth source/drain electrode. With these, two further digital information items can be stored by charge quantities Q5, Q6 scattered into a corresponding charge-storing layer under the further interconnect 16 at the corner areas 2c, 2d. All transistors of the semiconductor circuit according to the invention, shown or indicated in the figures, can also be formed without a charge-storing layer, for example only with a gate dielectric 14 between the gate electrode 7 and the semiconductor substrate 20, in which case they can be used as logic transistors or as transistors for any other circuits. In this case, the indicated charge quantities Q1 to Q6 are omitted.

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Figure 7 shows a schematic top view of a conventional semiconductor circuit which can be, for example, a logic part-circuit. Three interconnects G1, G2, G3 are

shown which are used as gate electrodes. Between the interconnects, source/drain areas 1, 2, 5, 7 are shown which are arranged in two rows between the interconnects G1, G2, G3. In the conventional semiconductor circuit of figure 7, these source/drain electrodes are not offset with respect to one another. Q denotes charge quantities indicated in circles which are arranged in the charge-storing layer along the entire edges of the source/drain areas. Accordingly, an inversion channel takes up the entire width of a source/drain area along the extent of, for example, the interconnect G2. The semiconductor circuit illustrated in figure 7 represents a part-circuit of an NAND gate in which three transistors are connected in series in the direction of the arrow extending vertically. A current can only flow through this series circuit of three transistors if a gate voltage is applied in each of the transistors such as shown, for example, for the center transistor with the gate electrode G2 by means of the horizontal arrow.

Figure 8 shows a semiconductor circuit according to the invention by means of which the part-circuit of figure 7 can be realized with source/drain electrodes mutually offset in the direction of interconnects. Also shown are three interconnects G1, G2, G3 and a number of source/drain electrodes 1, 2, 3, 4, 5, 6, 7 of which, for example, the first, second, fifth and seventh source/drain electrode can be connected to form three series-connected transistors as indicated by the diagonal arrow. In particular, the first and the second source/drain electrode 1, 2, together with the interconnect G1, form a first transistor T, and the second and the fifth source/drain electrode 2, 5, together with the second interconnect G2, form a second transistor T'. The circuit operates in the same manner as in figure 7 but can be arranged much more densely together with other circuit elements. In particular,

figure 8 shows possible starting and end points of further inversion channels which are indicated by circles at the corner areas of the source/drain electrodes. As indicated by comparison with figure 7, these starting and end areas of the inversion channels are packed much more densely.

The circuits shown in figures 7 and 8 represent part-circuits of a NAND gate. Figures 9 and 10 show the complete circuit diagram of such a circuit. In each case, three n-channel transistors N connected to common gate electrodes G1, G2 and G3 and further p-channel transistors P are shown, the part-circuit S corresponding to that of the in each case three transistors in figures 7, 8. The three n-channel transistors N are connected in series and are connected to a signal output A. If only one of these three transistors does not conduct, the corresponding p-channel transistor connected to the same gate line is conducting and connects the potential of the signal output A to the operating voltage Vdd. If all three n-channel transistors are conducting, the signal output A is grounded. The circuit shown in figure 10, in which the signal output A is first connected to the operating voltage via a p-channel transistor P and only then, with the transistor P switched off, are possible gate voltages applied to the gate lines G1, G2 and G3 in order to subsequently ground the signal output A if required, has the same switching character.

Using the present invention, any other logical part-circuit can be produced. The advantage of densely packed inversion channels can be utilized, in particular, in storage circuits in which information items are stored in a charge-storing layer of the transistor or in another structure.

CLAIMS

1. An integrated semiconductor circuit comprising a transistor (10) and an interconnect (11),
 - 5 - the transistor (10) exhibiting a first (1) and a second source/drain electrode (2) which are arranged in a semiconductor substrate (20), and a gate electrode (7),
 - the interconnect (11) being electrically insulated
10 from the semiconductor substrate (20) at least by a gate dielectric (14) and forming the gate electrode (7) in the area of the transistor (10),
 - the interconnect (11) extending along a first direction (x) in the area of the transistor (10),
 - 15 - the second source/drain electrode (2) being arranged offset with respect to the first source/drain electrode (1) in the first direction (x), and
 - the transistor (10) exhibiting between the gate
20 electrode (7) and the semiconductor substrate (20) a charge-storing layer (13) in which electrical charges (Q1, Q2) are locally bound.
2. The semiconductor circuit as claimed in claim 1,
25 characterized in that the second source/drain electrode (2) is arranged offset with respect to the first source/drain electrode (1) by a distance (d) corresponding to the width of the first source/drain electrode (1) along the first
30 direction (x).
3. The semiconductor circuit as claimed in claim 1 or 2, characterized in that the first (1) and the second source/drain electrode (2) have a
35 rectangular base area (G) in the semiconductor substrate (20) and in that the transistor (10) forms an inversion channel (K1) which only extends

between a corner area (1a) of the first source/drain electrode (1) facing the second source/drain electrode (2) and a corner area (2a) of the second source/drain electrode (2) facing the first source/drain electrode (1).

4. The semiconductor circuit as claimed in one of claims 1 to 3, characterized in that the transistor (10) stores electrical charges (Q1; Q2) in the charge-storing layer (13) exclusively at the corner area (1a) of the first source/drain electrode (1) facing the second source/drain electrode (2) and/or at the corner area (2a) of the second source/drain electrode (2) facing the first source/drain electrode (1).

5. The semiconductor circuit as claimed in one of claims 1 to 4, characterized in that the first (1) and the second source/drain electrode (2) can be optionally electrically biased positively or negatively with respect to one another.

6. The semiconductor circuit as claimed in one of claims 3 to 5, characterized in that a third source/drain electrode (3) is provided which is arranged on the same side of the interconnect (11) as the first source/drain electrode (1) and which is arranged offset with respect to the second source/drain electrode (2) in the first direction (x).

7. The semiconductor circuit as claimed in claim 6, characterized in that a fourth source/drain electrode (4) is provided which is arranged on the same side of the interconnect (11) as the second source/drain electrode (2) and is arranged offset with respect to the third source/drain electrode (3) in the first direction (x).

8. The semiconductor circuit as claimed in one of claims 4 to 7, characterized in that the charge-storing layer (13) is a nitride layer which is surrounded by electrical insulation layers (14, 15) on both sides.
9. The semiconductor circuit as claimed in one of claims 1 to 8, characterized in that the semiconductor circuit exhibits adjacently to the second source/drain electrode (2) a further interconnect (16) extending in parallel with the interconnect (11) and a fifth source/drain electrode (5), the fifth source/drain electrode (5) being arranged on the side of the further interconnect (16) opposite to the second source/drain electrode (2) and being arranged offset with respect to the second source/drain electrode (2) in the first direction (x).
10. The semiconductor circuit as claimed in claim 9, characterized in that a sixth source/drain electrode (6) is provided which is faced by a corner area (2d) of the second source/drain electrode (2) so that, with the aid of the first (1), the third (3), the fifth (5) and the sixth source/drain electrode (6), up to four inversion channels (K1, K2, K5, K6) can be formed which extend to in each case different corner areas (2a, 2b, 2c, 2d) of the second source/drain electrode (2).
11. The semiconductor circuit as claimed in one of claims 1 to 10, characterized in that the semiconductor circuit is a non-volatile memory circuit in which one digital information item each (Q2, Q3, Q5, Q6) can be stored at each corner area (2a, 2b, 2c, 2d) of the second source/drain

electrode (2).

12. The semiconductor circuit as claimed in claim 9 or 10, characterized in that the semiconductor circuit is a logical part-circuit in which the first (1), the second (2) and the fifth source/drain electrode (5) and the two interconnects (11, 16) form two series-connected logic transistors (T, T').