

CLAIMS:

1. A method of forming and testing a plurality of monolithic electronic devices, the method comprising:
- 5 a) forming a monolithic electronic device array comprising:
forming a common semiconducting layer comprising a Group III-nitride on a sacrificial substrate;
forming an array of monolithic electronic devices on a surface of the common semiconducting layer on an opposite side of the common semiconducting layer to the sacrificial substrate, each monolithic electronic device of the array of monolithic electronic devices comprising a plurality of Group III-nitride layers;
- 10 forming a planarising dielectric layer over the array of monolithic electronic devices to provide a planarised dielectric surface which is generally aligned with the surface of the common semiconducting layer;
- 15 forming a grid of trenches by etching the planarising dielectric layer and the common semiconducting layer from the planarised dielectric surface through to the sacrificial substrate, wherein the grid of trenches surrounds each monolithic electronic device;
- forming first electrical contacts to each monolithic electronic device through the planarising dielectric layer,
- 20 forming a sacrificial dielectric layer over the grid of trenches and the planarised surface of the planarising dielectric layer to form a first bonding surface generally aligned with the surface of the common semiconducting layer, wherein the first bonding surface comprises first apertures aligned with each of the first electrical contacts;
- 25 b) providing a test substrate comprising:
an electronics substrate comprising electronics testing circuitry configured to supply power to each of the monolithic electronic devices of the monolithic electronic device array;
and
30 a plurality of second electrical contacts arranged on the electronics substrate to correspond to an arrangement of the first electrical contacts of the monolithic electronic device array;
- wherein a bonding dielectric layer is formed on the electronics substrate to provide a second bonding surface, the second bonding surface comprising second apertures
35 aligned with each of the second electrical contacts;

- c) aligning the second electrical contacts of the test substrate with the first electrical contacts of the monolithic electronic device array and bonding the second bonding surface of the test substrate to the first bonding surface of the sacrificial dielectric layer such that
5 the first and second electrical contacts are in electrical contact;
- d) supplying power from the test substrate to the monolithic electronic device array to test each of the monolithic electronic devices of the monolithic electronic device array via the plurality of first and second electrical contacts; and
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- e) selectively removing first portions of the sacrificial substrate through a thickness of the sacrificial substrate to separate each of the monolithic electronic devices; and removing the sacrificial dielectric layer to separate each monolithic electronic device from the test substrate.
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2. A method according to claim 1, wherein the bonding dielectric layer is a sacrificial bonding dielectric layer, wherein the sacrificial bonding dielectric layer is configured to be selectively removed with the sacrificial dielectric layer to separate each monolithic electronic device from the text substrate.
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3. A method according to claim 1 or claim 2, wherein, following the removal of the sacrificial dielectric layer to separate each monolithic electronic device from the test substrate, the test substrate may be reused in a method of forming and testing a plurality of monolithic devices.
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4. A method according to any preceding claim, wherein the electronics testing circuitry of the test substrate is configured to supply power to each of the monolithic electronic devices in parallel.
- 30 5. A method according to any preceding claim, wherein each monolithic electronic device of the monolithic electronic device array comprises a light emitting diode (LED).
6. A method according to any preceding claim, wherein

each monolithic electronic device is a monolithic light emitting diode (LED) pixel comprising a plurality of LED subpixels on the surface of the common semiconducting layer, each LED subpixel comprising a stack of Group III-nitride layers.

- 5 7. A method according to claim 6, wherein, following bonding of the test substrate the monolithic electronic device array, the method comprises:
- forming light extraction features for each of the monolithic LED pixels comprising: selectively removing second portions of the sacrificial substrate aligned with each of the LED subpixels.
- 10 8. A method according to claim 7, wherein
- forming light extraction features for each of the monolithic LED pixels comprises: selectively removing second portions of the sacrificial substrate aligned with each of the LED subpixels to form a container volume for each LED subpixel; and
- 15 providing a first colour converting layer in at least one of the container volumes of each monolithic LED pixel, the first colour converting layer configured to absorb light of a first wavelength and emit converted light of a first converted light wavelength longer than the first wavelength.
- 20 9. A method according to claim 8, wherein
- the first converted light wavelength is at least 500 nm and/or no greater than 650 nm.
10. A method according to claim 8 or claim 9, wherein
- 25 a second colour converting layer is provided in in at least one other of the container volumes of each monolithic LED pixel, the second colour converting layer configured to absorb light of a first wavelength and emit converted light of a second converted light wavelength longer than the first converted light wavelength
- 30 11. A method according to any of claims 6 to 10, wherein
- each LED subpixel is configured to generate light having a first wavelength of at least 380 nm and/or no greater than 490 nm.
12. A method according to any of claims 6 to 11, wherein

the surface area of each LED subpixel on the common semiconducting layer may define an area of no greater than 100 μm x 100 μm .

13. A monolithic device array for bonding to the test substrate of any of claims 16 to 20,
5 comprising:
a sacrificial substrate;
a common semiconducting layer comprising a Group III-nitride provided on the sacrificial substrate;
an array of monolithic electronic devices provided on a surface of the common
10 semiconducting layer on an opposite side of the common semiconducting layer to the sacrificial substrate, each monolithic electronic device of the array of monolithic electronic devices comprising a plurality of Group III-nitride layers;
a planarising dielectric layer provided on the array of monolithic electronic devices to provide a planarised dielectric surface which is aligned with the surface of the common
15 semiconducting layer, wherein
the planarising dielectric layer defines a grid of trenches extending from the planarised dielectric surface through to the sacrificial substrate, wherein the grid of trenches surrounds each monolithic electronic device;
first electrical contacts for each monolithic electronic device, the first electrical
20 contacts extending from each monolithic electronic device to the planarised dielectric surface; and
a sacrificial dielectric layer provided within the grid of trenches and over the planarised surface of the planarising dielectric layer to provide a first bonding surface generally aligned with the surface of the common semiconducting layer, wherein the first
25 bonding surface comprises first apertures aligned with each of the first electrical contacts.
14. A monolithic device array according to claim 13, wherein
each monolithic electronic device of the monolithic electronic device array comprises a light emitting diode (LED).
15. A monolithic device array according to claim 13 or 14, wherein
each monolithic electronic device is a monolithic light emitting diode (LED) pixel comprising a plurality of LED subpixels on the surface of the common semiconducting layer, each LED subpixel comprising a stack of Group III-nitride layers.

16. A test substrate for bonding to the monolithic device array of any of claims 13 to 15, comprising:
- an electronics substrate comprising electronics testing circuitry configured to supply power to each of the monolithic electronic devices of the monolithic electronic device array;
- 5 a plurality of second electrical contacts arranged on the electronics substrate to correspond to an arrangement of the first electrical contacts of the monolithic electronic device array; and
- a bonding dielectric layer is formed on the electronics substrate to provide a second bonding surface, the second bonding surface comprising second apertures aligned with
- 10 each of the second electrical contacts.
17. A test substrate according to claim 16, wherein
- the bonding dielectric layer is a sacrificial bonding dielectric layer, wherein the sacrificial bonding dielectric layer is configured to be selectively removed with the sacrificial
- 15 dielectric layer to separate each monolithic electronic device from the test substrate
18. A test substrate according to claim 17, wherein
- the sacrificial bonding dielectric layer is configured to be selectively removed such that the test substrate may be reused for bonding to a monolithic electronic device.
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19. A test substrate according to any of claims 16 to 18, further comprising:
- an etch stop layer provided between the bonding dielectric layer and the electronics substrate.
- 25 20. A test substrate according to any of claims 16 to 19, wherein
- the electronics testing circuitry of the test substrate is configured to supply power to each of the monolithic electronic devices in parallel.