CLAIMS

WHAT IS CLAIMED IS:

1. A memory system comprising:

a memory controller configured to exchange data according to a first clock, the data including one or more of read data and write data; and

a memory device including a plurality of non-volatile memories and an interface circuit connected to the memory controller and the plurality of non-volatile memories, the interface circuit configured to,

divide the first clock into a second clock based on a number of the plurality of non-volatile memories, and

exchange the data with the plurality of non-volatile memories, according to the second clock,

wherein the interface circuit comprises:

a deserializer configured to receive the write data from the memory controller, divide the first clock into the second clock based on the number of the plurality of non-volatile memories, divide the write data to generate divided write data, and to transmit the divided write data to respective ones of the plurality of non-volatile memories based on the second clock; and

a serializer configured to receive divided read data from the plurality of non-volatile memories based on the second clock, buffer the divided read data, generate the read data based on the divided read data, and transmit the read data to the memory controller based on the first clock,

wherein the serializer comprises:

a plurality of buffer registers connected to respective ones of the plurality of non-volatile memories, the plurality of buffer registers configured to buffer the divided read data received from the respective ones of the plurality of non-volatile memories; and

a combiner configured to generate the read data from the divided read data, and

wherein the interface circuit is further configured to variably determine a margin based on memory sizes of the plurality of buffer registers.

2. The memory system of claim 1, wherein the interface circuit is configured to improve an operating frequency of the memory system by dividing the write data into the

divided write data via the deserializer, and to reduce loading between the memory controller and the plurality of non-volatile memories by buffering the divided read data output from each of the plurality of non-volatile memories in the serializer.

3. The memory system of claim 1 or claim 2, wherein the interface circuit further comprises:

a time-to-digital converter (TDC) configured to,

receive data strobe signals from the plurality of non-volatile memories, and

detect a skew based on a difference between times when the data strobe signals are received from the plurality of non-volatile memories.

4. The memory system of claim 3, wherein the interface circuit is further configured to determine, based on the skew, a delay time associated with the divided read data such that the divided read data buffered in different ones of the plurality of buffer registers correspond to each other.

5. The memory system of claim 4, wherein the interface circuit is configured to determine the delay time based on the margin and a largest delay among the plurality of non-volatile memories.

6. The memory system of any one of claims 1 to 3, wherein the interface circuit is configured to determine, based on a set maximum delay, a delay time associated with the divided read data such that the divided read data buffered in different ones of the plurality of buffer registers correspond to each other.

7. The memory system of claim 6, wherein the set maximum delay corresponds to a data access time (tDQSRE) parameter.

8. The memory system of any one of claims 1 to 7,

wherein the plurality of non-volatile memories are one of NAND flash memory, vertical NAND flash memory, a vertical NAND flash based on a cell-on-peri (CoP) structure, and a vertical NAND flash memory having a stacked structure including 100 or more layers,

wherein a frequency of the first clock corresponds to a maximum operating frequency of the plurality of non-volatile memory devices, the maximum operating frequency being greater than or equal to 1 GHz, and

wherein a frequency of the second clock is 1/N times the frequency of the first clock, N being one of (i) a number of NAND flash memories or (ii) a multiple of 8 thereof, when a number of input/output structures in a single NAND flash memory is the multiple of 8.