(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 November 2004 (04.11.2004)

PCT

(10) International Publication Number
WO 2004/095247 A1

(51) International Patent Classification[7]: G06F 1/32

(21) International Application Number:
PCT/US2004/003352

(22) International Filing Date: 18 February 2004 (18.02.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/394,256 24 March 2003 (24.03.2003) US

(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Blvd., Mailstop SC4-202, Santa Clara, CA 95052-8119 (US).

(72) Inventor: **KAHN, Opher**; 16 Haarava Street, P.O.Box 2194, 30900 Zichron Yacov (IL).

(74) Agents: **EITAN PEARL LATZER & COHEN ZEDEK L.L.P.** et al.; 10 Rockefeller Plaza, Suite 1001, New York, NY 10020 (US).

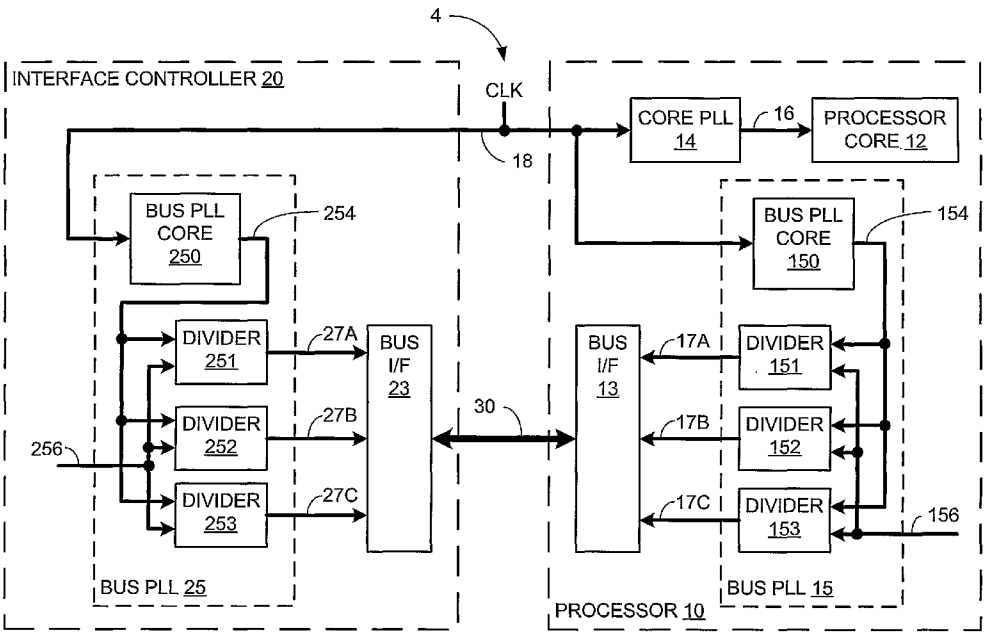
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: REDUCING CPU AND BUS POWER WHEN RUNNING IN POWER-SAVE MODES



(57) Abstract: A processing system includes a bus and a processor whose core is constrained to have one or more core clock signal frequencies no lower than a predetermined multiple of the lowest of one or more bus clock signal frequencies. In a power-save mode, the processor is able to generate one or more core clock signals at frequencies such that the lowest core clock signal frequency is lower than the predetermined multiple of the lowest of the one or more bus clock signal frequencies in performance mode. The processor is able to achieve this by generating the one or more bus clock signals so that the lowest of the bus clock signal frequencies in power-save mode is lower than the lowest of the bus clock signal frequencies in performance mode.

WO 2004/095247 A1