

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
26 April 2001 (26.04.2001)

PCT

(10) International Publication Number
WO 01/29974 A1

(51) International Patent Classification⁷: H03M 13/41

(21) International Application Number: PCT/US00/29313

(22) International Filing Date: 23 October 2000 (23.10.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/422,920 21 October 1999 (21.10.1999) US

(71) Applicant: QUALCOMM INCORPORATED [US/US];
5775 Morehouse Drive, San Diego, CA 92121-1714 (US).

(72) Inventor: HANSQUINE, David; 12885 Sundance Avenue, San Diego, CA 92129 (US).

(74) Agents: WADSWORTH, Philip, R. et al.; Qualcomm Incorporated, 5775 Morehouse Drive, San Diego, CA 92121-1714 (US).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

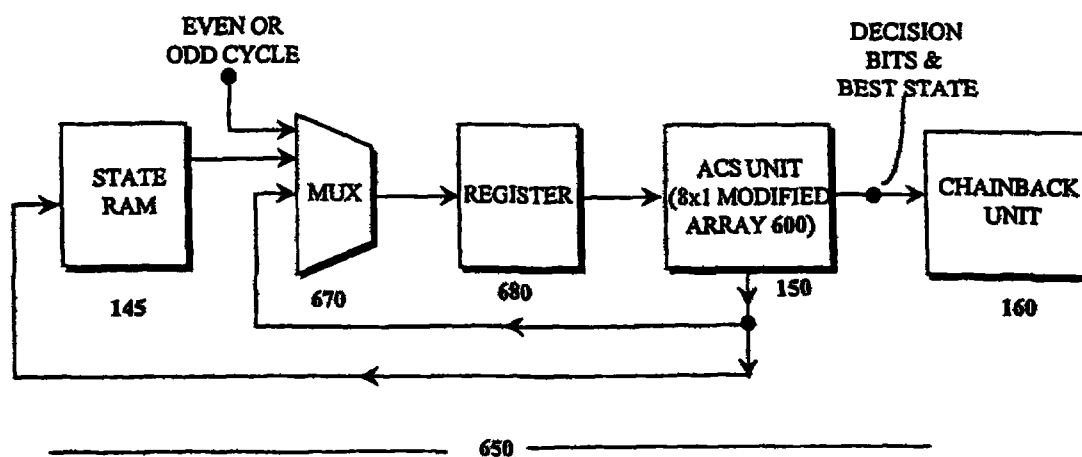
(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:

- With international search report.
- Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: HIGH-SPEED ACS UNIT FOR A VITERBI DECODER



(57) Abstract: System performing an ad-compare-select (ACS) butterfly operation in an implementation of the Viterbi algorithm. The system includes a first memory element (145) for storing a plurality of source state metrics; a multiplexer (670) which is capable of selecting between a first and second operating path based on even and odd clock cycles. ACS mechanism (600), which calculates the target state metrics for each of the source state metrics. A second memory coupled to the ACS mechanism and the multiplexer, is used to temporarily store the target metrics. The multiplexer therefore selects the first operating path during even clock cycles and supplies the source state metrics from the first memory to the ACS mechanism to generate target state metrics. During odd clock cycles, the multiplexer selects the second operating path to access the second memory and use the previously calculated target state metrics as intermediate source state metrics.