ABSTRACT

METHODS FOR GAP FILL AND PLANARIZATION OF INTERMETAL DIELECTRICS

An improved method of gap filling and planarization in the dielectric layer by combining an anti-reflective coating with a CMP etch stop is described. Semiconductor device structures are provided in and on a semiconductor substrate. A conducting layer is deposited overlying the surfaces of the semiconductor device structures. A hard mask is deposited overlying the conducting layer wherein the hard mask acts as an anti-reflective coating. The conducting layer and the hard mask are patterned to form conducting lines wherein a gap is formed between the conducting lines. A first dielectric layer is deposited over the surfaces of the conducting lines wherein the gap remains between the conducting lines. A second dielectric layer is deposited overlying the first dielectric layer wherein the gap is filled by the second dielectric layer. The first and second dielectric layers are planarized wherein the hard mask acts as an etch stop or a polish stop. A third dielectric layer is deposited over the planarized first and second dielectric layers completing the fabrication of the integrated circuit device.

(FIGURE 4 IS SUGGESTED FOR PUBLICATION)