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TITLE OF THE INVENTION

POROUS REGION REMOVING METHOD AND SEMICONDUCTOR SUBSTRATE MANUFACTURING METHOD

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to a porous region removing method and a semiconductor substrate manufacturing method and, more particularly, to a method of removing a porous region from a substrate having the porous region, a semiconductor substrate manufacturing method using this method, and an apparatus for removing a porous region.

DESCRIPTION OF THE RELATED ART

There is a method of sequentially forming a porous Si layer and a single-crystal Si layer on a first substrate, bonding the first substrate to a separately prepared second substrate, and separating the bonded substrate stack into two substrates at the porous Si layer to transfer the single-crystal Si layer formed on the first substrate side to the second substrate side, thereby manufacturing an SOI substrate.

In this method, after the bonded substrate stack is separated into two substrates, the porous Si layer remaining

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on the surface on the second substrate side is removed. In removing the porous Si layer, the planarity of the surface of the underlying second substrate and, more particularly, film thickness uniformity of the single-crystal Si layer as the surface layer of the second substrate is preferably not hindered.

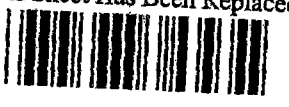
SUMMARY OF THE INVENTION

The present invention has been made in consideration of the above situation, and has as its object to provide a porous region removing method capable of maintaining a given planarity of an underlying layer and a semiconductor substrate manufacturing method using this method.

According to the present invention, there is provided a porous region removing method of removing a porous region from a substrate having the porous region, characterized by comprising the first step of processing the porous region by an etchant while supplying an ultrasonic wave to the etchant, the second step of processing the porous region by the etchant without supplying any ultrasonic wave to the etchant or while supplying an ultrasonic wave weaker than the ultrasonic wave supplied in the first step to the etchant, and the third step of removing the porous region remaining on the substrate.

In the porous region removing method, the first step

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preferably comprises filling pores in the porous region with the etchant to a deep portion.

In the porous region removing method, the second step preferably comprises thinning pore walls in the porous region to not more than a predetermined thickness by an etching function.

In the porous region removing method, the second step preferably comprises thinning the pore walls in the porous region to a thickness that allows removal of the remaining porous region at once in the third step.

In the porous region removing method, the third step preferably comprises removing the porous region remaining on the substrate by the etchant.

In the porous region removing method, the third step preferably comprises removing the porous region remaining on the substrate by the etchant while supplying the ultrasonic wave to the etchant.

In the porous region removing method, the first to third steps are preferably executed while dipping the substrate to be processed in the same etchant.

In the porous region removing method, the third step preferably comprises removing the porous region remaining on the substrate by an etchant whose etching rate for the porous region is higher than that of the first or second etchant.

In the porous region removing method, the first to third

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steps are preferably executed while completely dipping the substrate to be processed in the etchant.

In the porous region removing method, the first and/or second steps is preferably executed while completely dipping the substrate to be processed in the etchant.

In the porous region removing method, the third step preferably comprises removing the porous region remaining on the substrate by a high-pressure fluid.

In the porous region removing method, the third step preferably comprises removing the porous region remaining on the substrate by scrubbing.

In the porous region removing method, in processing the substrate while supplying the ultrasonic wave to the etchant, a relative positional relationship between an ultrasonic source and the substrate is preferably changed.

In the porous region removing method, in processing the substrate while supplying the ultrasonic wave to the etchant, the substrate is preferably swung in the etchant.

In the porous region removing method, in processing the substrate while supplying the ultrasonic wave to the etchant, the substrate is preferably rotated.

In the porous region removing method, in processing the substrate while supplying the ultrasonic wave to the etchant, a position of at least one of the substrate and the ultrasonic source is preferably changed substantially in a direction parallel or perpendicular to a vibration plane of the

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ultrasonic wave.

In the porous region removing method, in processing the substrate by the etchant, the substrate is preferably swung or rotated.

In the porous region removing method, in processing the substrate by the etchant, the etchant is preferably circulated to form a flow of etchant near the substrate.

In the porous region removing method, preferably, the first and second steps are executed while dipping the substrate in the same etching tank, the first step comprises operating the ultrasonic source, and the second step comprises stopping operation of the ultrasonic source.

In the porous region removing method, preferably, the first and second steps are executed while dipping the substrate in the same etching tank, the first and second steps comprise continuously operating the ultrasonic source, and the second step comprises inserting an ultrasonic shielding plate between the ultrasonic source and the substrate.

In the porous region removing method, the substrate to be processed preferably essentially consists of single-crystal Si.

In the porous region removing method, the porous region preferably essentially consists of porous Si.

In the porous region removing method, the porous region is preferably formed by anodizing a single-crystal Si substrate.

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In the porous region removing method, preferably, as the etchant, any one of

(a) fluoric acid,

(b) a mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to fluoric acid,

(c) buffered fluoric acid, and

(d) a mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to buffered fluoric acid

is used.

According to the present invention, there is also provided a semiconductor substrate manufacturing method characterized by comprising the steps of forming a porous layer and at least one non-porous layer on a first substrate, bonding a second substrate to the non-porous layer side of the first substrate, removing the first substrate from the bonded substrate stack to expose the porous layer on a surface of the second substrate, and removing the porous layer on the second substrate using the above porous region removing method.

In the porous region removing method, the step of exposing the porous layer preferably comprises grinding, polishing, or etching the first substrate from a lower surface side of the first substrate of the bonded substrate stack, thereby exposing the porous layer on the surface of the second substrate.

In the porous region removing method, the step of

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exposing the porous layer preferably comprises dividing the bonded substrate stack at the porous layer, thereby exposing the porous layer on the surface of the second substrate.

In the porous region removing method, the non-porous layer preferably includes a single-crystal Si layer.

In the porous region removing method, the non-porous layer preferably includes a single-crystal Si layer and an Si oxide layer.

In the porous region removing method, the single-crystal Si layer is preferably epitaxially grown on the porous layer on the first substrate.

In the porous region removing method, the non-porous layer preferably includes a single-crystal compound semiconductor layer.

In the porous region removing method, the second substrate preferably essentially consists of an Si material.

In the porous region removing method, the second substrate preferably has an Si oxide layer on a surface to be bonded to the first substrate.

In the porous region removing method, the second substrate preferably comprises a transparent substrate.

According to the present invention, there is also provided a porous region removing apparatus for removing a porous region from a substrate having the porous region, characterized by comprising means for executing the first step of processing the porous region by an etchant while

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supplying an ultrasonic wave to the etchant, means for executing the second step of processing the porous region by the etchant without supplying any ultrasonic wave to the etchant or while supplying an ultrasonic wave weaker than the ultrasonic wave supplied in the first step to the etchant, and means for executing the third step of removing the porous region remaining on the substrate.

Further objects, features and advantages of the present invention will become apparent from the following detailed description of embodiments of the present invention with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1C are views for explaining the principle of a porous layer removing method according to a preferred embodiment of the present invention;

Figs. 2A to 2C are views showing a fabrication method according to the first application example of the porous layer removing method;

Figs. 3A to 3F are views showing a semiconductor substrate manufacturing method according to another preferred embodiment of the present invention;

Fig. 4 is a perspective view showing the first arrangement of a wafer processing apparatus;

Fig. 5 is a perspective view showing the second

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arrangement of the wafer processing apparatus;

Fig. 6 is a perspective view showing the third arrangement of the wafer processing apparatus;

Fig. 7A is a view showing operation of the wafer processing apparatus shown in Fig. 6;

Fig. 7B is a view showing operation of the wafer processing apparatus shown in Fig. 6;

Fig. 7C is a view showing operation of the wafer processing apparatus shown in Fig. 6;

Fig. 7D is a view showing operation of the wafer processing apparatus shown in Fig. 6;

Fig. 7E is a view showing operation of the wafer processing apparatus shown in Fig. 6;

Fig. 8 is a perspective view of a swing assist member in the wafer processing apparatus shown in Fig. 6;

Fig. 9 is a view showing the fourth arrangement of the wafer processing apparatus;

Fig. 10 is a view showing the fifth arrangement of the wafer processing apparatus;

Figs. 11A and 11B are views showing a modification of the wafer processing apparatus shown in Fig. 5 or 6; and

Figs. 12A to 12C are views showing the seventh arrangement of the wafer processing apparatus.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

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The present invention is suitable for a method of sequentially forming a porous layer and a non-porous layer on a first substrate, bonding the first substrate to a separately prepared second substrate, separating the bonded substrate stack into two substrates at the porous layer to transfer the non-porous layer formed on the first substrate side to the second substrate side, and removing the porous layer remaining on the surface on the second substrate side, thereby manufacturing an SOI substrate.

As the first substrate, a single-crystal Si substrate can be used. In this case, the porous layer is a porous Si layer. On the porous Si layer, a single-crystal Si layer can be epitaxially grown as a non-porous layer. An insulating layer such as an SiO_2 layer may be formed on the single-crystal Si layer.

In the embodiment, the first substrate on which the porous Si layer and the non-porous layer are sequentially formed is bonded to the separately prepared second substrate to form a bonded substrate stack. After the bonded substrate stack is separated into two substrates at the porous Si layer, the porous Si layer remaining on the second substrate side is removed by, e.g., wet etching.

In etching the porous Si layer, break of the porous Si layer can be prompted by supplying an ultrasonic wave to the etching tank. More specifically, when an ultrasonic wave is supplied into the etching tank, and more specifically, to

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the bonded substrate stack during etching, pore walls in the porous Si layer can be broken before they become thin. Since the time from the start to the end of break of pore walls in the porous Si layer can be greatly shortened, the etching selectivity ratio between the porous layer and the underlying second substrate (e.g., a single-crystal Si substrate) can be increased. Hence, SOI thickness variations in surface of the second substrate and SOI thickness variations between the substrates after removal of the porous layer are suppressed, and a high-quality SOI substrate having a single-crystal Si layer with high film thickness uniformity can be obtained.

However, if the porous layer on the substrate to be etched has variations in thickness, it may be difficult to ensure high film thickness uniformity of the surface layer (single-crystal Si layer) of the second substrate after removal of the porous Si layer. Especially in mass production, this problem may result in a low yield.

In this embodiment, a method of more properly ensuring high film thickness uniformity of the surface layer (single-crystal Si layer) of the second substrate after removal of the porous Si layer is provided.

Figs. 1A to 1C are views for explaining the principle of a porous layer removing method according to a preferred embodiment of the present invention. Referring to Figs. 1A to 1C, reference numeral 201 denotes an underlying substrate

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(second substrate); 202, a porous layer; and 203, an etchant.

In Fig. 1A, the pores of the porous layer 202 are filled with the etchant 203 to the deepest portions. At this time, an ultrasonic wave is preferably supplied to the object (e.g., a bonded substrate stack) to be processed. When an ultrasonic wave is supplied, the speed at which the pores are filled with the etchant increases.

In Fig. 1B, the pores grow by the etching function. At this time, preferably, no ultrasonic wave is supplied to the object to be processed, or the ultrasonic strength is reduced. If an ultrasonic wave is supplied, the porous layer starts to break as soon as the walls between adjacent pores become thin to some degree as the pores grow. Since the porous layer breaks first at thin portions, the surface of the underlying substrate 201 is etched in these portions. In this case, obviously film thickness uniformity of the surface layer of the substrate 201 degrades. However, when no ultrasonic wave is supplied, the pores do not break unless they become much thinner than in a case wherein an ultrasonic wave is supplied. In this case, therefore etching can be prevented from locally excessively progressing.

Even when no ultrasonic wave is supplied to the object to be processed, etching progresses not only in the horizontal direction (planar direction) but also in the vertical direction. However, the influence on etching is negligible compared to the case wherein an ultrasonic wave

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is supplied.

In Fig. 1C, the porous layer 202 with thin pore walls is removed. Not only etching but also polishing, scrubbing, or the water jet method can be applied to this step. In this step, the porous layer having a fragile structure upon etching is removed at once.

When etching is applied to the step shown in Fig. 1C, the steps in Figs. 1A to 1C can be executed using the same etching tank. In this case, the step shown in Fig. 1B is executed until pore walls at the deepest portion of the porous layer are thinned to immediately break in the entire region upon resupply of an ultrasonic wave, and then, the step in Fig. 1C is executed (supply of an ultrasonic wave). With this process, the porous layer can be removed at once, and almost simultaneously, the underlying substrate 201 can be exposed in the entire region of the object to be processed. For this reason, variations in etching can be reduced, and a given planarity of the underlying substrate 201 can be maintained.

The above porous layer removing method can be easily applied to batch processing of a number of substrates. More specifically, for each of a number of objects to be processed, after the pore walls at the deepest portion of the porous layer are thinned to allow immediate break in the entire region in the step shown in Fig. 1B, the step shown in Fig. 1C is executed.

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This porous layer removing method is preferably practiced while completely dipping the object to be processed in the etchant. In this case, particles can be prevented from sticking to the object to be processed near the interface between the etchant and air.

According to this porous layer removing method, by supplying an ultrasonic wave, etching is prompted to break the porous layer, and particles can be efficiently removed from the object to be processed.

When the porous layer is removed while changing the relative positional relationship between the ultrasonic source (e.g., an ultrasonic vibrator) and the object to be processed and, more specifically, the positional relationship between the substrate and a standing wave generated between the ultrasonic vibration surface and the liquid surface of the etchant, processing can be uniformly performed in all regions of the substrate surface. To do this, for example, the substrate is rotated, the substrate is swung, a carrier holding the substrate is swung, or the ultrasonic source is moved.

Application examples of the porous layer removing method will be described below.

(First Application Example)

The first application example is associated with an object fabrication method. Figs. 2A to 2C are views showing the fabrication method of this application example. In

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Fig. 2A, an Si substrate 401 locally having porous Si portions 402 is prepared. The Si substrate 401 is obtained by, e.g., forming a resist film on the Si substrate, patterning the resist film by lithography, and anodizing the resultant structure. In place of the resist film, a patterned Si_3N_4 film or wax may be employed. As this wax, wax having fluoric acid resistance, e.g., Apizoen wax (trade name) can be used.

In Fig. 2B, a non-porous layer (pattern) 403 is formed on the surface of the Si substrate shown in Fig. 2A.

In Fig. 2C, the porous Si portions 402 are removed. More specifically, first, the substrate shown in Fig. 2B, with the porous Si portions 402 exposed, is set in an etching apparatus having an etching tank filled with an etchant for porous Si, and etching is performed while supplying an ultrasonic wave.

When the pores of the porous Si portions 402 are sufficiently filled with the etchant, supply of the ultrasonic wave is stopped, and etching is continued. In this process, the pore walls in the porous Si portions 402 gradually thin. The color of porous Si portions 402 also gradually becomes lighter when viewed from the surface (lower side of the drawing). When the pore walls have sufficiently thinned, the underlying non-porous layer (pattern) 403 can be seen through the porous Si portions 402.

In this state, the remaining porous Si portions are

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removed. To remove the porous Si portions, for example, 1) etching is performed while resupplying an ultrasonic wave, or 2) etching is performed using an etchant with high Si etching rate.

To leave a hard structure, the porous Si portions may be removed by a jet of water.

When the entire Si substrate 401 is made of porous Si, only the non-porous layer formed on the substrate can be left. In addition, when the non-porous layer 403 is patterned, as described above, various structures including a cantilever shown in Fig. 2C can be formed.

(Second Application Example)

The second application example is associated with a semiconductor substrate manufacturing method. Figs. 3A to 3F show the semiconductor substrate manufacturing method of this application example. In Fig. 3A, a first single-crystal Si substrate 501 is prepared, and a porous Si layer 502 is formed on one surface of the first single-crystal Si substrate 501. In Fig. 3B, at least one non-porous layer 503 is formed on the porous Si layer 502. As the non-porous layer 503, a single-crystal Si layer, a polycrystalline Si layer, an amorphous Si layer, a metal layer, a compound semiconductor layer, or a superconductor layer is suitable. As the non-porous layer 503, a layer including a device structure such as a MOSFET may be formed. An SiO_2 layer 504 is preferably formed on the surface layer, thus completing

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the first substrate. This SiO_2 layer 504 is useful also because when the first substrate is bonded to a second substrate 505, the interface states of the bonding interface can be separated from the active layer.

Subsequently, as shown in Fig. 3D, the separately prepared second substrate 505 is brought into contact with the first substrate shown in Fig. 3C at room temperature via the SiO_2 layer 504. After this, anode bonding, pressing, a heat treatment as needed, or a combination thereof is performed to firmly bond the substrates.

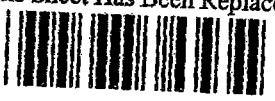
When a single-crystal Si layer is formed as the non-porous layer 503, the first substrate is preferably bonded to the second substrate 505 after the SiO_2 layer 504 is formed on the surface of the single-crystal Si layer by, e.g., thermal oxidation.

As the second substrate 505, an Si substrate, a substrate obtained by forming an SiO_2 layer on an Si substrate, a transparent substrate consisting of silica glass or quartz, or a sapphire substrate is suitable. Any other substrate can be used as far as the second substrate 505 has a sufficiently flat surface to be bonded.

Fig. 3D shows a state wherein the first substrate and the second substrate are bonded via the SiO_2 layer 504. If the non-porous layer 503 or the second substrate does not consist of Si, the SiO_2 layer 504 need not be formed.

In bonding, an insulating thin plate may be inserted

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between the first and the second substrates.

In Fig. 3E, the first Si substrate 501 is removed from the second substrate side at the porous Si layer 502. To remove the first substrate, either the first substrate side is discarded by grinding, polishing, or etching, or the bonded substrate stack is separated into the first substrate side and the second substrate at the porous Si layer 502.

In Fig. 3F, the porous Si layer 502 remaining on the surface on the second substrate side is removed. More specifically, first, the second substrate side is set in an etching tank filled with a porous Si etchant, and etching is performed while supplying an ultrasonic wave.

When the pores of the porous Si portions are sufficiently filled with the etchant, supply of the ultrasonic wave is stopped, and etching is continued. In this process, the pore walls in the porous Si layer 502 gradually thin. The color of porous Si layer 502 also gradually becomes lighter when viewed from the surface. When the pore walls have sufficiently thinned, the underlying non-porous layer (e.g., a single-crystal Si layer) 503 can be seen through the porous Si layer 502.

In this state, the remaining porous Si layer 502 is removed. To remove the porous Si layer, for example, 1) etching is performed while resupplying an ultrasonic wave, 2) etching is performed using an etchant with high Si etching rate, 3) the porous Si layer 502 is removed by a jet of water,

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4) the porous Si layer 502 is polished, or 5) scrubbing is performed.

Fig. 3F is a view schematically showing a semiconductor substrate (SOI substrate) obtained by the above method. The non-porous layer (e.g., a single-crystal Si layer) 503 with a flat surface and uniform film thickness is formed on the second substrate 505 via the insulating layer (e.g., an Sio_2 layer) 504. According to this method, a large-area semiconductor substrate having high quality can be manufactured.

When an insulating substrate is employed as the second substrate 505, the semiconductor substrate obtained by the above manufacturing method is very useful to form an insulated electronic device.

When the bonded substrate stack shown in Fig. 3D is divided at the porous Si layer 502, the first substrate can be reused after the porous Si layer 502 remaining on the first substrate 501 is removed, and the surface is planarized, as needed.

Specific examples of a wafer processing apparatus suitable to remove a porous layer will be listed below.

(First Arrangement of Processing Apparatus)

Fig. 4 is a perspective view showing the schematic arrangement of a wafer processing apparatus suitable to remove a porous layer.

In a wafer processing apparatus 100, members which may

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come into contact with the process solution are preferably made of silica glass or a plastic in accordance with their application purposes. As the plastic, a fluoroplastic, vinyl chloride, polyethylene, polypropylene, polybutylene terephthalate (PBT), or polyether ether ketone (PEEK) can be used. As the fluoroplastic, PVDF, PFA, or PTFE is suitable.

The wafer processing apparatus 100 comprises a wafer processing tank 110, an overflow tank 120, an ultrasonic tank 130, and a wafer rotating mechanism (111 to 119) for supporting wafers 140 while rotating them.

Before processing wafers, the wafer processing tank 110 is filled with a process solution (etchant). The overflow tank 120 for temporarily storing the process solution overflowing from the wafer processing tank 110 is mounted on the upper portion the wafer processing tank 110 to surround it. The process solution temporarily stored in the overflow tank 120 is discharged from the bottom portion of the overflow tank 120 to a circulator 121 through a discharge pipe 121a. The circulator 121 filters the discharged process solution to remove particles and sends the process solution to the bottom portion of the wafer processing tank 110 through a supply pipe 121b. With this arrangement, particles in the wafer processing tank 110 are efficiently removed.

The wafer processing tank 110 preferably has a depth with which the wafers 140 can be completely immersed. With

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this arrangement, particles in the air or near the liquid surface can be prevented from adhering to the wafers 140.

The ultrasonic tank 130 is located under the wafer processing tank 110. Inside the ultrasonic tank 130, an ultrasonic source 131 is supported by an adjustment mechanism 132. The adjustment mechanism 132 has, as mechanisms for adjusting the relative positional relationship between the ultrasonic source 131 and the wafer processing tank 110 has a mechanism, a mechanism for adjusting the vertical position of the ultrasonic source 131 and a mechanism for adjusting the horizontal position. With this mechanism, the ultrasonic wave to be supplied into the wafer processing tank 110 and, more specifically, to the wafers 140 can be optimized. The ultrasonic source 131 preferably has a function of adjusting the frequency or strength of the generated ultrasonic wave. With this arrangement, supply of an ultrasonic wave can be further optimized. By imparting the function of optimizing supply of an ultrasonic wave to the wafers 140, the ultrasonic wave can be supplied individually to a variety of types of wafers. The ultrasonic tank 130 is filled with an ultrasonic transmission medium (e.g., water), so the ultrasonic wave is transmitted to the wafer processing tank 110 through the ultrasonic transmission medium.

The wafer processing apparatus 100 has a control section for ON/OFF-controlling the ultrasonic source 131. With this control section, porous layer removing processing can be

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controlled.

The wafers 140 are held to be almost perpendicular to the bottom surface of the wafer processing tank 110 by four wafer rotary rods 111 each having grooves 111a engaging with the wafers 140. The wafer rotary rods 111 have a function of supporting the wafers 140 while rotating them and constitute part of the wafer rotating mechanism. Each wafer rotary rod 111 is pivotally supported by a pair of rod support members 118 opposite to each other, so the wafer rotary rods 111 rotate in the same direction upon receiving a driving torque generated by a motor 119. Each wafer rotary rod 111 preferably has a small diameter not to impede transmission of the ultrasonic wave.

The number of wafer rotary rods 111 is preferably as small as possible. To ensure a desired frictional force with respect to the wafers 140, preferably, two wafer rotary rods 111 for limiting movement in the rolling direction (X-axis direction) of the wafers 140, and two wafer rotary rods 111 for supporting the wafers 140 from the lower side are provided. When two wafer rotary rods 111 are disposed at an appropriate interval below the wafers, the driving torque can be efficiently transmitted to the wafers having an orientation flat. If only one wafer rotary rod 111 is placed underneath the wafers, and the orientation flat is positioned above this wafer rotary rod 111, the wafers cannot be rotated by the wafer rotary rod 111.

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Normally, a standing wave, i.e., an ultrasonic wave having a high-strength portion and a low-strength portion is formed between the bottom surface of the wafer processing tank 110 and the liquid surface. However, since this wafer processing apparatus 100 can process the wafers 140 while rotating them, nonuniformity in processing due to the standing wave can be reduced.

In the wafer processing apparatus 100, the number of members on the bottom portion of the wafer processing tank 110 or around the wafers 140 is decreased as small as possible. For this reason, the ultrasonic wave can be efficiently and uniformly supplied to the wafers 140. In addition, with this arrangement, since the process solution can freely flow around the wafers 140, the wafers can be uniformly processed, and processing defects can be prevented.

(Second Arrangement of Wafer Processing Apparatus)

Fig. 5 is a view showing the schematic arrangement of a wafer processing apparatus suitable to remove a porous layer.

In a wafer processing apparatus 10, members which may come into contact with the process solution are preferably made of silica glass or a plastic in accordance with their application purposes. As the plastic, a fluoroplastic, vinyl chloride, polyethylene, polypropylene, polybutylene terephthalate (PBT), or polyether ether ketone (PEEK) can be used. As the fluoroplastic, PVDF, PFA, or PTFE is

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suitable.

The wafer processing apparatus 10 comprises a wafer processing tank 11, and a holder driving mechanism 31 for swinging a wafer holder 21 in the wafer processing tank 11. The wafer processing apparatus 10 preferably has an ultrasonic tank 61.

Before processing wafers, the wafer processing tank 11 is filled with a process solution. The wafer processing tank 11 has a four-side overflow tank 12. The process solution is supplied by a circulator 71 with a filter from the bottom portion of the wafer processing tank 11 into the wafer processing tank 11. The process solution overflowing from the wafer processing tank 11 is stored in the four-side overflow tank 12 and discharged from the bottom portion of the four-side overflow tank 12 to the circulator 71. In this wafer processing apparatus 10, the wafer holder 21 is swung by the holder driving mechanism 31, and simultaneously, the process solution is stirred. For this reason, the circulating system including the four-side overflow tank 12 is extremely effective to maintain a constant liquid surface of the process solution.

As the wafer holder 21, a commercially available product can be used. The wafer holder 21 is preferably made of silica glass or a plastic. As the plastic, a fluoroplastic, vinyl chloride, polyethylene, polypropylene, polybutylene terephthalate (PBT), or polyether ether ketone (PEEK) can

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be used. As the fluoroplastic, PVDF, PFA, or PTFE is suitable.

The holder driving mechanism 31 has a pair of holding portions 31a for holding the wafer holder 21. The wafer holder 21 is held by the pair of holding portion 31a and dipped in the wafer processing tank 11. Desired processing can be performed for a wafer 40 while swinging the wafer holder 21 in the wafer processing tank 11. The holder driving mechanism 31 has a function of conveying the wafer holder 21 storing wafers 40 which have been processed in the preceding step to the wafer processing tank 11 or to the next step. The holder driving mechanism 31 also has a function as part of the wafer processing apparatus 10.

In this embodiment, the holding portions 31a hold the wafer holder 21, so the wafer 40 is indirectly held. However, the holding portions 31a may be replaced with, e.g., chuck pads to directly hold the wafer 40. The direction in which the wafer 40 is held is not limited to the direction perpendicular to the bottom surface of the wafer processing tank 11 and may be parallel to the bottom surface.

The ultrasonic tank 61 has an ultrasonic source 51 and is filled with an ultrasonic transmission medium (e.g., water). The ultrasonic source 51 is fixed on an adjustment mechanism 62 for adjusting the vertical and/or horizontal position of the ultrasonic source 51. When the positional relationship between the ultrasonic source 51 and the wafer

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processing tank 11 is adjusted by the adjustment mechanism 62, the ultrasonic wave to be supplied to the wafer processing tank 11 and, more specifically, to the wafer 40 can be optimized. The ultrasonic source 51 preferably has a function of adjusting the frequency or strength of the generated ultrasonic wave. With this arrangement, supply of an ultrasonic wave can be further optimized. By imparting the function of optimizing supply of an ultrasonic wave to the wafer 40, the ultrasonic wave can be supplied individually to a variety of types of wafers.

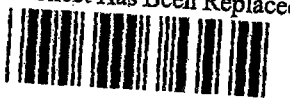
The wafer processing apparatus 10 has a control section for ON/OFF-controlling the ultrasonic source 51. With this control section, porous layer removing processing can be controlled.

(Third Arrangement of Wafer Processing Apparatus)

Fig. 6 is a view showing the schematic arrangement of a wafer processing apparatus suitable to remove a porous layer. Figs. 7A to 7E are views showing operation of the wafer processing apparatus shown in Fig. 6. Fig. 8 is a perspective view of a swing assist member in the wafer processing apparatus shown in Fig. 6.

The wafer processing tank 11 preferably has, on the bottom surface, a swing assist member 13 for increasing the efficiency of swing of the wafer 40 by the holder driving mechanism 31. The swing assist member 13 comes into contact with the side surface of the wafer 40 held by the wafer holder

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21 when the wafer holder 21 moves, thereby rotating and vertically moving the wafer 40 in the wafer holder 21 by the frictional force. The swing assist member 13 is useful to improve the surface uniformity of the processed wafer.

It is also effective to use a driving mechanism for vertically (Y-axis direction) and/or horizontally (X-axis direction) moving the swing assist member 13. In this case, the swing assist member 13 itself moves to rotate the wafer 40 and vertically move the wafer 40 in the wafer holder 21. Therefore, the range in which the holder driving mechanism 31 moves the wafer holder 21 can be made small. In other words, the wafer processing tank 11 can be made compact.

The ultrasonic tank 61 has the ultrasonic source 51 and is filled with an ultrasonic transmission medium (e.g., water). The ultrasonic source 51 is fixed on the adjustment mechanism 62 for adjusting the vertical and/or horizontal position of the ultrasonic source 51. When the positional relationship between the ultrasonic source 51 and the wafer processing tank 11 is adjusted by the adjustment mechanism 62, the ultrasonic wave to be supplied to the wafer processing tank 11 and, more specifically, to the wafer 40 can be optimized. The ultrasonic source 51 preferably has a function of adjusting the frequency or strength of the generated ultrasonic wave. With this arrangement, supply of an ultrasonic wave can be further optimized. By imparting the function of optimizing supply of an ultrasonic wave to

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the wafer 40, the ultrasonic wave can be supplied individually to a variety of types of wafers.

The wafer processing apparatus 10 has a control section for ON/OFF-controlling the ultrasonic source 51. With this control section, porous layer removing processing can be controlled.

Figs. 7A to 7E are views for explaining a wafer swing method. In these drawings, arrows indicate the moving directions of the wafer holder 21. Fig. 7A shows a state immediately before the wafer starts to be swung. When the start of wafer swing operation is instructed, the holder driving mechanism 31 presses the holding portions 31a downward under computer control, as shown in Fig. 7B. The side surface of the wafer 40 comes into contact with the swing assist member 13 midway this pressing. The wafer 40 is supported by the swing assist member 13 at its lower portion.

When the swing assist member 13 comes into contact with the wafer 40, particles may be produced albeit in a small amount. To prevent this, the distal end portion of the swing assist member 13 is preferably has a round shape, as shown in Fig. 8, for smooth contact with the wafer 40.

The swing assist member 13 only need to assist swing of the wafer 40 and therefore can have a shape not to impede transmission of the ultrasonic wave, e.g., a thin plate-like shape. With this arrangement, the ultrasonic wave can be uniformly supplied to the wafer 40, and the wafer 40 can

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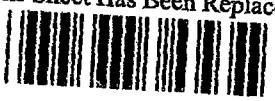
be uniformly processed.

In this wafer processing apparatus 10, the wafer 40 is processed while changing the relative positional relationship between the wafer 40 and the swing assist member 13, i.e., the relative positional relationship between the wafer 40 and the wafer processing tank 11. For this reason, slight nonuniformity of the ultrasonic wave due to the swing assist member 13 poses no problem.

When the press amount of the wafer holder 21 is large to some extent, the contact pressure between the wafer 40 and the swing assist member 13 can be increased. Hence, sliding movement between the swing assist member 13 and the wafer 40 is eliminated to prevent operation failures. If the press amount is small, the gravity against the wafer 40 acts more largely on the wafer holder 21 than on the distal end portion of the swing assist member 13. When the swing assist member 13 having the shape of this embodiment is used, the press amount is preferably set to be about 30 mm after the wafer 40 comes into contact with the swing assist member 13.

When the operation of pressing the wafer holder 21 is ended, the holder driving mechanism 31 moves the holding portions 31a to the right (positive X-axis direction) under computer control, as shown in Fig. 7C. The wafer 40 substantially horizontally moves to the right (positive X-axis direction) in the wafer processing tank 11 while rotating clockwise. The moving amount of the holding

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portions 31a must be set within the range in which the holding portions 31a do not collide against the lower opening portion of the wafer holder 21.

When movement of the wafer holder 21 to the right (positive X-axis direction) is ended, the holder driving mechanism 31 moves the holding portions 31a upward under computer control, as shown in Fig. 7D. The moving amount of the holding portions 31a is preferably set within the range in which the wafer 40 does not come close to a liquid surface 14 of the process solution. If the wafer 40 comes close to the liquid surface 14, particles may adhere to the surface of the wafer 40.

When movement of the wafer holder 21 upward is ended, the holder driving mechanism 31 moves the holding portions 31a to the left (negative X-axis direction) under computer control, as shown in Fig. 7E, so the initial state is restored (Fig. 7A).

By repeating the above operation (Fig. 7A → Fig. 7B → Fig. 7C → Fig. 7D → Fig. 7E), the wafer 40 can be appropriately swung and uniformly processed.

According to the wafer processing apparatus 10, since the wafer 40 is swung in the region where supply of an ultrasonic wave is optimized by adjusting the ultrasonic tank 61, the ultrasonic wave acting on the wafer 40 can be optimized.

As is known, the standing wave of an ultrasonic wave

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has antinodes and nodes at a predetermined interval. Therefore, it is difficult to uniform the ultrasonic wave in the wafer processing tank 11.

However, in this wafer processing apparatus 10, processing for the wafer 40 can be uniformed independently of the nonuniform strength distribution of the ultrasonic wave because the holder driving mechanism 31 swings the wafer 40. Even when the wafer 40 is simply moved only in the horizontal direction, vertical direction, or oblique direction, processing for the wafer 40 can be uniformed. When the wafer 40 is also swung in the axial direction (Z-axis direction), nonuniformity in processing between wafers due to the high-strength portion of the ultrasonic wave in the horizontal plane can also be corrected.

Since the wafer processing apparatus 10 has the swing assist member 13, the swing amount of the wafer 40 can be efficiently increased. The fixed position of the swing assist member 13 is not limited to the bottom portion of the wafer processing tank 11. As far as the swing assist member 13 can contact all wafers 40 in the wafer holder 21, the swing assist member 13 may be fixed on the inner wall of the wafer processing tank 11 or on the holder driving mechanism 31 (in this case, a mechanism for changing the relative positional relationship between the holding portions 31a and the swing assist member 13 is required).

In addition, according to the wafer processing

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apparatus 10, since no driving mechanism is present in the wafer processing tank 11, particles are not produced due to operation of the driving mechanism.

(Fourth Arrangement of Wafer Processing Apparatus)

Fig. 9 is a view showing the schematic arrangement of a wafer processing apparatus suitable to remove a porous layer.

In a wafer processing apparatus 300, the wafer 40 is held almost parallel to the bottom surface of the wafer processing tank 11 (i.e., almost parallel to the vibration plane of the ultrasonic wave) and completely dipped in the process solution (etchant) in the wafer processing tank 11, and in this state, swung by a wafer moving mechanism 80, thereby uniformly processing the wafer 40 and prevent contamination by particles.

The wafer moving mechanism 80 holds the wafer 40 with an arm 81 and swings the wafer 40 in the wafer processing tank 11. The wafer 40 is preferably swung in a direction crossing the vibration plane of the ultrasonic wave (i.e., in the vertical direction) and a direction parallel to the vibration plane (i.e., in the horizontal direction).

In this wafer processing apparatus 300 as well, preferably, the wafer 40 completely dipped in the process solution is processed. In this case, particles can be prevented from adhering to the wafer 40 near the interface between the process solution and gas.

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According to the wafer processing apparatus 300, the wafer 40 can be uniformly processed by swinging the wafer 40 in the wafer processing tank 11.

(Fifth Arrangement of Wafer Processing Apparatus)

Fig. 10 is a view showing the schematic arrangement of a wafer processing apparatus suitable to remove a porous layer. In the wafer processing apparatuses of the second to fourth arrangements, wafers are processed while being swung. In a wafer processing apparatus 500 of the fifth arrangement, the speed of flow of the process solution (etchant) is increased instead of swinging wafers.

In the wafer processing apparatus 500, a support portion 73 for supporting the wafer holder 21 is placed at the lower portion of the wafer processing tank 11. The process solution supplied from the circulator 71 spouts from spout ports 72 under the support portion 73 at a high speed. The support portion 73 has a plurality of opening portions. The process solution spouted from the spout ports 72 moves upward through the opening portions.

When the process solution is circulated at a high speed, the wafer 40 can be uniformly processed.

It is also effective to assemble the above-described circulating mechanism (71 to 73) in the wafer processing apparatus 10 shown in Fig. 5.

(Sixth Arrangement of Wafer Processing Apparatus)

In the above-described wafer processing apparatuses,

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supply and nonsupply of the ultrasonic wave to the wafer processing tank are switched by controlling the ultrasonic source. Instead, a mechanism for shielding the ultrasonic wave as needed may be inserted between the ultrasonic source and the wafer.

A modification of the wafer processing apparatus shown in Fig. 5 or 6 will be described. Figs. 11A and 11B show a modification of the wafer processing apparatus shown in Fig. 5 or 6. In Figs. 11A and 11B, the overflow tank and the circulator are omitted.

The wafer processing apparatus of this modification has shutters 91 and 92 for shielding the ultrasonic wave, as needed, between the ultrasonic source 51 and the bottom surface of the wafer processing tank 11. To transmit the ultrasonic wave to the wafer processing tank 11, the shutters 91 and 92 are opened by a driving section (not shown), as shown in Fig. 11A. To shield the ultrasonic wave to the wafer processing tank 11, the shutters 91 and 92 are closed by the driving section (not shown), as shown in Fig. 11B. As the material of the shutters 91 and 92, a material which hardly transmits the ultrasonic wave, e.g., PFA or PTFE is suitable.

(Seventh Arrangement of Wafer Processing Apparatus)

Figs. 12A to 12C are views showing the schematic arrangement of a wafer processing apparatus suitable to remove a porous layer. Fig. 12A is a front view, Fig. 12B is a side view, and Fig. 1C is a plan view.

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In a wafer processing apparatus 700, a jet of fluid (e.g., water) 701 is sprayed from the spray nozzle 700, and the porous layer of the wafer 40 is removed by the sprayed fluid.

In the example shown in Figs. 12A to 12C, the spray nozzle 700 is scanned in the Z-axis direction while spraying the fluid 701 from the spray nozzle 700 perpendicularly to the wafer 40, thereby removing a porous layer 40a on the entire surface.

Examples to which the above porous layer removing method is applied will be described below.

(Example 1)

A film of a material having a HF resistance was formed on the surface of a single-crystal Si substrate and patterned to form a mask pattern having an opening. The single-crystal Si substrate exposed in the opening portion was anodized in an HF solution to form a porous layer. With this process, a 50-μm thick porous layer was formed on the single-crystal Si substrate. Next, the mask pattern was removed. Instead of forming a mask pattern on the single-crystal Si substrate, the single-crystal Si substrate may be set in a holder with which the HF solution can contact only the region where the porous layer is to be formed, and subjected to anodizing.

The resultant substrate was set in the processing apparatus 100 shown in Fig. 4. The wafer processing tank 110 of the processing apparatus 100 shown in Fig. 4 was filled with a mixed solution (etchant) of fluoric acid, hydrogen

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peroxide, and pure water in advance. In the processing apparatus 100, the substrate was rotated for about 2 hrs, and at the same time, an ultrasonic wave near 1 MHz was applied to fill pores in the porous Si layer with the etchant.

The operation of the ultrasonic source 131 was stopped, and the substrate was left to stand in the wafer processing tank 110 for about 1 hr. With this process, the pore walls of the porous Si layer thinned.

Subsequently, the porous Si layer was completely removed using the apparatus shown in Figs. 12A to 12C. As a result, a structure having a 50-μm deep recessed portion on the substrate surface was formed.

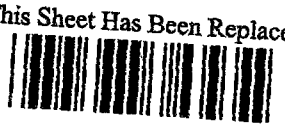
The same structure as described above could be formed using the apparatus shown in Fig. 5, 6, or 9.

(Example 2)

A film of a material having a HF resistance was formed on the surface of a single-crystal Si substrate and patterned to form a mask pattern having an opening. The single-crystal Si substrate exposed in the opening portion was anodized in an HF solution to form a porous layer reaching the lower surface. Then, the mask pattern was removed. Instead of forming a mask pattern on the single-crystal Si substrate, the single-crystal Si substrate may be set in a holder with which the HF solution can contact only the region where the porous layer is to be formed, and subjected to anodizing.

Subsequently, a single-crystal Si layer having a

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thickness of 1 μm was formed on the surface of the substrate as a resultant structure by epitaxial growth.

The resultant substrate was set in the processing apparatus 100 shown in Fig. 4. The wafer processing tank 110 of the processing apparatus 100 shown in Fig. 4 was filled with a mixed solution (etchant) of fluoric acid, hydrogen peroxide, and pure water in advance. In the processing apparatus 100, the substrate was rotated for about 6 hrs, and at the same time, an ultrasonic wave near 0.25 MHz was applied to fill pores in the porous Si layer with the etchant.

The operation of the ultrasonic source 131 was stopped, and the substrate was left to stand in the wafer processing tank 110 for about 2 hrs. With this process, the pore walls of the porous Si layer thinned.

The ultrasonic source 131 was operated again for about 5 min to completely remove the porous Si layer. As a result, a single-crystal Si membrane including the epitaxial layer (single-crystal Si layer) formed on the porous Si layer was formed. The epitaxial layer had a virtually uniform thickness on the entire surface.

A cantilever structure of single-crystal Si may be formed, as shown in Fig. 2C, by partially removing the epitaxial layer (single-crystal Si layer) in advance.

The same result as described above could be obtained by the apparatus shown in Fig. 5, 6, or 9.

(Example 3)

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A first single-crystal Si substrate was prepared. The surface layer was anodized in a HF solution to form a porous Si layer. The anodizing conditions were as follows.

Current density: 7 (mA/cm^2)

Anodizing solution: $HF : H_2O : C_2H_5OH = 1 : 1 : 1$

Time: 11 (min)

Thickness of porous Si layer: 12 (μm)

This substrate was then oxidized in an oxygen atmosphere at 400°C for 1 hr. Upon this oxidation, the inner wall of each pore of the porous Si layer was covered with a thermal oxide film. A single-crystal Si layer having a thickness of 0.30 μm was epitaxially grown on the porous Si layer by CVD (Chemical Vapor Deposition). The growing conditions were as follows.

Source gas: SiH_2Cl_2/H_2

Gas flow rate: 0.5/180 (l/min)

Gas pressure: 80 (Torr)

Temperature: 950 (°C)

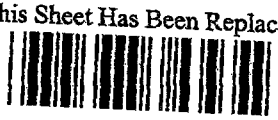
Growth rate: 0.3 (μm/min)

Subsequently, an SiO_2 layer having a thickness of 200 nm was formed on the epitaxial Si layer by thermal oxidation.

The surface of the SiO_2 layer of the first substrate was bonded to the surface of a prepared Si substrate (second substrate).

The first substrate side was removed by grinding, polishing, or etching to expose the porous Si layer in the

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entire region on the second substrate.

The second substrate was set in the wafer processing apparatus 100 shown in Fig. 4. The wafer processing tank 110 of the processing apparatus shown in Fig. 4 was filled with a mixed solution (etchant) of fluoric acid, hydrogen peroxide, and pure water in advance. In the processing apparatus 100, the second substrate was rotated for about 1.5 hrs, and at the same time, an ultrasonic wave near 0.25 MHz was applied to fill pores in the porous Si layer with the etchant.

The operation of the ultrasonic source 131 was stopped, and the substrate was left to stand in the wafer processing tank 110 for about 1 hr. With this process, the pore walls of the porous Si layer thinned.

The ultrasonic source 131 was operated again for about 5 min to completely remove the porous Si layer. At this time, when the etchant is appropriately circulated, as shown in Fig. 10, surface uniformity of the processed substrate increases.

The ultrasonic wave is applied to the etchant for the porous Si layer, the substrate is rotated, and simultaneously, the etchant is circulated to fill the pores in the porous layer on the substrate with the etchant. After this, application of the ultrasonic wave is stopped, and the substrate is left to stand for an appropriate time. With this process, for each of all substrates, the pore walls in the porous Si layer can be sufficiently thinned in the entire

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region on the surface. For this reason, the remaining porous Si layer can be removed at once uniformly on the entire region of each substrate.

The same result as described above could be obtained by the apparatus shown in Fig. 5, 6, or 9.

Even when one of the following methods is employed instead of the method of applying an ultrasonic wave again after application of the ultrasonic wave is stopped, the remaining porous Si layer can be removed with high quality.

(1) The resultant structure is dipped in a mixed solution of fluoric acid, nitric acid, and pure water for about 5 sec to remove the porous layer.

(2) The porous Si layer is removed by polishing.

(3) The porous Si layer is removed by scrubbing.

(4) The porous Si layer is removed by scanning the substrate while spraying a water jet at a pressure of, e.g., 1,000 kg/cm^2.

In the step of removing the porous Si layer, the single-crystal Si layer functioned as an etch stop layer, so the porous Si layer was selectively etched and completely removed.

The etching rate of the non-porous Si single crystal for the above etchant is very low. The selectivity ratio to the etching rate of the non-porous Si single crystal to that of the porous layer is 10^5 or more. The etching amount of the non-porous layer (about several ten Å) is allowable for

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practical use.

With the above process, an SOI substrate having a 0.2-μm thick single-crystal Si layer on the Si oxide film was formed. The thickness of the resultant single-crystal Si layer was measured at 100 points on the entire surface. The thickness was 201 nm ± 4 nm.

The resultant structure was subjected to a heat treatment in hydrogen at 1,100°C for 1 hr, and the surface roughness was evaluated with an atomic force microscope. The mean square roughness in a 5-μm square area was about 0.2 nm. This nearly equals that of a commercially available Si wafer.

Section observation with a transmission electron microscope revealed that no new crystal defects were formed in the single-crystal Si layer, and satisfactory crystallinity was maintained.

The same result as described above was obtained even when the oxide film (SiO_2) was formed not on the surface of the epitaxial layer but on the surface of the second substrate or on both these surfaces.

A satisfactory result was obtained even when a transparent substrate of silica glass or the like was used as the second substrate. In this case, however, since a slip may be formed in the single-crystal Si layer due to some difference in thermal expansion coefficient between silica glass and the single-crystal Si layer, the temperature of

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the heat treatment in hydrogen was decreased from 1,100°C to 1,000°C or less.

(Example 4)

A second substrate was subjected to two-step anodizing in an HF solution to form two porous layers. The anodizing conditions were as follows.

<Anodizing of First Step>

Current density: 7 (mA/cm^2)

Anodizing solution: HF : H_2O : C_2H_5OH = 1 : 1 : 1

Time: 5 (min)

Thickness of porous Si layer: 5.5 (μm)

<Anodizing of Second Step>

Current density: 30 (mA/cm^2)

Anodizing solution: HF : H_2O : C_2H_5OH = 1 : 1 : 1

Time: 110 (sec)

Thickness of porous Si layer: 3 (μm)

Subsequently, this substrate was oxidized in an oxygen atmosphere at 400°C for 1 hr. Upon this oxidation, the inner wall of each pore of the porous Si layer was covered with a thermal oxide film. A single-crystal Si layer having a thickness of 0.15 μm was epitaxially grown on the porous Si layer by CVD (Chemical Vapor Deposition). The growing conditions were as follows.

Source gas: SiH_2Cl_2/H_2

Gas flow rate: 0.5/180 (l/min)

Gas pressure: 80 (Torr)

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Temperature: 950 (°C)

Growth rate: 0.3 (μm/min)

After that, an SiO_2 layer having a thickness of 100 nm was formed on the epitaxial Si layer by thermal oxidation.

The surface of the SiO_2 layer of the first substrate was bonded to the surface of a prepared Si substrate (second substrate).

The bonded substrate stack was divided into two substrates by the porous Si layer formed at a current density of 30 mA/cm^2 (anodizing of second step) to expose the porous Si layer to the entire surface on the second substrate side. To divide the bonded substrate stack, the substrates are mechanically pulled, twisted, or pressed, a wedge is driven into the edge of the bonded substrate stack, the bonded substrate stack is oxidized from the end face to peel the substrates, thermal stress is used, an ultrasonic wave is applied, or a water jet is injected into the edge of the bonded substrate stack.

The second substrate was set in the wafer processing apparatus 100 shown in Fig. 4. The wafer processing tank 110 of the processing apparatus shown in Fig. 4 was filled with a mixed solution (etchant) of fluoric acid, hydrogen peroxide, and pure water in advance. In the processing apparatus 100, the second substrate was rotated for about 1.5 hrs, and at the same time, an ultrasonic wave near 0.25 MHz was applied to fill pores in the porous Si layer with the etchant.

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The operation of the ultrasonic source 131 was stopped, and the substrate was left to stand in the wafer processing tank 110 for about 1 hr. With this process, the pore walls of the porous Si layer thinned.

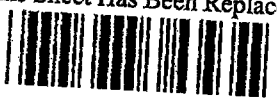
The ultrasonic source 131 was operated again for about 5 min to completely remove the porous Si layer. At this time, when the etchant is appropriately circulated, as shown in Fig. 10, surface uniformity of the processed substrate improves.

The ultrasonic wave is applied to the etchant for the porous Si layer, the substrate is rotated, and simultaneously, the etchant is circulated to fill the pores in the porous layer on the substrate with the etchant. After this, application of the ultrasonic wave is stopped, and the substrate was left to stand for an appropriate time. With this process, for each of all substrates, the pore walls in the porous Si layer can be sufficiently thinned in the entire region on the surface. For this reason, the remaining porous Si layer can be removed at once uniformly on the entire region of each substrate.

The same result as described above could be obtained by the apparatus shown in Fig. 5, 6, or 9.

Even when one of the following methods is employed instead of the method of applying an ultrasonic wave again after application of the ultrasonic wave is stopped, the remaining porous Si layer can be removed with high quality.

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(1) The resultant structure is dipped in a mixed solution of fluoric acid, nitric acid, and pure water for about 5 sec to remove the porous layer.

(2) The porous Si layer is removed by polishing.

(3) The porous Si layer is removed by scrubbing.

(4) The porous Si layer is removed by scanning the substrate while spraying a water jet at a pressure of, e.g., 1,000 kg/cm^2.

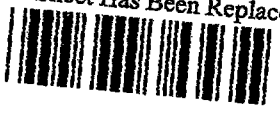
In the step of removing the porous Si layer, the single-crystal Si layer functioned as an etch stop layer, so the porous Si layer was selectively etched and completely removed.

The etching rate of the non-porous Si single crystal for the above etchant is very low. The selectivity ratio to the etching rate of the non-porous Si single crystal to that of the porous layer is 10^5 or more. The etching amount of the non-porous layer (about several ten Å) is allowable for practical use.

With the above process, an SOI substrate having a 0.1-μm thick single-crystal Si layer on the Si oxide film was formed. The thickness of the resultant single-crystal Si layer was measured at 100 points on the entire surface. The thickness was 101 nm ± 3 nm.

The resultant structure was subjected to a heat treatment in hydrogen at 1,100°C for 1 hr, and the surface roughness was evaluated with an atomic force microscope. The

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mean square roughness in a 5-μm square area was about 0.2 nm. This nearly equals that of a commercially available Si wafer.

Section observation with a transmission electron microscope revealed that no new crystal defects were formed in the single-crystal Si layer, and satisfactory crystallinity was maintained.

The same result as described above was obtained even when the oxide film was formed not on the surface of the epitaxial layer but on the surface of the second substrate or on both these surfaces.

A satisfactory result was obtained even when a transparent substrate of silica glass or the like was used as the second substrate. However, since a slip may be formed in the single-crystal Si layer due to some difference in thermal expansion coefficient between silica glass and the Si layer, the temperature of the heat treatment in hydrogen was decreased from 1,100°C to 1,000°C or less.

Section observation with a transmission electron microscope indicated that no new crystal defects were formed in the single-crystal Si layer, and satisfactory crystallinity was maintained.

The same result as described above was obtained even when the oxide film (SiO_2) was formed not on the surface of the epitaxial layer but on the surface of the second substrate or on both these surfaces.

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A satisfactory result was obtained even when a transparent substrate of silica glass or the like was used as the second substrate. However, since a slip may be formed in the single-crystal Si layer due to any difference in thermal expansion coefficient between silica glass and the single-crystal Si layer, the temperature of the heat treatment in hydrogen was decreased from 1,100°C to 1,000°C or less.

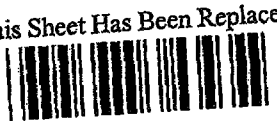
When the porous Si layer left on the first substrate side was selectively etched and subjected to a surface treatment such as hydrogen annealing or surface polishing, the substrate could be recycled as the first or second substrate.

Almost the same result as described above was obtained even when a porous layer with a single-layered structure was formed by anodizing.

In the above examples, as the epitaxial growing method of forming a single-crystal Si layer on the porous Si layer, not only CVD but also MBE, sputtering, or liquid phase growing can be used. A single-crystal compound semiconductor layer of GaAs or InP may be epitaxially grown on the porous Si layer. In this case, a high-frequency device such as GaAs on Si or GaAs on Glass (Quartz) or a substrate suitable for OEIC can be manufactured.

As the etchant used to selectively etch the porous Si layer, a mixed solution of 49% fluoric acid, 30% hydrogen

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peroxide and H_2O is suitable. However, the following etchants can also be used. Since the porous Si layer has a large surface area, selective etching is easy.

(a) Fluoric acid

(b) Mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to fluoric acid

(c) Buffered fluoric acid

(d) Mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to buffered fluoric acid

(e) Mixed solution of fluoric acid, nitric acid, and acetic acid.

In the above examples, to stop application of the ultrasonic wave, the operation of the ultrasonic source is stopped. However, use of shutters is also effective, as shown in Figs. 11A and 11B.

According to the present invention, a high planarity of the underlying layer of the porous region can be maintained.

The present invention is not limited to the above embodiments and various changes and modifications can be made within the spirit and scope of the present invention. Therefore, to apprise the public of the scope of the present invention, the following claims are made.

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WHAT IS CLAIMED IS:

1. A porous region removing method of removing a porous region from a substrate having the porous region, characterized by comprising:

the first step of processing the porous region by an etchant while supplying an ultrasonic wave to the etchant;

the second step of processing the porous region by the etchant without supplying any ultrasonic wave to the etchant or while supplying an ultrasonic wave weaker than the ultrasonic wave supplied in the first step to the etchant; and

the third step of removing the porous region remaining on the substrate.

2. The method according to claim 1, characterized in that the first step comprises filling pores in the porous region with the etchant to a deep portion.

3. The method according to claim 1 or 2, characterized in that the second step comprises thinning pore walls in the porous region to not more than a predetermined thickness by an etching function.

4. The method according to claim 3, characterized in that the second step comprises thinning the pore walls in the

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porous region to a thickness that allows removal of the remaining porous region at once in the third step.

5. The method according to any one of claims 1 to 4, characterized in that the third step comprises removing the porous region remaining on the substrate by the etchant.

6. The method according to claim 5, characterized in that the third step comprises removing the porous region remaining on the substrate by the etchant while supplying the ultrasonic wave to the etchant.

7. The method according to claim 5 or 6, characterized in that the first to third steps are executed while dipping the substrate to be processed in the same etchant.

8. The method according to claim 5 or 6, characterized in that the third step comprises removing the porous region remaining on the substrate by an etchant whose etching rate for the porous region is higher than that of the first or second etchant.

9. The method according to any one of claims 5 to 8, characterized in that the first to third steps are executed while completely dipping the substrate to be processed in the etchant.

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10. The method according to any one of claims 1 to 4, characterized in that the first and/or second steps is executed while completely dipping the substrate to be processed in the etchant.

11. The method according to any one of claims 1 to 4, characterized in that the third step comprises removing the porous region remaining on the substrate by a high-pressure fluid.

12. The method according to any one of claims 1 to 4, characterized in that the third step comprises removing the porous region remaining on the substrate by scrubbing.

13. The method according to any one of claims 1 to 12, characterized in that in processing the substrate while supplying the ultrasonic wave to the etchant, a relative positional relationship between an ultrasonic source and the substrate is changed.

14. The method according to claim 13, characterized in that in processing the substrate while supplying the ultrasonic wave to the etchant, the substrate is swung in the etchant.

15. The method according to claim 13, characterized in that

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in processing the substrate while supplying the ultrasonic wave to the etchant, the substrate is rotated.

16. The method according to claim 13, characterized in that in processing the substrate while supplying the ultrasonic wave to the etchant, a position of at least one of the substrate and the ultrasonic source is changed substantially in a direction parallel or perpendicular to a vibration plane of the ultrasonic wave.

17. The method according to any one of claims 1 to 12, characterized in that in processing the substrate by the etchant, the substrate is swung or rotated.

18. The method according to any one of claims 1 to 12, characterized in that in processing the substrate by the etchant, the etchant is circulated to form a flow of etchant near the substrate.

19. The method according to any one of claims 1 to 18, characterized in that the first and second steps are executed while dipping the substrate in the same etching tank, the first step comprises operating the ultrasonic source, and the second step comprises stopping operation of the ultrasonic source.

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20. The method according to any one of claims 1 to 18, characterized in that the first and second steps are executed while dipping the substrate in the same etching tank, the first and second steps comprise continuously operating the ultrasonic source, and the second step comprises inserting an ultrasonic shielding plate between the ultrasonic source and the substrate.

21. The method according to any one of claims 1 to 20, characterized in that the substrate to be processed essentially consists of single-crystal Si.

22. The method according to any one of claims 1 to 20, characterized in that the porous region essentially consists of porous Si.

23. The method according to claim 22, characterized in that the porous region is formed by anodizing a single-crystal Si substrate.

24. The method according to any one of claims 1 to 23, characterized in that as the etchant, any one of

(a) fluoric acid,

(b) a mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to fluoric acid,

(c) buffered fluoric acid, and

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(d) a mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to buffered fluoric acid is used.

25. A semiconductor substrate manufacturing method characterized by comprising the steps of:

forming a porous layer and at least one non-porous layer on a first substrate;

bonding a second substrate to the non-porous layer side of the first substrate;

removing the first substrate from the bonded substrate stack to expose the porous layer on a surface of the second substrate; and

removing the porous layer on the second substrate using any one of the methods of claims 1 to 24.

26. The method according to claim 25, characterized in that the step of exposing the porous layer comprises grinding, polishing, or etching the first substrate from a back surface side of the first substrate of the bonded substrate stack, thereby exposing the porous layer to the surface of the second substrate.

27. The method according to claim 25, characterized in that the step of exposing the porous layer comprises dividing the bonded substrate stack at the porous layer, thereby exposing

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the porous layer on the surface of the second substrate.

28. The method according to any one of claims 25 to 27, characterized in that the non-porous layer includes a single-crystal Si layer.

29. The method according to any one of claims 25 to 27, characterized in that the non-porous layer includes a single-crystal Si layer and an Si oxide layer.

30. The method according to claim 28 or 29, characterized in that the single-crystal Si layer is epitaxially grown on the porous layer on the first substrate.

31. The method according to any one of claims 25 to 27, characterized in that the non-porous layer includes a single-crystal compound semiconductor layer.

32. The method according to any one of claims 25 to 31, characterized in that the second substrate essentially consists of an Si material.

33. The method according to any one of claims 25 to 32, characterized in that the second substrate has an Si oxide layer on a surface to be bonded to the first substrate.

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34. The method according to any one of claims 25 to 31, characterized in that the second substrate comprises a transparent substrate.

35. A porous region removing apparatus for removing a porous region from a substrate having the porous region, characterized by comprising:

means for executing the first step of processing the porous region by an etchant while supplying an ultrasonic wave to the etchant;

means for executing the second step of processing the porous region by the etchant without supplying any ultrasonic wave to the etchant or while supplying an ultrasonic wave weaker than the ultrasonic wave supplied in the first step to the etchant; and

means for executing the third step of removing the porous region remaining on the substrate.

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ABSTRACT OF THE DISCLOSURE

This invention is to ensure a high planarity of an underlying layer after a porous layer is removed. A substrate to be processed is dipped in an etchant. In the first step, pores in the porous Si layer are filled with the etchant by supplying an ultrasonic wave. In the second step, supply of the ultrasonic wave is stopped, and the pore walls are thinned by the etching function. In the third step, the ultrasonic wave is supplied again to break the porous layer at once.

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FIG. 1A

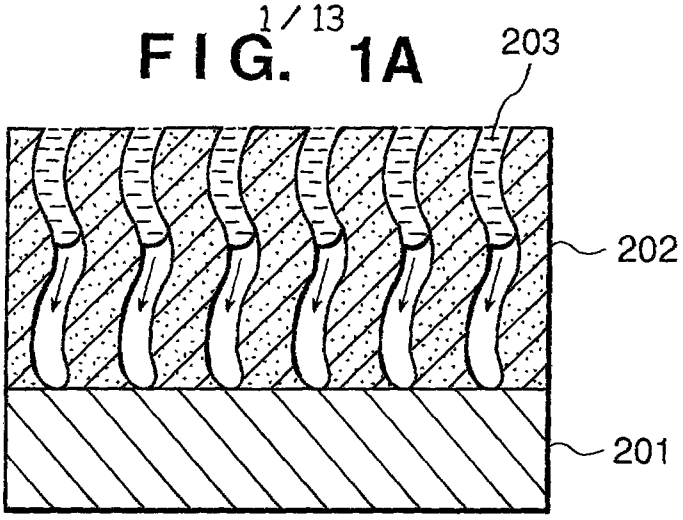


FIG. 1B

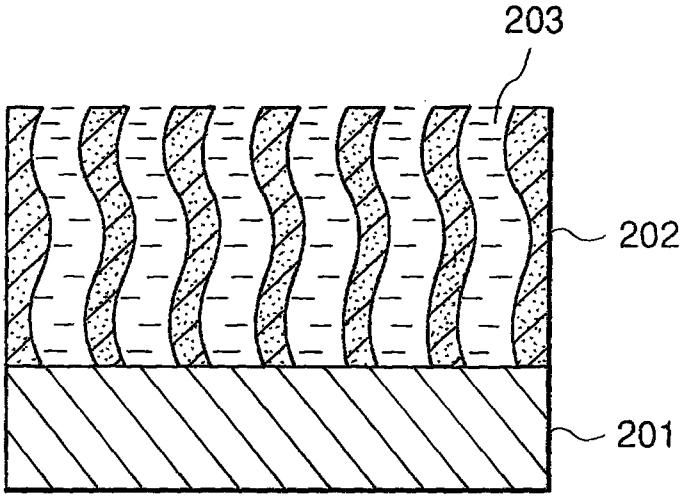


FIG. 1C

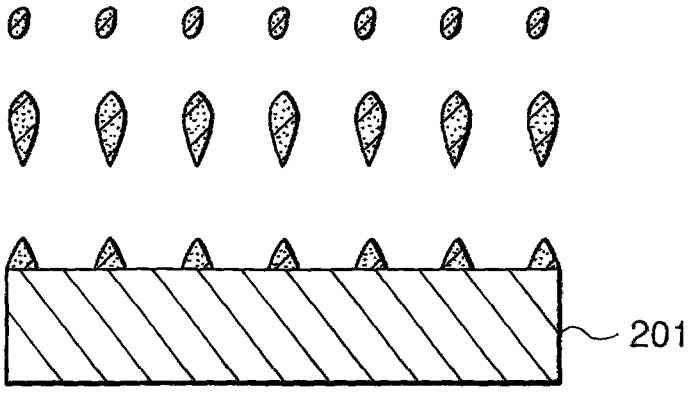


FIG. 2A

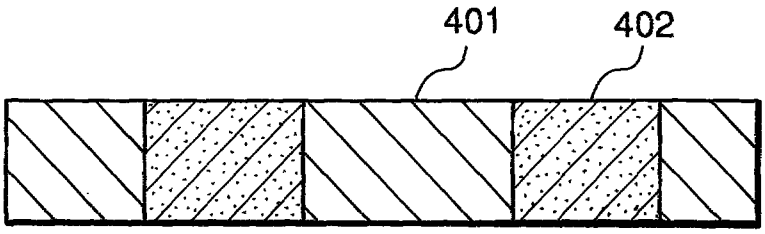


FIG. 2B

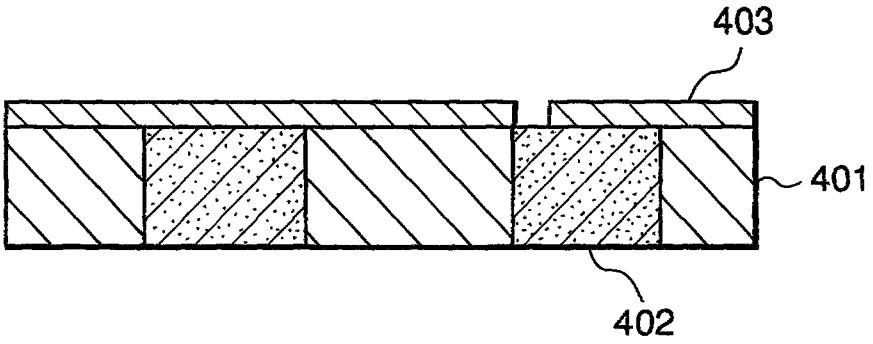


FIG. 2C

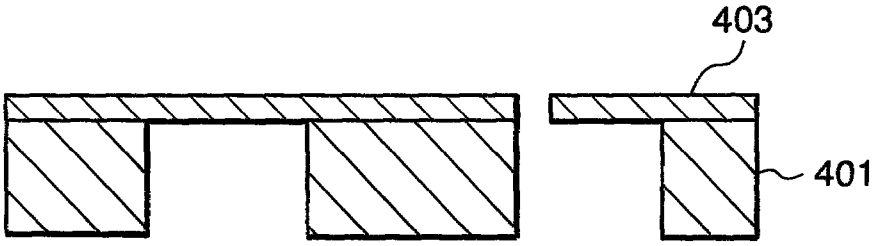


FIG. 3A

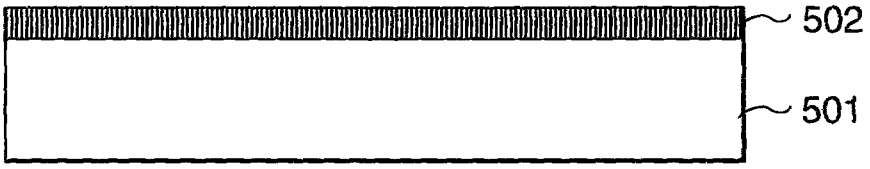


FIG. 3B

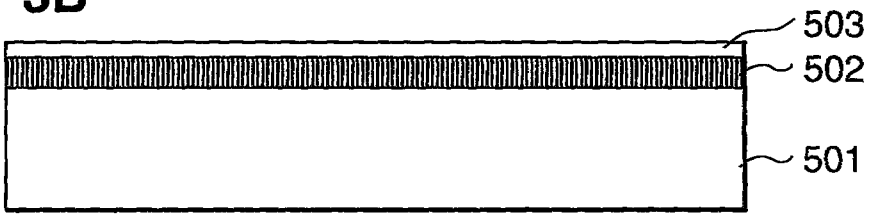


FIG. 3C

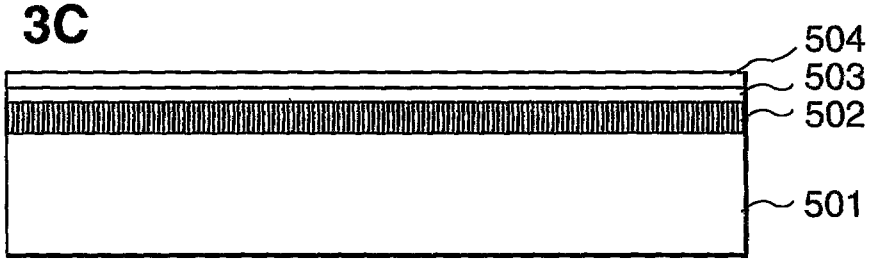


FIG. 3D

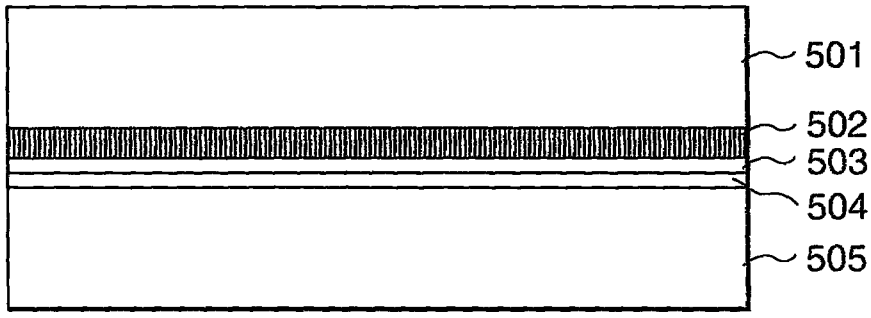


FIG. 3E

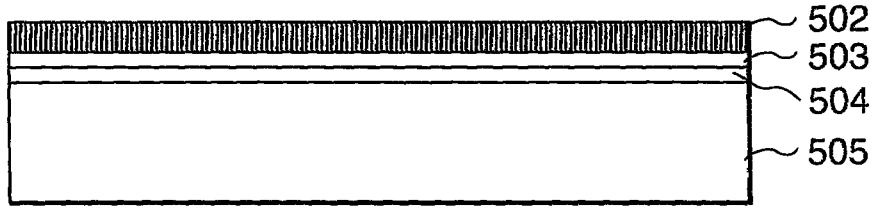


FIG. 3F

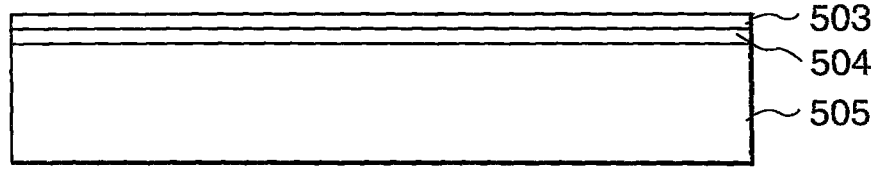


FIG. 4

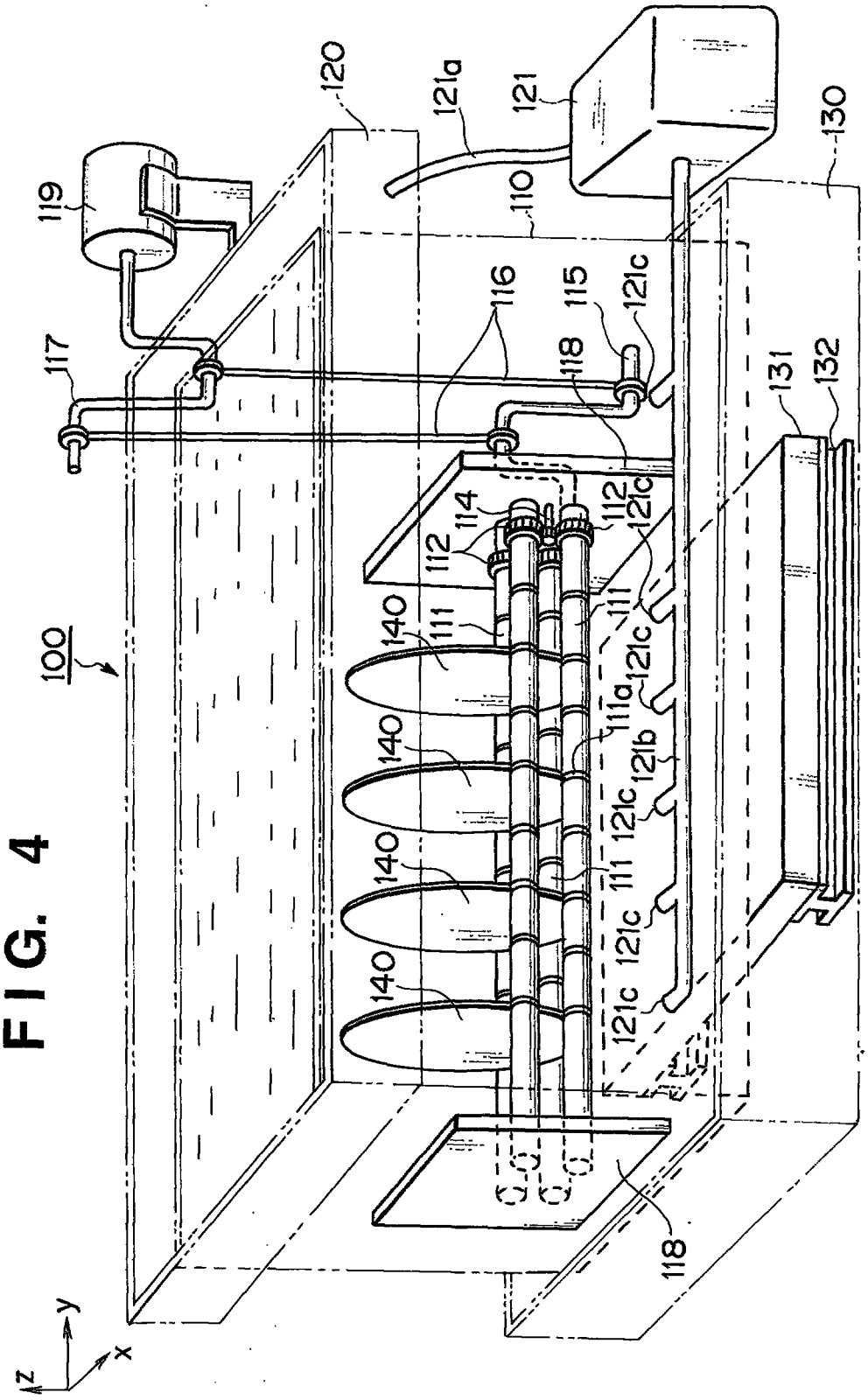

100
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y
z

FIG. 5

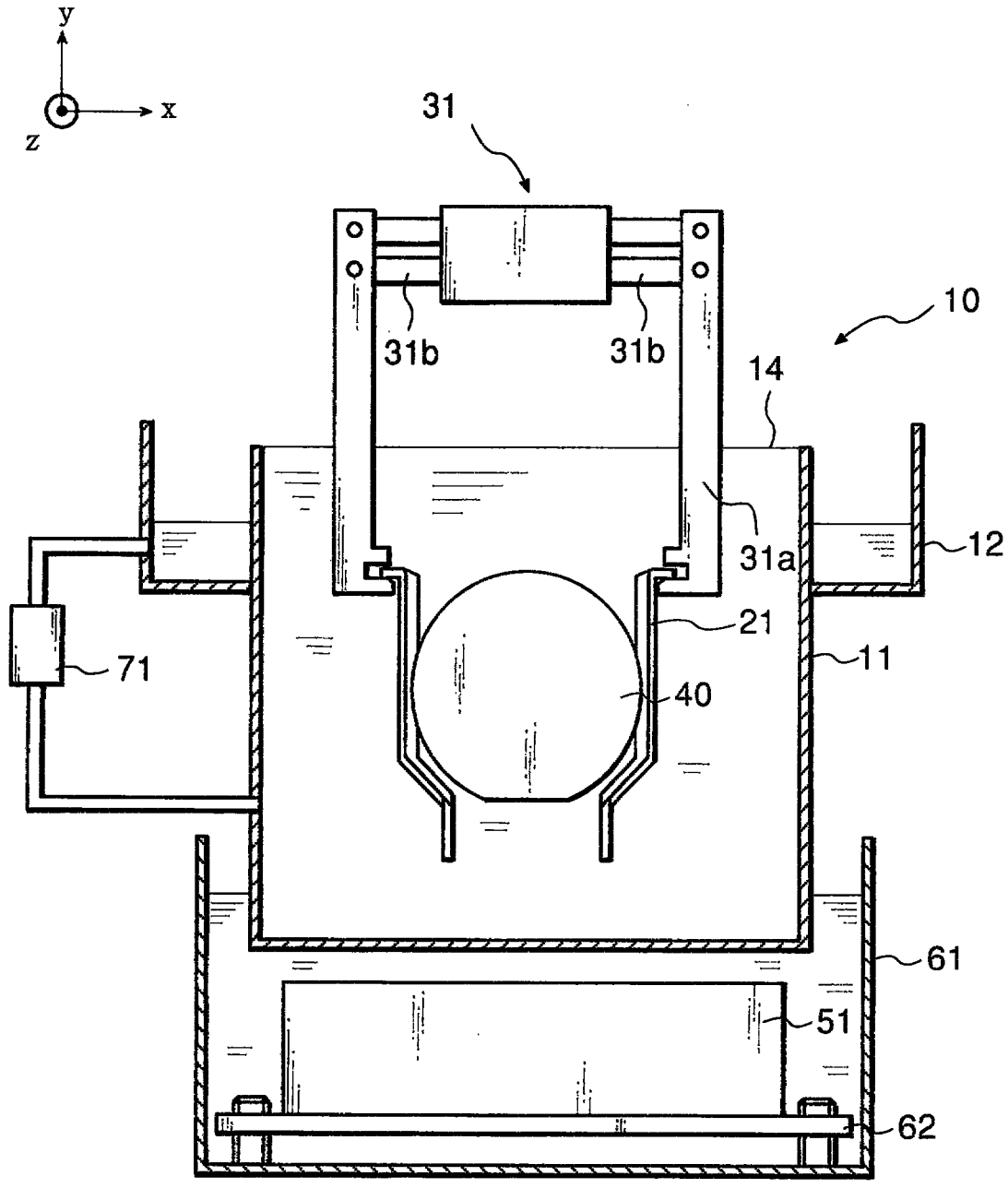


FIG. 6

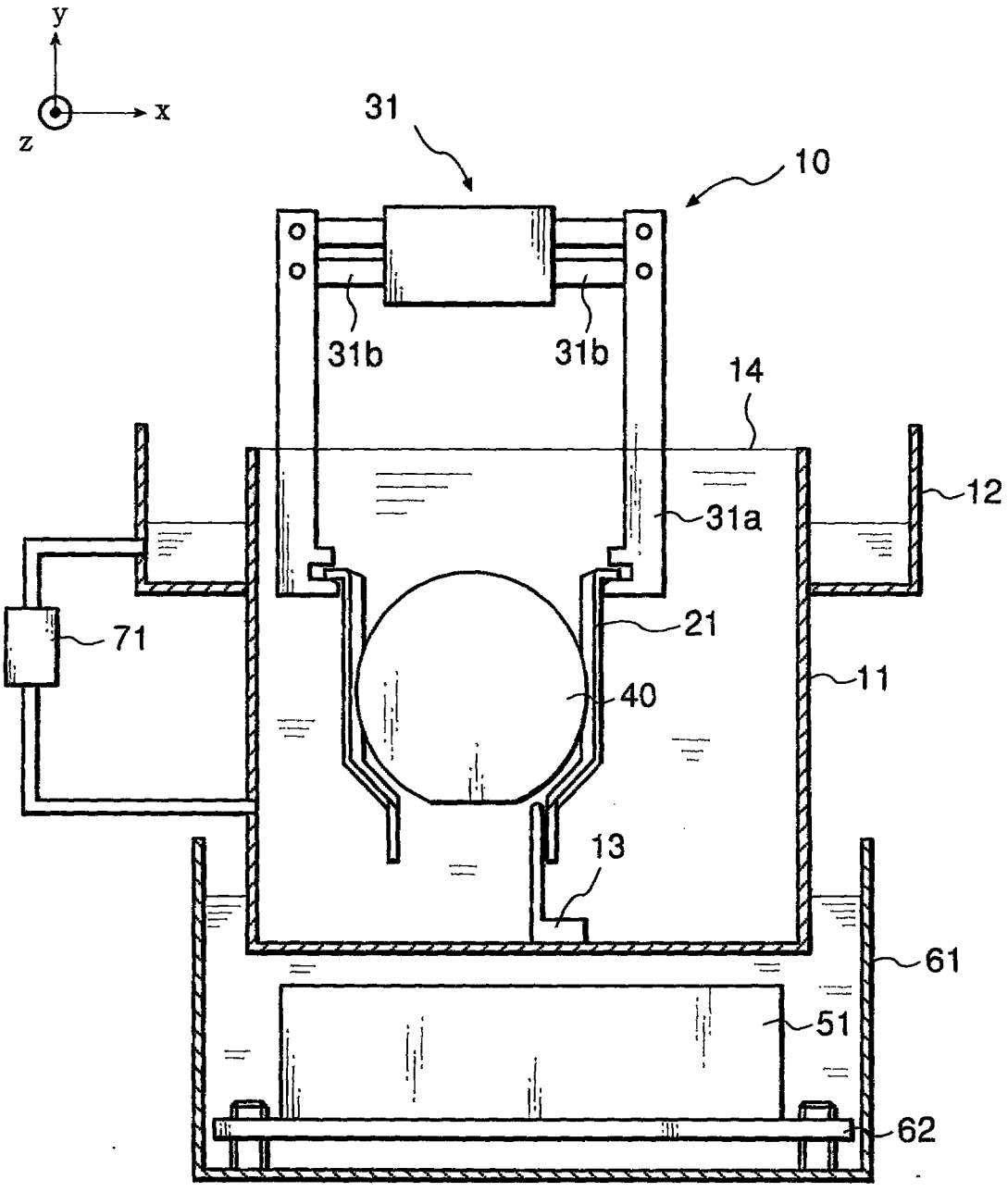


FIG. 7A

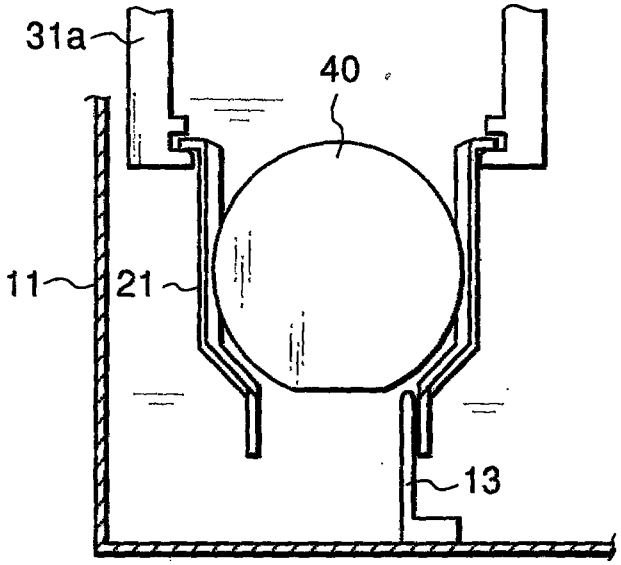


FIG. 7B

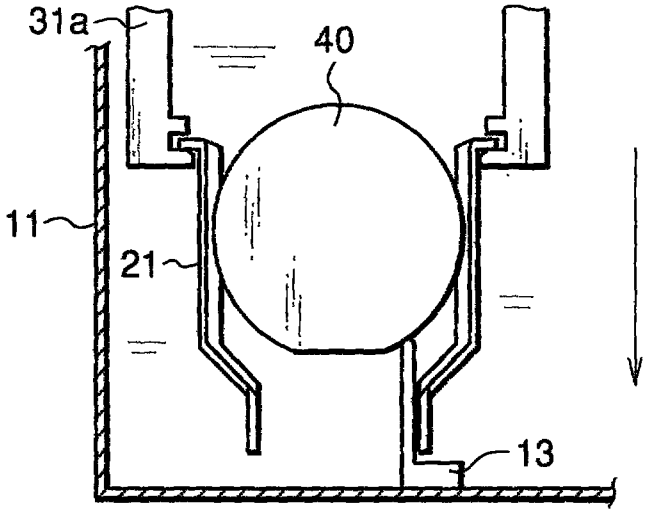


FIG. 7C

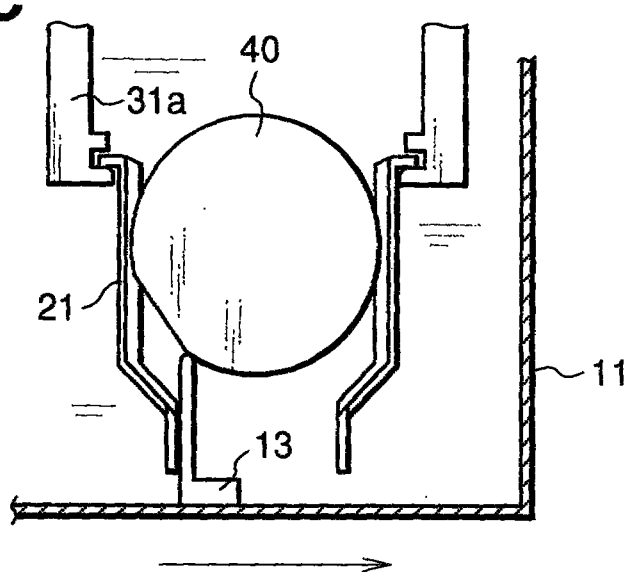


FIG. 7D

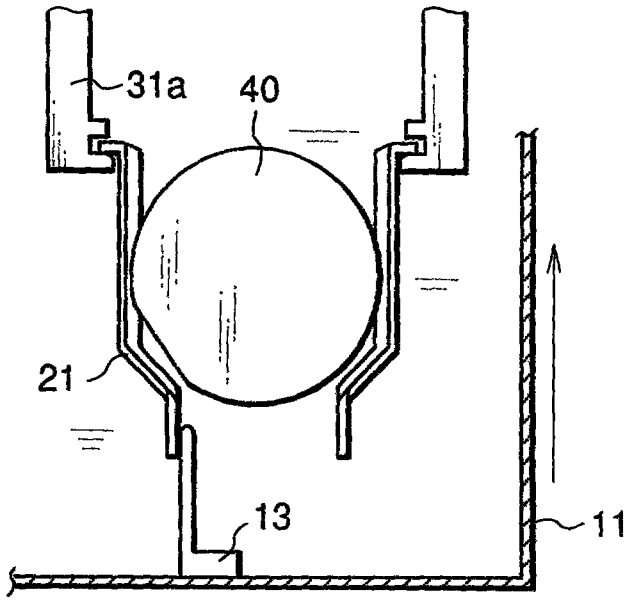


FIG. 7E

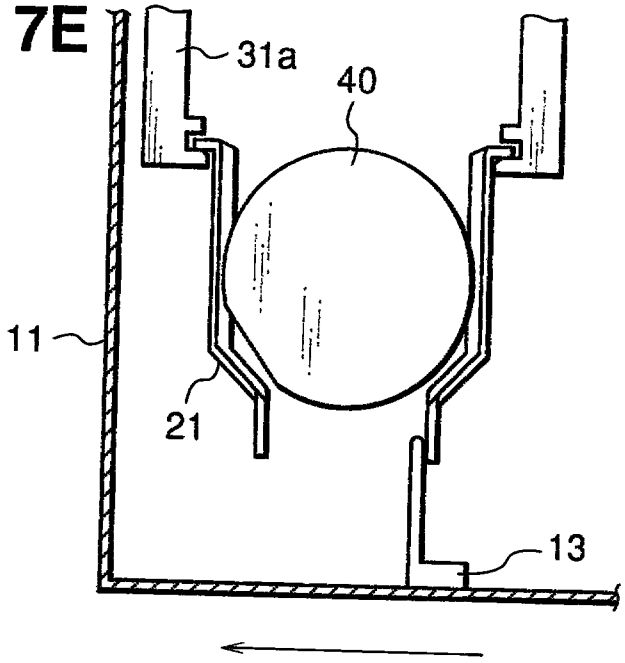


FIG. 8

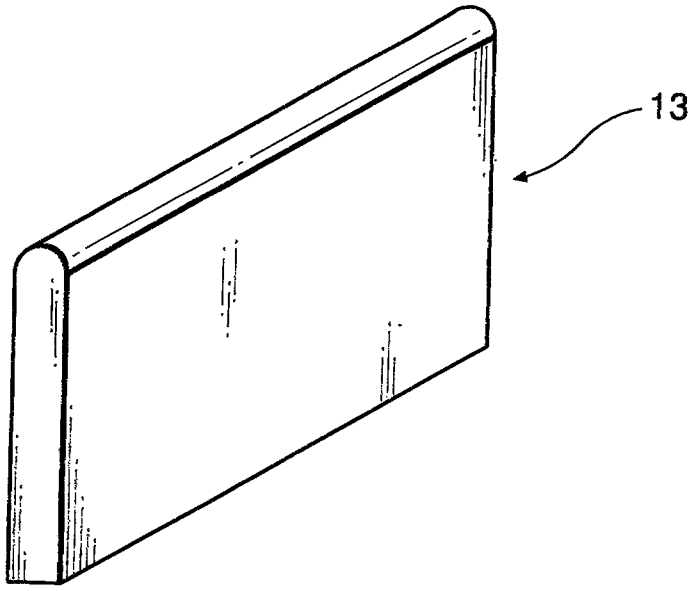


FIG. 9

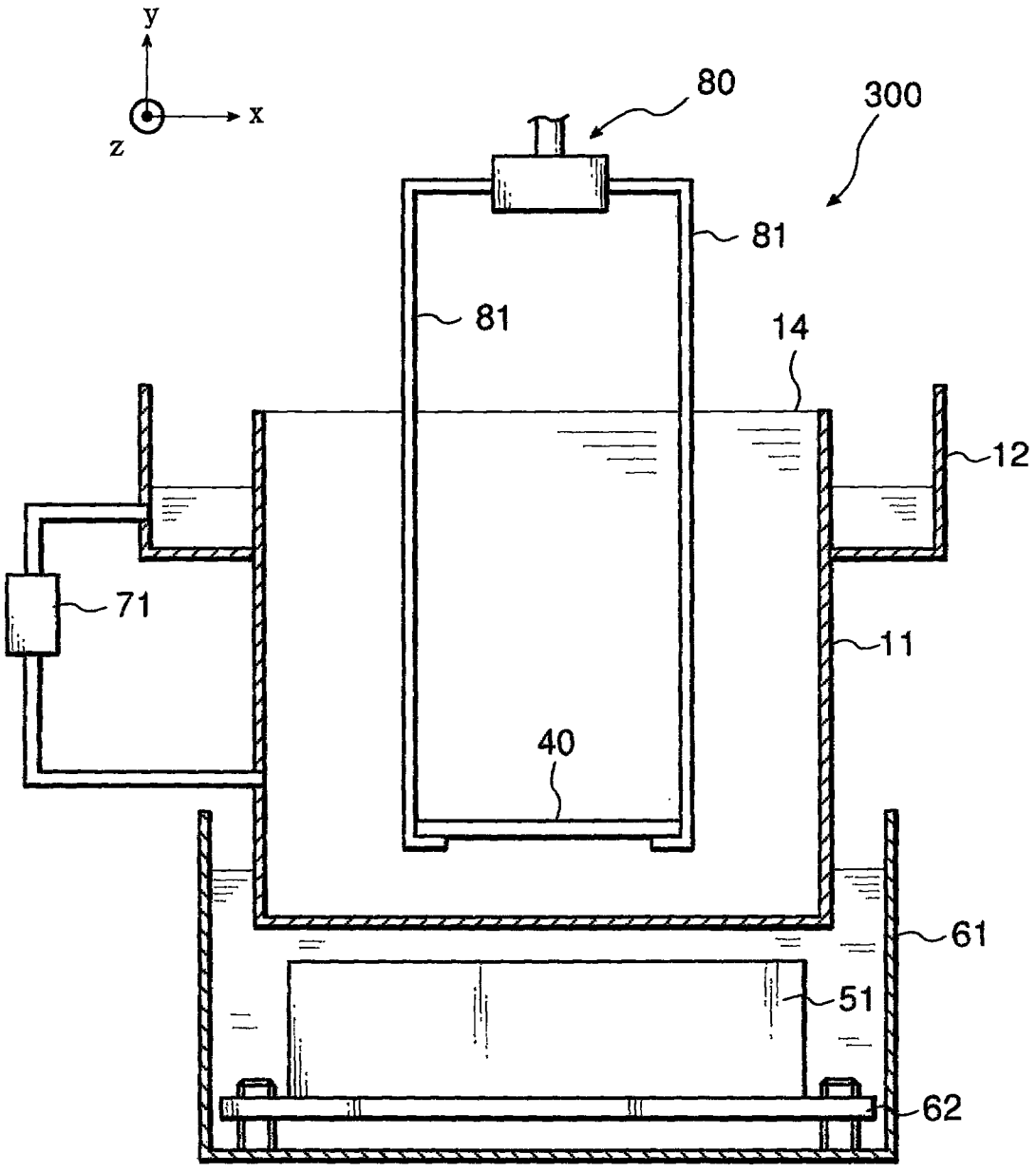


FIG. 10

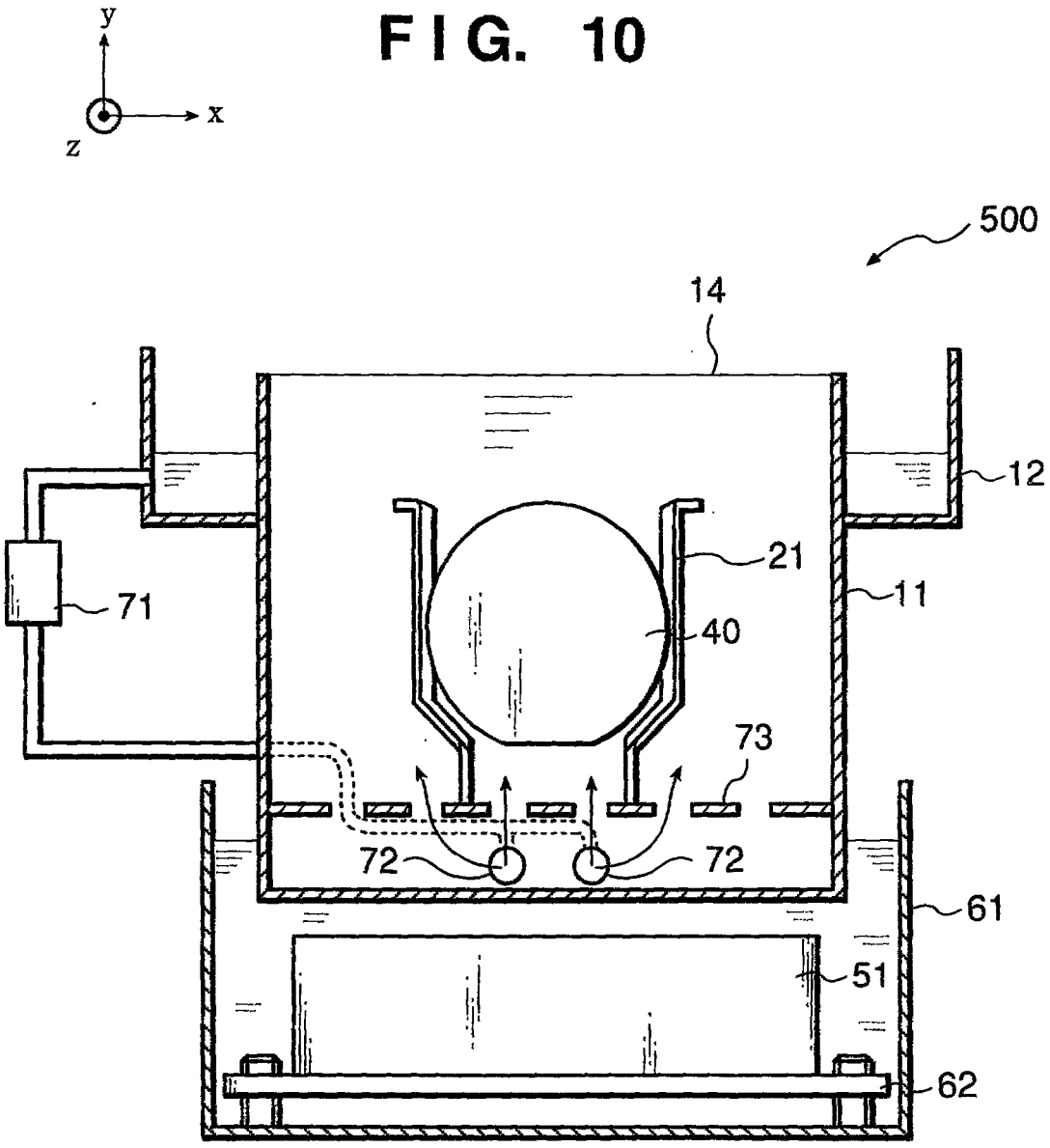


FIG. 11A

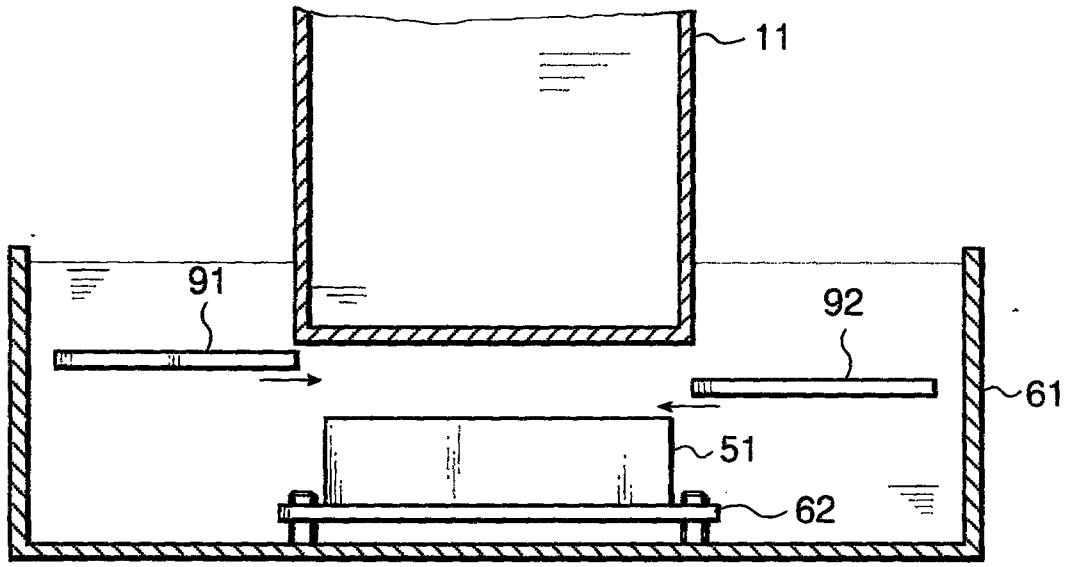


FIG. 11B

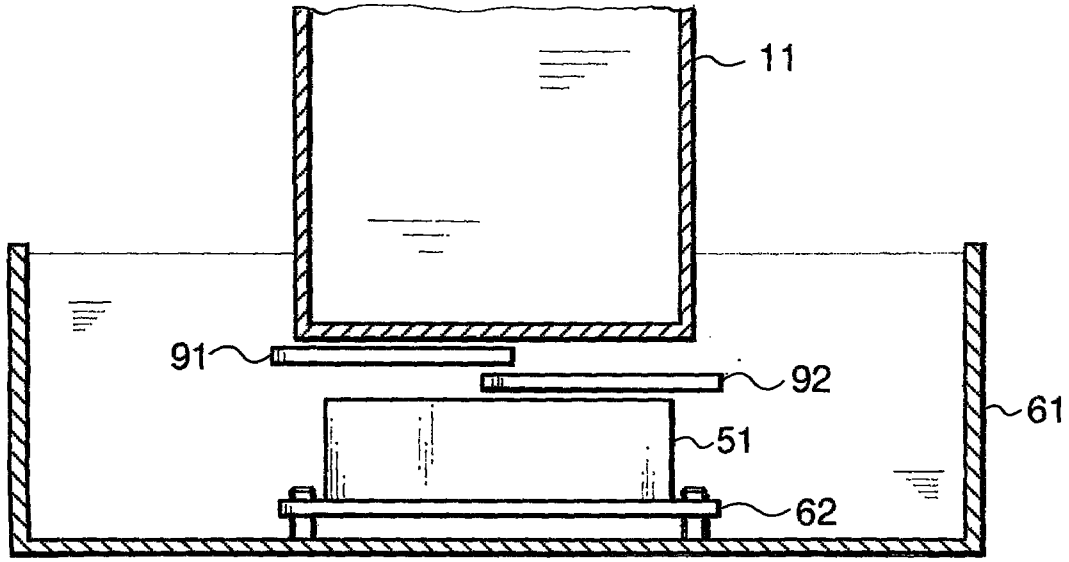


FIG. 12A

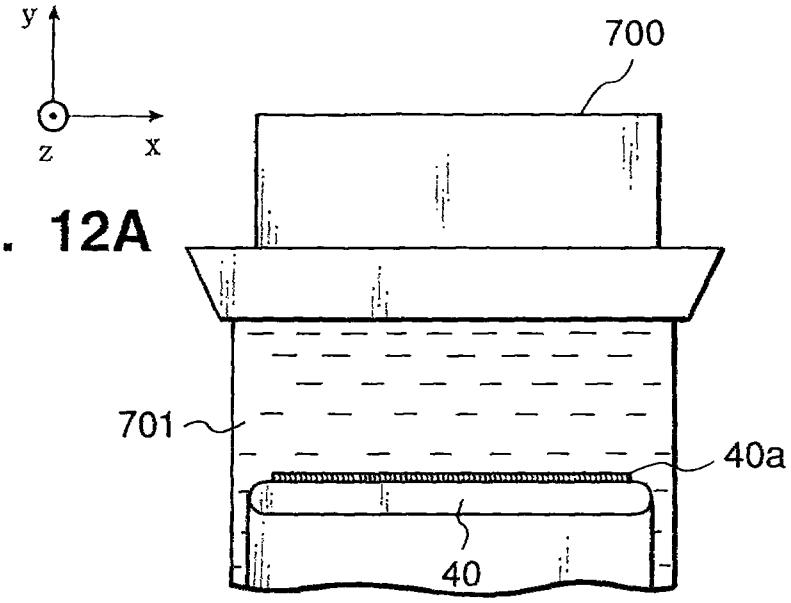


FIG. 12B

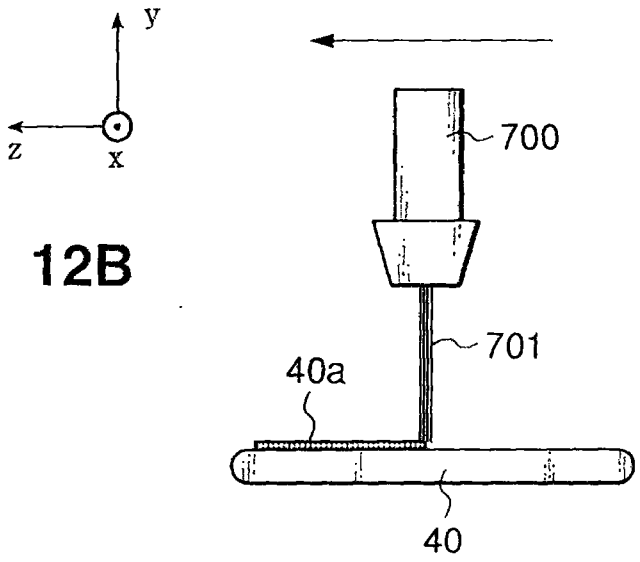
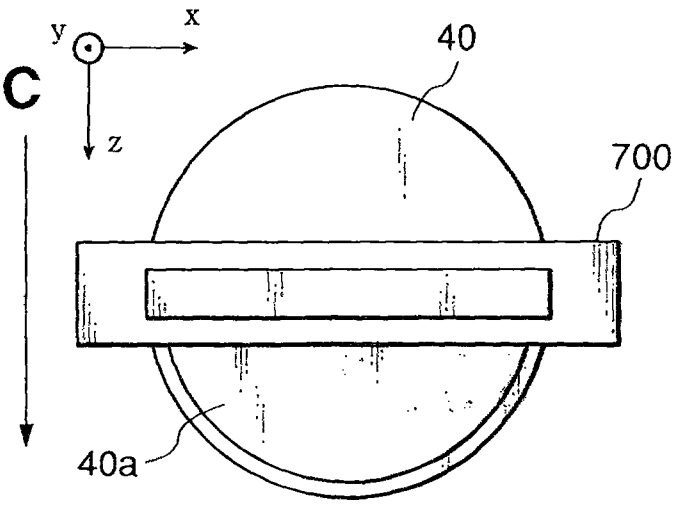


FIG. 12C



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Description : paged 1 to paged 48
Claim(s) : paged 49 to paged 56
Drawing(s) : paged ..... to paged .....
Abstract : paged 57 to paged 57
DATE OF RECEIPT 11·03·99

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11 MAR 1999
SG-9805829-0

TITLE OF THE INVENTION

POROUS REGION REMOVING METHOD AND SEMICONDUCTOR SUBSTRATE MANUFACTURING METHOD

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to a porous region removing method and a semiconductor substrate manufacturing method and, more particularly, to a method of removing a porous region from a substrate having the porous region, a semiconductor substrate manufacturing method using this method, and an apparatus for removing a porous region.

DESCRIPTION OF THE RELATED ART

There is a method of sequentially forming a porous Si layer and a single-crystal Si layer on a first substrate, bonding the first substrate to a separately prepared second substrate, and separating the bonded substrate stack into two substrates at the porous Si layer to transfer the single-crystal Si layer formed on the first substrate side to the second substrate side, thereby manufacturing an SOI substrate.

In this method, after the bonded substrate stack is separated into two substrates, the porous Si layer remaining

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on the surface on the second substrate side is removed. In removing the porous Si layer, the planarity of the surface of the underlying second substrate and, more particularly, film thickness uniformity of the single-crystal Si layer as the surface layer of the second substrate is preferably not hindered.

SUMMARY OF THE INVENTION

The present invention has been made in consideration of the above situation, and has as its object to provide a porous region removing method capable of maintaining a given planarity of an underlying layer and a semiconductor substrate manufacturing method using this method.

According to the present invention, there is provided a porous region removing method of removing a porous region from a substrate having the porous region, characterized by comprising the first step of processing the porous region by an etchant while supplying an ultrasonic wave to the etchant, the second step of processing the porous region by the etchant without supplying any ultrasonic wave to the etchant or while supplying an ultrasonic wave weaker than the ultrasonic wave supplied in the first step to the etchant, and the third step of removing the porous region remaining on the substrate.

In the porous region removing method, the first step

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preferably comprises filling pores in the porous region with the etchant to a deep portion.

In the porous region removing method, the second step preferably comprises thinning pore walls in the porous region to not more than a predetermined thickness by an etching function.

In the porous region removing method, the second step preferably comprises thinning the pore walls in the porous region to a thickness that allows removal of the remaining porous region at once in the third step.

In the porous region removing method, the third step preferably comprises removing the porous region remaining on the substrate by the etchant.

In the porous region removing method, the third step preferably comprises removing the porous region remaining on the substrate by the etchant while supplying the ultrasonic wave to the etchant.

In the porous region removing method, the first to third steps are preferably executed while dipping the substrate to be processed in the same etchant.

In the porous region removing method, the third step preferably comprises removing the porous region remaining on the substrate by an etchant whose etching rate for the porous region is higher than that of the first or second etchant.

In the porous region removing method, the first to third

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steps are preferably executed while completely dipping the substrate to be processed in the etchant.

In the porous region removing method, the first and/or second steps is preferably executed while completely dipping the substrate to be processed in the etchant.

In the porous region removing method, the third step preferably comprises removing the porous region remaining on the substrate by a high-pressure fluid.

In the porous region removing method, the third step preferably comprises removing the porous region remaining on the substrate by scrubbing.

In the porous region removing method, in processing the substrate while supplying the ultrasonic wave to the etchant, a relative positional relationship between an ultrasonic source and the substrate is preferably changed.

In the porous region removing method, in processing the substrate while supplying the ultrasonic wave to the etchant, the substrate is preferably swung in the etchant.

In the porous region removing method, in processing the substrate while supplying the ultrasonic wave to the etchant, the substrate is preferably rotated.

In the porous region removing method, in processing the substrate while supplying the ultrasonic wave to the etchant, a position of at least one of the substrate and the ultrasonic source is preferably changed substantially in a direction parallel or perpendicular to a vibration plane of the

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ultrasonic wave.

In the porous region removing method, in processing the substrate by the etchant, the substrate is preferably swung or rotated.

In the porous region removing method, in processing the substrate by the etchant, the etchant is preferably circulated to form a flow of etchant near the substrate.

In the porous region removing method, preferably, the first and second steps are executed while dipping the substrate in the same etching tank, the first step comprises operating the ultrasonic source, and the second step comprises stopping operation of the ultrasonic source.

In the porous region removing method, preferably, the first and second steps are executed while dipping the substrate in the same etching tank, the first and second steps comprise continuously operating the ultrasonic source, and the second step comprises inserting an ultrasonic shielding plate between the ultrasonic source and the substrate.

In the porous region removing method, the substrate to be processed preferably essentially consists of single-crystal Si.

In the porous region removing method, the porous region preferably essentially consists of porous Si.

In the porous region removing method, the porous region is preferably formed by anodizing a single-crystal Si substrate.

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In the porous region removing method, preferably, as the etchant, any one of

(a) fluoric acid,

(b) a mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to fluoric acid,

(c) buffered fluoric acid, and

(d) a mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to buffered fluoric acid

is used.

According to the present invention, there is also provided a semiconductor substrate manufacturing method characterized by comprising the steps of forming a porous layer and at least one non-porous layer on a first substrate, bonding a second substrate to the non-porous layer side of the first substrate, removing the first substrate from the bonded substrate stack to expose the porous layer on a surface of the second substrate, and removing the porous layer on the second substrate using the above porous region removing method.

In the porous region removing method, the step of exposing the porous layer preferably comprises grinding, polishing, or etching the first substrate from a lower surface side of the first substrate of the bonded substrate stack, thereby exposing the porous layer on the surface of the second substrate.

In the porous region removing method, the step of

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exposing the porous layer preferably comprises dividing the bonded substrate stack at the porous layer, thereby exposing the porous layer on the surface of the second substrate.

In the porous region removing method, the non-porous layer preferably includes a single-crystal Si layer.

In the porous region removing method, the non-porous layer preferably includes a single-crystal Si layer and an Si oxide layer.

In the porous region removing method, the single-crystal Si layer is preferably epitaxially grown on the porous layer on the first substrate.

In the porous region removing method, the non-porous layer preferably includes a single-crystal compound semiconductor layer.

In the porous region removing method, the second substrate preferably essentially consists of an Si material.

In the porous region removing method, the second substrate preferably has an Si oxide layer on a surface to be bonded to the first substrate.

In the porous region removing method, the second substrate preferably comprises a transparent substrate.

According to the present invention, there is also provided a porous region removing apparatus for removing a porous region from a substrate having the porous region, characterized by comprising means for executing the first step of processing the porous region by an etchant while

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supplying an ultrasonic wave to the etchant, means for executing the second step of processing the porous region by the etchant without supplying any ultrasonic wave to the etchant or while supplying an ultrasonic wave weaker than the ultrasonic wave supplied in the first step to the etchant, and means for executing the third step of removing the porous region remaining on the substrate.

Further objects, features and advantages of the present invention will become apparent from the following detailed description of embodiments of the present invention with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1C are views for explaining the principle of a porous layer removing method according to a preferred embodiment of the present invention;

Figs. 2A to 2C are views showing a fabrication method according to the first application example of the porous layer removing method;

Figs. 3A to 3F are views showing a semiconductor substrate manufacturing method according to another preferred embodiment of the present invention;

Fig. 4 is a perspective view showing the first arrangement of a wafer processing apparatus;

Fig. 5 is a perspective view showing the second

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arrangement of the wafer processing apparatus;

Fig. 6 is a perspective view showing the third arrangement of the wafer processing apparatus;

Fig. 7A is a view showing operation of the wafer processing apparatus shown in Fig. 6;

Fig. 7B is a view showing operation of the wafer processing apparatus shown in Fig. 6;

Fig. 7C is a view showing operation of the wafer processing apparatus shown in Fig. 6;

Fig. 7D is a view showing operation of the wafer processing apparatus shown in Fig. 6;

Fig. 7E is a view showing operation of the wafer processing apparatus shown in Fig. 6;

Fig. 8 is a perspective view of a swing assist member in the wafer processing apparatus shown in Fig. 6;

Fig. 9 is a view showing the fourth arrangement of the wafer processing apparatus;

Fig. 10 is a view showing the fifth arrangement of the wafer processing apparatus;

Figs. 11A and 11B are views showing a modification of the wafer processing apparatus shown in Fig. 5 or 6; and

Figs. 12A to 12C are views showing the seventh arrangement of the wafer processing apparatus.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

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The present invention is suitable for a method of sequentially forming a porous layer and a non-porous layer on a first substrate, bonding the first substrate to a separately prepared second substrate, separating the bonded substrate stack into two substrates at the porous layer to transfer the non-porous layer formed on the first substrate side to the second substrate side, and removing the porous layer remaining on the surface on the second substrate side, thereby manufacturing an SOI substrate.

As the first substrate, a single-crystal Si substrate can be used. In this case, the porous layer is a porous Si layer. On the porous Si layer, a single-crystal Si layer can be epitaxially grown as a non-porous layer. An insulating layer such as an SiO_2 layer may be formed on the single-crystal Si layer.

In the embodiment, the first substrate on which the porous Si layer and the non-porous layer are sequentially formed is bonded to the separately prepared second substrate to form a bonded substrate stack. After the bonded substrate stack is separated into two substrates at the porous Si layer, the porous Si layer remaining on the second substrate side is removed by, e.g., wet etching.

In etching the porous Si layer, break of the porous Si layer can be prompted by supplying an ultrasonic wave to the etching tank. More specifically, when an ultrasonic wave is supplied into the etching tank, and more specifically, to

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the bonded substrate stack during etching, pore walls in the porous Si layer can be broken before they become thin. Since the time from the start to the end of break of pore walls in the porous Si layer can be greatly shortened, the etching selectivity ratio between the porous layer and the underlying second substrate (e.g., a single-crystal Si substrate) can be increased. Hence, SOI thickness variations in surface of the second substrate and SOI thickness variations between the substrates after removal of the porous layer are suppressed, and a high-quality SOI substrate having a single-crystal Si layer with high film thickness uniformity can be obtained.

However, if the porous layer on the substrate to be etched has variations in thickness, it may be difficult to ensure high film thickness uniformity of the surface layer (single-crystal Si layer) of the second substrate after removal of the porous Si layer. Especially in mass production, this problem may result in a low yield.

In this embodiment, a method of more properly ensuring high film thickness uniformity of the surface layer (single-crystal Si layer) of the second substrate after removal of the porous Si layer is provided.

Figs. 1A to 1C are views for explaining the principle of a porous layer removing method according to a preferred embodiment of the present invention. Referring to Figs. 1A to 1C, reference numeral 201 denotes an underlying substrate

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(second substrate); 202, a porous layer; and 203, an etchant.

In Fig. 1A, the pores of the porous layer 202 are filled with the etchant 203 to the deepest portions. At this time, an ultrasonic wave is preferably supplied to the object (e.g., a bonded substrate stack) to be processed. When an ultrasonic wave is supplied, the speed at which the pores are filled with the etchant increases.

In Fig. 1B, the pores grow by the etching function. At this time, preferably, no ultrasonic wave is supplied to the object to be processed, or the ultrasonic strength is reduced. If an ultrasonic wave is supplied, the porous layer starts to break as soon as the walls between adjacent pores become thin to some degree as the pores grow. Since the porous layer breaks first at thin portions, the surface of the underlying substrate 201 is etched in these portions. In this case, obviously film thickness uniformity of the surface layer of the substrate 201 degrades. However, when no ultrasonic wave is supplied, the pores do not break unless they become much thinner than in a case wherein an ultrasonic wave is supplied. In this case, therefore etching can be prevented from locally excessively progressing.

Even when no ultrasonic wave is supplied to the object to be processed, etching progresses not only in the horizontal direction (planar direction) but also in the vertical direction. However, the influence on etching is negligible compared to the case wherein an ultrasonic wave

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is supplied.

In Fig. 1C, the porous layer 202 with thin pore walls is removed. Not only etching but also polishing, scrubbing, or the water jet method can be applied to this step. In this step, the porous layer having a fragile structure upon etching is removed at once.

When etching is applied to the step shown in Fig. 1C, the steps in Figs. 1A to 1C can be executed using the same etching tank. In this case, the step shown in Fig. 1B is executed until pore walls at the deepest portion of the porous layer are thinned to immediately break in the entire region upon resupply of an ultrasonic wave, and then, the step in Fig. 1C is executed (supply of an ultrasonic wave). With this process, the porous layer can be removed at once, and almost simultaneously, the underlying substrate 201 can be exposed in the entire region of the object to be processed. For this reason, variations in etching can be reduced, and a given planarity of the underlying substrate 201 can be maintained.

The above porous layer removing method can be easily applied to batch processing of a number of substrates. More specifically, for each of a number of objects to be processed, after the pore walls at the deepest portion of the porous layer are thinned to allow immediate break in the entire region in the step shown in Fig. 1B, the step shown in Fig. 1C is executed.

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This porous layer removing method is preferably practiced while completely dipping the object to be processed in the etchant. In this case, particles can be prevented from sticking to the object to be processed near the interface between the etchant and air.

According to this porous layer removing method, by supplying an ultrasonic wave, etching is prompted to break the porous layer, and particles can be efficiently removed from the object to be processed.

When the porous layer is removed while changing the relative positional relationship between the ultrasonic source (e.g., an ultrasonic vibrator) and the object to be processed and, more specifically, the positional relationship between the substrate and a standing wave generated between the ultrasonic vibration surface and the liquid surface of the etchant, processing can be uniformly performed in all regions of the substrate surface. To do this, for example, the substrate is rotated, the substrate is swung, a carrier holding the substrate is swung, or the ultrasonic source is moved.

Application examples of the porous layer removing method will be described below.

(First Application Example)

The first application example is associated with an object fabrication method. Figs. 2A to 2C are views showing the fabrication method of this application example. In

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Fig. 2A, an Si substrate 401 locally having porous Si portions 402 is prepared. The Si substrate 401 is obtained by, e.g., forming a resist film on the Si substrate, patterning the resist film by lithography, and anodizing the resultant structure. In place of the resist film, a patterned Si_3N_4 film or wax may be employed. As this wax, wax having fluoric acid resistance, e.g., Apizoen wax (trade name) can be used.

In Fig. 2B, a non-porous layer (pattern) 403 is formed on the surface of the Si substrate shown in Fig. 2A.

In Fig. 2C, the porous Si portions 402 are removed. More specifically, first, the substrate shown in Fig. 2B, with the porous Si portions 402 exposed, is set in an etching apparatus having an etching tank filled with an etchant for porous Si, and etching is performed while supplying an ultrasonic wave.

When the pores of the porous Si portions 402 are sufficiently filled with the etchant, supply of the ultrasonic wave is stopped, and etching is continued. In this process, the pore walls in the porous Si portions 402 gradually thin. The color of porous Si portions 402 also gradually becomes lighter when viewed from the surface (lower side of the drawing). When the pore walls have sufficiently thinned, the underlying non-porous layer (pattern) 403 can be seen through the porous Si portions 402.

In this state, the remaining porous Si portions are

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removed. To remove the porous Si portions, for example, 1) etching is performed while resupplying an ultrasonic wave, or 2) etching is performed using an etchant with high Si etching rate.

To leave a hard structure, the porous Si portions may be removed by a jet of water.

When the entire Si substrate 401 is made of porous Si, only the non-porous layer formed on the substrate can be left. In addition, when the non-porous layer 403 is patterned, as described above, various structures including a cantilever shown in Fig. 2C can be formed.

(Second Application Example)

The second application example is associated with a semiconductor substrate manufacturing method. Figs. 3A to 3F show the semiconductor substrate manufacturing method of this application example. In Fig. 3A, a first single-crystal Si substrate 501 is prepared, and a porous Si layer 502 is formed on one surface of the first single-crystal Si substrate 501. In Fig. 3B, at least one non-porous layer 503 is formed on the porous Si layer 502. As the non-porous layer 503, a single-crystal Si layer, a polycrystalline Si layer, an amorphous Si layer, a metal layer, a compound semiconductor layer, or a superconductor layer is suitable. As the non-porous layer 503, a layer including a device structure such as a MOSFET may be formed. An SiO_2 layer 504 is preferably formed on the surface layer, thus completing

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the first substrate. This SiO_2 layer 504 is useful also because when the first substrate is bonded to a second substrate 505, the interface states of the bonding interface can be separated from the active layer.

Subsequently, as shown in Fig. 3D, the separately prepared second substrate 505 is brought into contact with the first substrate shown in Fig. 3C at room temperature via the SiO_2 layer 504. After this, anode bonding, pressing, a heat treatment as needed, or a combination thereof is performed to firmly bond the substrates.

When a single-crystal Si layer is formed as the non-porous layer 503, the first substrate is preferably bonded to the second substrate 505 after the SiO_2 layer 504 is formed on the surface of the single-crystal Si layer by, e.g., thermal oxidation.

As the second substrate 505, an Si substrate, a substrate obtained by forming an SiO_2 layer on an Si substrate, a transparent substrate consisting of silica glass or quartz, or a sapphire substrate is suitable. Any other substrate can be used as far as the second substrate 505 has a sufficiently flat surface to be bonded.

Fig. 3D shows a state wherein the first substrate and the second substrate are bonded via the SiO_2 layer 504. If the non-porous layer 503 or the second substrate does not consist of Si, the SiO_2 layer 504 need not be formed.

In bonding, an insulating thin plate may be inserted

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between the first and the second substrates.

In Fig. 3E, the first Si substrate 501 is removed from the second substrate side at the porous Si layer 502. To remove the first substrate, either the first substrate side is discarded by grinding, polishing, or etching, or the bonded substrate stack is separated into the first substrate side and the second substrate at the porous Si layer 502.

In Fig. 3F, the porous Si layer 502 remaining on the surface on the second substrate side is removed. More specifically, first, the second substrate side is set in an etching tank filled with a porous Si etchant, and etching is performed while supplying an ultrasonic wave.

When the pores of the porous Si portions are sufficiently filled with the etchant, supply of the ultrasonic wave is stopped, and etching is continued. In this process, the pore walls in the porous Si layer 502 gradually thin. The color of porous Si layer 502 also gradually becomes lighter when viewed from the surface. When the pore walls have sufficiently thinned, the underlying non-porous layer (e.g., a single-crystal Si layer) 503 can be seen through the porous Si layer 502.

In this state, the remaining porous Si layer 502 is removed. To remove the porous Si layer, for example, 1) etching is performed while resupplying an ultrasonic wave, 2) etching is performed using an etchant with high Si etching rate, 3) the porous Si layer 502 is removed by a jet of water,

4) the porous Si layer 502 is polished, or 5) scrubbing is performed.

Fig. 3F is a view schematically showing a semiconductor substrate (SOI substrate) obtained by the above method. The non-porous layer (e.g., a single-crystal Si layer) 503 with a flat surface and uniform film thickness is formed on the second substrate 505 via the insulating layer (e.g., an Sio_2 layer) 504. According to this method, a large-area semiconductor substrate having high quality can be manufactured.

When an insulating substrate is employed as the second substrate 505, the semiconductor substrate obtained by the above manufacturing method is very useful to form an insulated electronic device.

When the bonded substrate stack shown in Fig. 3D is divided at the porous Si layer 502, the first substrate can be reused after the porous Si layer 502 remaining on the first substrate 501 is removed, and the surface is planarized, as needed.

Specific examples of a wafer processing apparatus suitable to remove a porous layer will be listed below.

(First Arrangement of Processing Apparatus)

Fig. 4 is a perspective view showing the schematic arrangement of a wafer processing apparatus suitable to remove a porous layer.

In a wafer processing apparatus 100, members which may

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come into contact with the process solution are preferably made of silica glass or a plastic in accordance with their application purposes. As the plastic, a fluoroplastic, vinyl chloride, polyethylene, polypropylene, polybutylene terephthalate (PBT), or polyether ether ketone (PEEK) can be used. As the fluoroplastic, PVDF, PFA, or PTFE is suitable.

The wafer processing apparatus 100 comprises a wafer processing tank 110, an overflow tank 120, an ultrasonic tank 130, and a wafer rotating mechanism (111 to 119) for supporting wafers 140 while rotating them.

Before processing wafers, the wafer processing tank 110 is filled with a process solution (etchant). The overflow tank 120 for temporarily storing the process solution overflowing from the wafer processing tank 110 is mounted on the upper portion the wafer processing tank 110 to surround it. The process solution temporarily stored in the overflow tank 120 is discharged from the bottom portion of the overflow tank 120 to a circulator 121 through a discharge pipe 121a. The circulator 121 filters the discharged process solution to remove particles and sends the process solution to the bottom portion of the wafer processing tank 110 through a supply pipe 121b. With this arrangement, particles in the wafer processing tank 110 are efficiently removed.

The wafer processing tank 110 preferably has a depth with which the wafers 140 can be completely immersed. With

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this arrangement, particles in the air or near the liquid surface can be prevented from adhering to the wafers 140.

The ultrasonic tank 130 is located under the wafer processing tank 110. Inside the ultrasonic tank 130, an ultrasonic source 131 is supported by an adjustment mechanism 132. The adjustment mechanism 132 has, as mechanisms for adjusting the relative positional relationship between the ultrasonic source 131 and the wafer processing tank 110 has a mechanism, a mechanism for adjusting the vertical position of the ultrasonic source 131 and a mechanism for adjusting the horizontal position. With this mechanism, the ultrasonic wave to be supplied into the wafer processing tank 110 and, more specifically, to the wafers 140 can be optimized. The ultrasonic source 131 preferably has a function of adjusting the frequency or strength of the generated ultrasonic wave. With this arrangement, supply of an ultrasonic wave can be further optimized. By imparting the function of optimizing supply of an ultrasonic wave to the wafers 140, the ultrasonic wave can be supplied individually to a variety of types of wafers. The ultrasonic tank 130 is filled with an ultrasonic transmission medium (e.g., water), so the ultrasonic wave is transmitted to the wafer processing tank 110 through the ultrasonic transmission medium.

The wafer processing apparatus 100 has a control section for ON/OFF-controlling the ultrasonic source 131. With this control section, porous layer removing processing can be

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controlled.

The wafers 140 are held to be almost perpendicular to the bottom surface of the wafer processing tank 110 by four wafer rotary rods 111 each having grooves 111a engaging with the wafers 140. The wafer rotary rods 111 have a function of supporting the wafers 140 while rotating them and constitute part of the wafer rotating mechanism. Each wafer rotary rod 111 is pivotally supported by a pair of rod support members 118 opposite to each other, so the wafer rotary rods 111 rotate in the same direction upon receiving a driving torque generated by a motor 119. Each wafer rotary rod 111 preferably has a small diameter not to impede transmission of the ultrasonic wave.

The number of wafer rotary rods 111 is preferably as small as possible. To ensure a desired frictional force with respect to the wafers 140, preferably, two wafer rotary rods 111 for limiting movement in the rolling direction (X-axis direction) of the wafers 140, and two wafer rotary rods 111 for supporting the wafers 140 from the lower side are provided. When two wafer rotary rods 111 are disposed at an appropriate interval below the wafers, the driving torque can be efficiently transmitted to the wafers having an orientation flat. If only one wafer rotary rod 111 is placed underneath the wafers, and the orientation flat is positioned above this wafer rotary rod 111, the wafers cannot be rotated by the wafer rotary rod 111.

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Normally, a standing wave, i.e., an ultrasonic wave having a high-strength portion and a low-strength portion is formed between the bottom surface of the wafer processing tank 110 and the liquid surface. However, since this wafer processing apparatus 100 can process the wafers 140 while rotating them, nonuniformity in processing due to the standing wave can be reduced.

In the wafer processing apparatus 100, the number of members on the bottom portion of the wafer processing tank 110 or around the wafers 140 is decreased as small as possible. For this reason, the ultrasonic wave can be efficiently and uniformly supplied to the wafers 140. In addition, with this arrangement, since the process solution can freely flow around the wafers 140, the wafers can be uniformly processed, and processing defects can be prevented.

(Second Arrangement of Wafer Processing Apparatus)

Fig. 5 is a view showing the schematic arrangement of a wafer processing apparatus suitable to remove a porous layer.

In a wafer processing apparatus 10, members which may come into contact with the process solution are preferably made of silica glass or a plastic in accordance with their application purposes. As the plastic, a fluoroplastic, vinyl chloride, polyethylene, polypropylene, polybutylene terephthalate (PBT), or polyether ether ketone (PEEK) can be used. As the fluoroplastic, PVDF, PFA, or PTFE is

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suitable.

The wafer processing apparatus 10 comprises a wafer processing tank 11, and a holder driving mechanism 31 for swinging a wafer holder 21 in the wafer processing tank 11. The wafer processing apparatus 10 preferably has an ultrasonic tank 61.

Before processing wafers, the wafer processing tank 11 is filled with a process solution. The wafer processing tank 11 has a four-side overflow tank 12. The process solution is supplied by a circulator 71 with a filter from the bottom portion of the wafer processing tank 11 into the wafer processing tank 11. The process solution overflowing from the wafer processing tank 11 is stored in the four-side overflow tank 12 and discharged from the bottom portion of the four-side overflow tank 12 to the circulator 71. In this wafer processing apparatus 10, the wafer holder 21 is swung by the holder driving mechanism 31, and simultaneously, the process solution is stirred. For this reason, the circulating system including the four-side overflow tank 12 is extremely effective to maintain a constant liquid surface of the process solution.

As the wafer holder 21, a commercially available product can be used. The wafer holder 21 is preferably made of silica glass or a plastic. As the plastic, a fluoroplastic, vinyl chloride, polyethylene, polypropylene, polybutylene terephthalate (PBT), or polyether ether ketone (PEEK) can

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be used. As the fluoroplastic, PVDF, PFA, or PTFE is suitable.

The holder driving mechanism 31 has a pair of holding portions 31a for holding the wafer holder 21. The wafer holder 21 is held by the pair of holding portion 31a and dipped in the wafer processing tank 11. Desired processing can be performed for a wafer 40 while swinging the wafer holder 21 in the wafer processing tank 11. The holder driving mechanism 31 has a function of conveying the wafer holder 21 storing wafers 40 which have been processed in the preceding step to the wafer processing tank 11 or to the next step. The holder driving mechanism 31 also has a function as part of the wafer processing apparatus 10.

In this embodiment, the holding portions 31a hold the wafer holder 21, so the wafer 40 is indirectly held. However, the holding portions 31a may be replaced with, e.g., chuck pads to directly hold the wafer 40. The direction in which the wafer 40 is held is not limited to the direction perpendicular to the bottom surface of the wafer processing tank 11 and may be parallel to the bottom surface.

The ultrasonic tank 61 has an ultrasonic source 51 and is filled with an ultrasonic transmission medium (e.g., water). The ultrasonic source 51 is fixed on an adjustment mechanism 62 for adjusting the vertical and/or horizontal position of the ultrasonic source 51. When the positional relationship between the ultrasonic source 51 and the wafer

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processing tank 11 is adjusted by the adjustment mechanism 62, the ultrasonic wave to be supplied to the wafer processing tank 11 and, more specifically, to the wafer 40 can be optimized. The ultrasonic source 51 preferably has a function of adjusting the frequency or strength of the generated ultrasonic wave. With this arrangement, supply of an ultrasonic wave can be further optimized. By imparting the function of optimizing supply of an ultrasonic wave to the wafer 40, the ultrasonic wave can be supplied individually to a variety of types of wafers.

The wafer processing apparatus 10 has a control section for ON/OFF-controlling the ultrasonic source 51. With this control section, porous layer removing processing can be controlled.

(Third Arrangement of Wafer Processing Apparatus)

Fig. 6 is a view showing the schematic arrangement of a wafer processing apparatus suitable to remove a porous layer. Figs. 7A to 7E are views showing operation of the wafer processing apparatus shown in Fig. 6. Fig. 8 is a perspective view of a swing assist member in the wafer processing apparatus shown in Fig. 6.

The wafer processing tank 11 preferably has, on the bottom surface, a swing assist member 13 for increasing the efficiency of swing of the wafer 40 by the holder driving mechanism 31. The swing assist member 13 comes into contact with the side surface of the wafer 40 held by the wafer holder

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21 when the wafer holder 21 moves, thereby rotating and vertically moving the wafer 40 in the wafer holder 21 by the frictional force. The swing assist member 13 is useful to improve the surface uniformity of the processed wafer.

It is also effective to use a driving mechanism for vertically (Y-axis direction) and/or horizontally (X-axis direction) moving the swing assist member 13. In this case, the swing assist member 13 itself moves to rotate the wafer 40 and vertically move the wafer 40 in the wafer holder 21. Therefore, the range in which the holder driving mechanism 31 moves the wafer holder 21 can be made small. In other words, the wafer processing tank 11 can be made compact.

The ultrasonic tank 61 has the ultrasonic source 51 and is filled with an ultrasonic transmission medium (e.g., water). The ultrasonic source 51 is fixed on the adjustment mechanism 62 for adjusting the vertical and/or horizontal position of the ultrasonic source 51. When the positional relationship between the ultrasonic source 51 and the wafer processing tank 11 is adjusted by the adjustment mechanism 62, the ultrasonic wave to be supplied to the wafer processing tank 11 and, more specifically, to the wafer 40 can be optimized. The ultrasonic source 51 preferably has a function of adjusting the frequency or strength of the generated ultrasonic wave. With this arrangement, supply of an ultrasonic wave can be further optimized. By imparting the function of optimizing supply of an ultrasonic wave to

the wafer 40, the ultrasonic wave can be supplied individually to a variety of types of wafers.

The wafer processing apparatus 10 has a control section for ON/OFF-controlling the ultrasonic source 51. With this control section, porous layer removing processing can be controlled.

Figs. 7A to 7E are views for explaining a wafer swing method. In these drawings, arrows indicate the moving directions of the wafer holder 21. Fig. 7A shows a state immediately before the wafer starts to be swung. When the start of wafer swing operation is instructed, the holder driving mechanism 31 presses the holding portions 31a downward under computer control, as shown in Fig. 7B. The side surface of the wafer 40 comes into contact with the swing assist member 13 midway this pressing. The wafer 40 is supported by the swing assist member 13 at its lower portion.

When the swing assist member 13 comes into contact with the wafer 40, particles may be produced albeit in a small amount. To prevent this, the distal end portion of the swing assist member 13 is preferably has a round shape, as shown in Fig. 8, for smooth contact with the wafer 40.

The swing assist member 13 only need to assist swing of the wafer 40 and therefore can have a shape not to impede transmission of the ultrasonic wave, e.g., a thin plate-like shape. With this arrangement, the ultrasonic wave can be uniformly supplied to the wafer 40, and the wafer 40 can

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be uniformly processed.

In this wafer processing apparatus 10, the wafer 40 is processed while changing the relative positional relationship between the wafer 40 and the swing assist member 13, i.e., the relative positional relationship between the wafer 40 and the wafer processing tank 11. For this reason, slight nonuniformity of the ultrasonic wave due to the swing assist member 13 poses no problem.

When the press amount of the wafer holder 21 is large to some extent, the contact pressure between the wafer 40 and the swing assist member 13 can be increased. Hence, sliding movement between the swing assist member 13 and the wafer 40 is eliminated to prevent operation failures. If the press amount is small, the gravity against the wafer 40 acts more largely on the wafer holder 21 than on the distal end portion of the swing assist member 13. When the swing assist member 13 having the shape of this embodiment is used, the press amount is preferably set to be about 30 mm after the wafer 40 comes into contact with the swing assist member 13.

When the operation of pressing the wafer holder 21 is ended, the holder driving mechanism 31 moves the holding portions 31a to the right (positive X-axis direction) under computer control, as shown in Fig. 7C. The wafer 40 substantially horizontally moves to the right (positive X-axis direction) in the wafer processing tank 11 while rotating clockwise. The moving amount of the holding

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portions 31a must be set within the range in which the holding portions 31a do not collide against the lower opening portion of the wafer holder 21.

When movement of the wafer holder 21 to the right (positive X-axis direction) is ended, the holder driving mechanism 31 moves the holding portions 31a upward under computer control, as shown in Fig. 7D. The moving amount of the holding portions 31a is preferably set within the range in which the wafer 40 does not come close to a liquid surface 14 of the process solution. If the wafer 40 comes close to the liquid surface 14, particles may adhere to the surface of the wafer 40.

When movement of the wafer holder 21 upward is ended, the holder driving mechanism 31 moves the holding portions 31a to the left (negative X-axis direction) under computer control, as shown in Fig. 7E, so the initial state is restored (Fig. 7A).

By repeating the above operation (Fig. 7A → Fig. 7B → Fig. 7C → Fig. 7D → Fig. 7E), the wafer 40 can be appropriately swung and uniformly processed.

According to the wafer processing apparatus 10, since the wafer 40 is swung in the region where supply of an ultrasonic wave is optimized by adjusting the ultrasonic tank 61, the ultrasonic wave acting on the wafer 40 can be optimized.

As is known, the standing wave of an ultrasonic wave

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has antinodes and nodes at a predetermined interval. Therefore, it is difficult to uniform the ultrasonic wave in the wafer processing tank 11.

However, in this wafer processing apparatus 10, processing for the wafer 40 can be uniformed independently of the nonuniform strength distribution of the ultrasonic wave because the holder driving mechanism 31 swings the wafer 40. Even when the wafer 40 is simply moved only in the horizontal direction, vertical direction, or oblique direction, processing for the wafer 40 can be uniformed. When the wafer 40 is also swung in the axial direction (Z-axis direction), nonuniformity in processing between wafers due to the high-strength portion of the ultrasonic wave in the horizontal plane can also be corrected.

Since the wafer processing apparatus 10 has the swing assist member 13, the swing amount of the wafer 40 can be efficiently increased. The fixed position of the swing assist member 13 is not limited to the bottom portion of the wafer processing tank 11. As far as the swing assist member 13 can contact all wafers 40 in the wafer holder 21, the swing assist member 13 may be fixed on the inner wall of the wafer processing tank 11 or on the holder driving mechanism 31 (in this case, a mechanism for changing the relative positional relationship between the holding portions 31a and the swing assist member 13 is required).

In addition, according to the wafer processing

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apparatus 10, since no driving mechanism is present in the wafer processing tank 11, particles are not produced due to operation of the driving mechanism.

(Fourth Arrangement of Wafer Processing Apparatus)

Fig. 9 is a view showing the schematic arrangement of a wafer processing apparatus suitable to remove a porous layer.

In a wafer processing apparatus 300, the wafer 40 is held almost parallel to the bottom surface of the wafer processing tank 11 (i.e., almost parallel to the vibration plane of the ultrasonic wave) and completely dipped in the process solution (etchant) in the wafer processing tank 11, and in this state, swung by a wafer moving mechanism 80, thereby uniformly processing the wafer 40 and prevent contamination by particles.

The wafer moving mechanism 80 holds the wafer 40 with an arm 81 and swings the wafer 40 in the wafer processing tank 11. The wafer 40 is preferably swung in a direction crossing the vibration plane of the ultrasonic wave (i.e., in the vertical direction) and a direction parallel to the vibration plane (i.e., in the horizontal direction).

In this wafer processing apparatus 300 as well, preferably, the wafer 40 completely dipped in the process solution is processed. In this case, particles can be prevented from adhering to the wafer 40 near the interface between the process solution and gas.

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According to the wafer processing apparatus 300, the wafer 40 can be uniformly processed by swinging the wafer 40 in the wafer processing tank 11.

(Fifth Arrangement of Wafer Processing Apparatus)

Fig. 10 is a view showing the schematic arrangement of a wafer processing apparatus suitable to remove a porous layer. In the wafer processing apparatuses of the second to fourth arrangements, wafers are processed while being swung. In a wafer processing apparatus 500 of the fifth arrangement, the speed of flow of the process solution (etchant) is increased instead of swinging wafers.

In the wafer processing apparatus 500, a support portion 73 for supporting the wafer holder 21 is placed at the lower portion of the wafer processing tank 11. The process solution supplied from the circulator 71 spouts from spout ports 72 under the support portion 73 at a high speed. The support portion 73 has a plurality of opening portions. The process solution spouted from the spout ports 72 moves upward through the opening portions.

When the process solution is circulated at a high speed, the wafer 40 can be uniformly processed.

It is also effective to assemble the above-described circulating mechanism (71 to 73) in the wafer processing apparatus 10 shown in Fig. 5.

(Sixth Arrangement of Wafer Processing Apparatus)

In the above-described wafer processing apparatuses,

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supply and nonsupply of the ultrasonic wave to the wafer processing tank are switched by controlling the ultrasonic source. Instead, a mechanism for shielding the ultrasonic wave as needed may be inserted between the ultrasonic source and the wafer.

A modification of the wafer processing apparatus shown in Fig. 5 or 6 will be described. Figs. 11A and 11B show a modification of the wafer processing apparatus shown in Fig. 5 or 6. In Figs. 11A and 11B, the overflow tank and the circulator are omitted.

The wafer processing apparatus of this modification has shutters 91 and 92 for shielding the ultrasonic wave, as needed, between the ultrasonic source 51 and the bottom surface of the wafer processing tank 11. To transmit the ultrasonic wave to the wafer processing tank 11, the shutters 91 and 92 are opened by a driving section (not shown), as shown in Fig. 11A. To shield the ultrasonic wave to the wafer processing tank 11, the shutters 91 and 92 are closed by the driving section (not shown), as shown in Fig. 11B. As the material of the shutters 91 and 92, a material which hardly transmits the ultrasonic wave, e.g., PFA or PTFE is suitable.

(Seventh Arrangement of Wafer Processing Apparatus)

Figs. 12A to 12C are views showing the schematic arrangement of a wafer processing apparatus suitable to remove a porous layer. Fig. 12A is a front view, Fig. 12B is a side view, and Fig. 1C is a plan view.

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In a wafer processing apparatus 700, a jet of fluid (e.g., water) 701 is sprayed from the spray nozzle 700, and the porous layer of the wafer 40 is removed by the sprayed fluid.

In the example shown in Figs. 12A to 12C, the spray nozzle 700 is scanned in the Z-axis direction while spraying the fluid 701 from the spray nozzle 700 perpendicularly to the wafer 40, thereby removing a porous layer 40a on the entire surface.

Examples to which the above porous layer removing method is applied will be described below.

(Example 1)

A film of a material having a HF resistance was formed on the surface of a single-crystal Si substrate and patterned to form a mask pattern having an opening. The single-crystal Si substrate exposed in the opening portion was anodized in an HF solution to form a porous layer. With this process, a 50-μm thick porous layer was formed on the single-crystal Si substrate. Next, the mask pattern was removed. Instead of forming a mask pattern on the single-crystal Si substrate, the single-crystal Si substrate may be set in a holder with which the HF solution can contact only the region where the porous layer is to be formed, and subjected to anodizing.

The resultant substrate was set in the processing apparatus 100 shown in Fig. 4. The wafer processing tank 110 of the processing apparatus 100 shown in Fig. 4 was filled with a mixed solution (etchant) of fluoric acid, hydrogen

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peroxide, and pure water in advance. In the processing apparatus 100, the substrate was rotated for about 2 hrs, and at the same time, an ultrasonic wave near 1 MHz was applied to fill pores in the porous Si layer with the etchant.

The operation of the ultrasonic source 131 was stopped, and the substrate was left to stand in the wafer processing tank 110 for about 1 hr. With this process, the pore walls of the porous Si layer thinned.

Subsequently, the porous Si layer was completely removed using the apparatus shown in Figs. 12A to 12C. As a result, a structure having a 50-μm deep recessed portion on the substrate surface was formed.

The same structure as described above could be formed using the apparatus shown in Fig. 5, 6, or 9.

(Example 2)

A film of a material having a HF resistance was formed on the surface of a single-crystal Si substrate and patterned to form a mask pattern having an opening. The single-crystal Si substrate exposed in the opening portion was anodized in an HF solution to form a porous layer reaching the lower surface. Then, the mask pattern was removed. Instead of forming a mask pattern on the single-crystal Si substrate, the single-crystal Si substrate may be set in a holder with which the HF solution can contact only the region where the porous layer is to be formed, and subjected to anodizing.

Subsequently, a single-crystal Si layer having a

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thickness of 1 μm was formed on the surface of the substrate as a resultant structure by epitaxial growth.

The resultant substrate was set in the processing apparatus 100 shown in Fig. 4. The wafer processing tank 110 of the processing apparatus 100 shown in Fig. 4 was filled with a mixed solution (etchant) of fluoric acid, hydrogen peroxide, and pure water in advance. In the processing apparatus 100, the substrate was rotated for about 6 hrs, and at the same time, an ultrasonic wave near 0.25 MHz was applied to fill pores in the porous Si layer with the etchant.

The operation of the ultrasonic source 131 was stopped, and the substrate was left to stand in the wafer processing tank 110 for about 2 hrs. With this process, the pore walls of the porous Si layer thinned.

The ultrasonic source 131 was operated again for about 5 min to completely remove the porous Si layer. As a result, a single-crystal Si membrane including the epitaxial layer (single-crystal Si layer) formed on the porous Si layer was formed. The epitaxial layer had a virtually uniform thickness on the entire surface.

A cantilever structure of single-crystal Si may be formed, as shown in Fig. 2C, by partially removing the epitaxial layer (single-crystal Si layer) in advance.

The same result as described above could be obtained by the apparatus shown in Fig. 5, 6, or 9.

(Example 3)

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A first single-crystal Si substrate was prepared. The surface layer was anodized in a HF solution to form a porous Si layer. The anodizing conditions were as follows.

Current density: 7 (mA/cm^2)

Anodizing solution: $HF : H_2O : C_2H_5OH = 1 : 1 : 1$

Time: 11 (min)

Thickness of porous Si layer: 12 (μm)

This substrate was then oxidized in an oxygen atmosphere at 400°C for 1 hr. Upon this oxidation, the inner wall of each pore of the porous Si layer was covered with a thermal oxide film. A single-crystal Si layer having a thickness of 0.30 μm was epitaxially grown on the porous Si layer by CVD (Chemical Vapor Deposition). The growing conditions were as follows.

Source gas: SiH_2Cl_2/H_2

Gas flow rate: 0.5/180 (l/min)

Gas pressure: 80 (Torr)

Temperature: 950 (°C)

Growth rate: 0.3 (μm/min)

Subsequently, an SiO_2 layer having a thickness of 200 nm was formed on the epitaxial Si layer by thermal oxidation.

The surface of the SiO_2 layer of the first substrate was bonded to the surface of a prepared Si substrate (second substrate).

The first substrate side was removed by grinding, polishing, or etching to expose the porous Si layer in the

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entire region on the second substrate.

The second substrate was set in the wafer processing apparatus 100 shown in Fig. 4. The wafer processing tank 110 of the processing apparatus shown in Fig. 4 was filled with a mixed solution (etchant) of fluoric acid, hydrogen peroxide, and pure water in advance. In the processing apparatus 100, the second substrate was rotated for about 1.5 hrs, and at the same time, an ultrasonic wave near 0.25 MHz was applied to fill pores in the porous Si layer with the etchant.

The operation of the ultrasonic source 131 was stopped, and the substrate was left to stand in the wafer processing tank 110 for about 1 hr. With this process, the pore walls of the porous Si layer thinned.

The ultrasonic source 131 was operated again for about 5 min to completely remove the porous Si layer. At this time, when the etchant is appropriately circulated, as shown in Fig. 10, surface uniformity of the processed substrate increases.

The ultrasonic wave is applied to the etchant for the porous Si layer, the substrate is rotated, and simultaneously, the etchant is circulated to fill the pores in the porous layer on the substrate with the etchant. After this, application of the ultrasonic wave is stopped, and the substrate is left to stand for an appropriate time. With this process, for each of all substrates, the pore walls in the porous Si layer can be sufficiently thinned in the entire

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region on the surface. For this reason, the remaining porous Si layer can be removed at once uniformly on the entire region of each substrate.

The same result as described above could be obtained by the apparatus shown in Fig. 5, 6, or 9.

Even when one of the following methods is employed instead of the method of applying an ultrasonic wave again after application of the ultrasonic wave is stopped, the remaining porous Si layer can be removed with high quality.

(1) The resultant structure is dipped in a mixed solution of fluoric acid, nitric acid, and pure water for about 5 sec to remove the porous layer.

(2) The porous Si layer is removed by polishing.

(3) The porous Si layer is removed by scrubbing.

(4) The porous Si layer is removed by scanning the substrate while spraying a water jet at a pressure of, e.g., 1,000 kg/cm^2.

In the step of removing the porous Si layer, the single-crystal Si layer functioned as an etch stop layer, so the porous Si layer was selectively etched and completely removed.

The etching rate of the non-porous Si single crystal for the above etchant is very low. The selectivity ratio to the etching rate of the non-porous Si single crystal to that of the porous layer is 10^5 or more. The etching amount of the non-porous layer (about several ten Å) is allowable for

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practical use.

With the above process, an SOI substrate having a 0.2-μm thick single-crystal Si layer on the Si oxide film was formed. The thickness of the resultant single-crystal Si layer was measured at 100 points on the entire surface. The thickness was 201 nm ± 4 nm.

The resultant structure was subjected to a heat treatment in hydrogen at 1,100°C for 1 hr, and the surface roughness was evaluated with an atomic force microscope. The mean square roughness in a 5-μm square area was about 0.2 nm. This nearly equals that of a commercially available Si wafer.

Section observation with a transmission electron microscope revealed that no new crystal defects were formed in the single-crystal Si layer, and satisfactory crystallinity was maintained.

The same result as described above was obtained even when the oxide film (SiO_2) was formed not on the surface of the epitaxial layer but on the surface of the second substrate or on both these surfaces.

A satisfactory result was obtained even when a transparent substrate of silica glass or the like was used as the second substrate. In this case, however, since a slip may be formed in the single-crystal Si layer due to some difference in thermal expansion coefficient between silica glass and the single-crystal Si layer, the temperature of

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the heat treatment in hydrogen was decreased from 1,100°C to 1,000°C or less.

(Example 4)

A second substrate was subjected to two-step anodizing in an HF solution to form two porous layers. The anodizing conditions were as follows.

<Anodizing of First Step>

Current density: 7 (mA/cm^2)

Anodizing solution: $HF : H_2O : C_2H_5OH = 1 : 1 : 1$

Time: 5 (min)

Thickness of porous Si layer: 5.5 (μm)

<Anodizing of Second Step>

Current density: 30 (mA/cm^2)

Anodizing solution: $HF : H_2O : C_2H_5OH = 1 : 1 : 1$

Time: 110 (sec)

Thickness of porous Si layer: 3 (μm)

Subsequently, this substrate was oxidized in an oxygen atmosphere at 400°C for 1 hr. Upon this oxidation, the inner wall of each pore of the porous Si layer was covered with a thermal oxide film. A single-crystal Si layer having a thickness of 0.15 μm was epitaxially grown on the porous Si layer by CVD (Chemical Vapor Deposition). The growing conditions were as follows.

Source gas: SiH_2Cl_2/H_2

Gas flow rate: 0.5/180 (l/min)

Gas pressure: 80 (Torr)

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Temperature: 950 (°C)

Growth rate: 0.3 (μm/min)

After that, an SiO_2 layer having a thickness of 100 nm was formed on the epitaxial Si layer by thermal oxidation.

The surface of the SiO_2 layer of the first substrate was bonded to the surface of a prepared Si substrate (second substrate).

The bonded substrate stack was divided into two substrates by the porous Si layer formed at a current density of 30 mA/cm^2 (anodizing of second step) to expose the porous Si layer to the entire surface on the second substrate side. To divide the bonded substrate stack, the substrates are mechanically pulled, twisted, or pressed, a wedge is driven into the edge of the bonded substrate stack, the bonded substrate stack is oxidized from the end face to peel the substrates, thermal stress is used, an ultrasonic wave is applied, or a water jet is injected into the edge of the bonded substrate stack.

The second substrate was set in the wafer processing apparatus 100 shown in Fig. 4. The wafer processing tank 110 of the processing apparatus shown in Fig. 4 was filled with a mixed solution (etchant) of fluoric acid, hydrogen peroxide, and pure water in advance. In the processing apparatus 100, the second substrate was rotated for about 1.5 hrs, and at the same time, an ultrasonic wave near 0.25 MHz was applied to fill pores in the porous Si layer with the etchant.

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The operation of the ultrasonic source 131 was stopped, and the substrate was left to stand in the wafer processing tank 110 for about 1 hr. With this process, the pore walls of the porous Si layer thinned.

The ultrasonic source 131 was operated again for about 5 min to completely remove the porous Si layer. At this time, when the etchant is appropriately circulated, as shown in Fig. 10, surface uniformity of the processed substrate improves.

The ultrasonic wave is applied to the etchant for the porous Si layer, the substrate is rotated, and simultaneously, the etchant is circulated to fill the pores in the porous layer on the substrate with the etchant. After this, application of the ultrasonic wave is stopped, and the substrate was left to stand for an appropriate time. With this process, for each of all substrates, the pore walls in the porous Si layer can be sufficiently thinned in the entire region on the surface. For this reason, the remaining porous Si layer can be removed at once uniformly on the entire region of each substrate.

The same result as described above could be obtained by the apparatus shown in Fig. 5, 6, or 9.

Even when one of the following methods is employed instead of the method of applying an ultrasonic wave again after application of the ultrasonic wave is stopped, the remaining porous Si layer can be removed with high quality.

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(1) The resultant structure is dipped in a mixed solution of fluoric acid, nitric acid, and pure water for about 5 sec to remove the porous layer.

(2) The porous Si layer is removed by polishing.

(3) The porous Si layer is removed by scrubbing.

(4) The porous Si layer is removed by scanning the substrate while spraying a water jet at a pressure of, e.g., 1,000 kg/cm^2.

In the step of removing the porous Si layer, the single-crystal Si layer functioned as an etch stop layer, so the porous Si layer was selectively etched and completely removed.

The etching rate of the non-porous Si single crystal for the above etchant is very low. The selectivity ratio to the etching rate of the non-porous Si single crystal to that of the porous layer is 10^5 or more. The etching amount of the non-porous layer (about several ten Å) is allowable for practical use.

With the above process, an SOI substrate having a 0.1-μm thick single-crystal Si layer on the Si oxide film was formed. The thickness of the resultant single-crystal Si layer was measured at 100 points on the entire surface. The thickness was 101 nm ± 3 nm.

The resultant structure was subjected to a heat treatment in hydrogen at 1,100°C for 1 hr, and the surface roughness was evaluated with an atomic force microscope. The

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mean square roughness in a 5-μm square area was about 0.2 nm. This nearly equals that of a commercially available Si wafer.

Section observation with a transmission electron microscope revealed that no new crystal defects were formed in the single-crystal Si layer, and satisfactory crystallinity was maintained.

The same result as described above was obtained even when the oxide film was formed not on the surface of the epitaxial layer but on the surface of the second substrate or on both these surfaces.

A satisfactory result was obtained even when a transparent substrate of silica glass or the like was used as the second substrate. However, since a slip may be formed in the single-crystal Si layer due to some difference in thermal expansion coefficient between silica glass and the Si layer, the temperature of the heat treatment in hydrogen was decreased from 1,100°C to 1,000°C or less.

Section observation with a transmission electron microscope indicated that no new crystal defects were formed in the single-crystal Si layer, and satisfactory crystallinity was maintained.

The same result as described above was obtained even when the oxide film (SiO_2) was formed not on the surface of the epitaxial layer but on the surface of the second substrate or on both these surfaces.

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A satisfactory result was obtained even when a transparent substrate of silica glass or the like was used as the second substrate. However, since a slip may be formed in the single-crystal Si layer due to any difference in thermal expansion coefficient between silica glass and the single-crystal Si layer, the temperature of the heat treatment in hydrogen was decreased from 1,100°C to 1,000°C or less.

When the porous Si layer left on the first substrate side was selectively etched and subjected to a surface treatment such as hydrogen annealing or surface polishing, the substrate could be recycled as the first or second substrate.

Almost the same result as described above was obtained even when a porous layer with a single-layered structure was formed by anodizing.

In the above examples, as the epitaxial growing method of forming a single-crystal Si layer on the porous Si layer, not only CVD but also MBE, sputtering, or liquid phase growing can be used. A single-crystal compound semiconductor layer of GaAs or InP may be epitaxially grown on the porous Si layer. In this case, a high-frequency device such as GaAs on Si or GaAs on Glass (Quartz) or a substrate suitable for OEIC can be manufactured.

As the etchant used to selectively etch the porous Si layer, a mixed solution of 49% fluoric acid, 30% hydrogen

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peroxide and H_2O is suitable. However, the following etchants can also be used. Since the porous Si layer has a large surface area, selective etching is easy.

(a) Fluoric acid

(b) Mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to fluoric acid

(c) Buffered fluoric acid

(d) Mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to buffered fluoric acid

(e) Mixed solution of fluoric acid, nitric acid, and acetic acid.

In the above examples, to stop application of the ultrasonic wave, the operation of the ultrasonic source is stopped. However, use of shutters is also effective, as shown in Figs. 11A and 11B.

According to the present invention, a high planarity of the underlying layer of the porous region can be maintained.

The present invention is not limited to the above embodiments and various changes and modifications can be made within the spirit and scope of the present invention. Therefore, to apprise the public of the scope of the present invention, the following claims are made.

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WHAT IS CLAIMED IS:

1. A porous region removing method of removing a porous region from a substrate having the porous region, characterized by comprising:

the first step of processing the porous region by an etchant while supplying an ultrasonic wave to the etchant;

the second step of processing the porous region by the etchant without supplying any ultrasonic wave to the etchant or while supplying an ultrasonic wave weaker than the ultrasonic wave supplied in the first step to the etchant; and

the third step of removing the porous region remaining on the substrate.

2. The method according to claim 1, characterized in that the first step comprises filling pores in the porous region with the etchant to a deep portion.

3. The method according to claim 1 or 2, characterized in that the second step comprises thinning pore walls in the porous region to not more than a predetermined thickness by an etching function.

4. The method according to claim 3, characterized in that the second step comprises thinning the pore walls in the

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porous region to a thickness that allows removal of the remaining porous region at once in the third step.

5. The method according to any one of claims 1 to 4, characterized in that the third step comprises removing the porous region remaining on the substrate by the etchant.

6. The method according to claim 5, characterized in that the third step comprises removing the porous region remaining on the substrate by the etchant while supplying the ultrasonic wave to the etchant.

7. The method according to claim 5 or 6, characterized in that the first to third steps are executed while dipping the substrate to be processed in the same etchant.

8. The method according to claim 5 or 6, characterized in that the third step comprises removing the porous region remaining on the substrate by an etchant whose etching rate for the porous region is higher than that of the first or second etchant.

9. The method according to any one of claims 5 to 8, characterized in that the first to third steps are executed while completely dipping the substrate to be processed in the etchant.

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10. The method according to any one of claims 1 to 4, characterized in that the first and/or second steps is executed while completely dipping the substrate to be processed in the etchant.

11. The method according to any one of claims 1 to 4, characterized in that the third step comprises removing the porous region remaining on the substrate by a high-pressure fluid.

12. The method according to any one of claims 1 to 4, characterized in that the third step comprises removing the porous region remaining on the substrate by scrubbing.

13. The method according to any one of claims 1 to 12, characterized in that in processing the substrate while supplying the ultrasonic wave to the etchant, a relative positional relationship between an ultrasonic source and the substrate is changed.

14. The method according to claim 13, characterized in that in processing the substrate while supplying the ultrasonic wave to the etchant, the substrate is swung in the etchant.

15. The method according to claim 13, characterized in that

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in processing the substrate while supplying the ultrasonic wave to the etchant, the substrate is rotated.

16. The method according to claim 13, characterized in that in processing the substrate while supplying the ultrasonic wave to the etchant, a position of at least one of the substrate and the ultrasonic source is changed substantially in a direction parallel or perpendicular to a vibration plane of the ultrasonic wave.

17. The method according to any one of claims 1 to 12, characterized in that in processing the substrate by the etchant, the substrate is swung or rotated.

18. The method according to any one of claims 1 to 12, characterized in that in processing the substrate by the etchant, the etchant is circulated to form a flow of etchant near the substrate.

19. The method according to any one of claims 1 to 18, characterized in that the first and second steps are executed while dipping the substrate in the same etching tank, the first step comprises operating the ultrasonic source, and the second step comprises stopping operation of the ultrasonic source.

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20. The method according to any one of claims 1 to 18, characterized in that the first and second steps are executed while dipping the substrate in the same etching tank, the first and second steps comprise continuously operating the ultrasonic source, and the second step comprises inserting an ultrasonic shielding plate between the ultrasonic source and the substrate.

21. The method according to any one of claims 1 to 20, characterized in that the substrate to be processed essentially consists of single-crystal Si.

22. The method according to any one of claims 1 to 20, characterized in that the porous region essentially consists of porous Si.

23. The method according to claim 22, characterized in that the porous region is formed by anodizing a single-crystal Si substrate.

24. The method according to any one of claims 1 to 23, characterized in that as the etchant, any one of

(a) fluoric acid,

(b) a mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to fluoric acid,

(c) buffered fluoric acid, and

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(d) a mixed solution prepared by adding at least one of an alcohol and hydrogen peroxide to buffered fluoric acid is used.

25. A semiconductor substrate manufacturing method characterized by comprising the steps of:

forming a porous layer and at least one non-porous layer on a first substrate;

bonding a second substrate to the non-porous layer side of the first substrate;

removing the first substrate from the bonded substrate stack to expose the porous layer on a surface of the second substrate; and

removing the porous layer on the second substrate using any one of the methods of claims 1 to 24.

26. The method according to claim 25, characterized in that the step of exposing the porous layer comprises grinding, polishing, or etching the first substrate from a back surface side of the first substrate of the bonded substrate stack, thereby exposing the porous layer to the surface of the second substrate.

27. The method according to claim 25, characterized in that the step of exposing the porous layer comprises dividing the bonded substrate stack at the porous layer, thereby exposing

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the porous layer on the surface of the second substrate.

28. The method according to any one of claims 25 to 27, characterized in that the non-porous layer includes a single-crystal Si layer.

29. The method according to any one of claims 25 to 27, characterized in that the non-porous layer includes a single-crystal Si layer and an Si oxide layer.

30. The method according to claim 28 or 29, characterized in that the single-crystal Si layer is epitaxially grown on the porous layer on the first substrate.

31. The method according to any one of claims 25 to 27, characterized in that the non-porous layer includes a single-crystal compound semiconductor layer.

32. The method according to any one of claims 25 to 31, characterized in that the second substrate essentially consists of an Si material.

33. The method according to any one of claims 25 to 32, characterized in that the second substrate has an Si oxide layer on a surface to be bonded to the first substrate.

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34. The method according to any one of claims 25 to 31, characterized in that the second substrate comprises a transparent substrate.

35. A porous region removing apparatus for removing a porous region from a substrate having the porous region, characterized by comprising:

means for executing the first step of processing the porous region by an etchant while supplying an ultrasonic wave to the etchant;

means for executing the second step of processing the porous region by the etchant without supplying any ultrasonic wave to the etchant or while supplying an ultrasonic wave weaker than the ultrasonic wave supplied in the first step to the etchant; and

means for executing the third step of removing the porous region remaining on the substrate.

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POROUS REGION REMOVING METHOD AND SEMICONDUCTOR SUBSTRATE MANUFACTURING METHOD

ABSTRACT OF THE DISCLOSURE

This invention is to ensure a high planarity of an underlying layer after a porous layer is removed. A substrate to be processed is dipped in an etchant. In the first step, pores in the porous Si layer are filled with the etchant by supplying an ultrasonic wave. In the second step, supply of the ultrasonic wave is stopped, and the pore walls are thinned by the etching function. In the third step, the ultrasonic wave is supplied again to break the porous layer at once.

Figure 1