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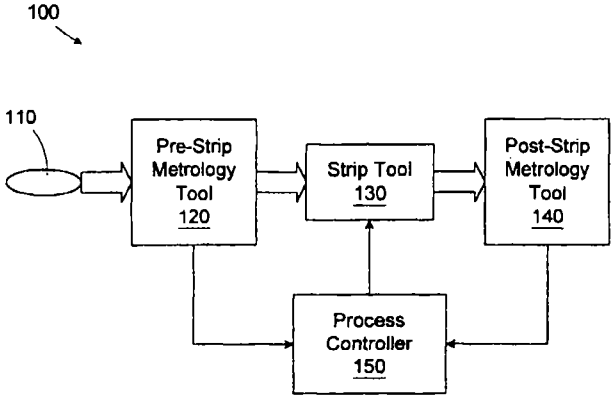
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(54) Title: FEEDBACK CONTROL OF STRIP TIME TO REDUCE POST STRIP CRITICAL DIMENSION VARIATION IN A TRANSISTOR GATE ELECTRODE



(57) Abstract: A method for decreasing variations in gate electrode widths is provided. The method includes providing a wafer having a ate electrode (230) formed thereon and an anti-reflective coating layer (240) formed over at least a portion of the gate electrode (230). The gate electrode (230) has a width. The width of the gate electrode (230) is measured. A strip rate for a strip tool (130) adapted to remove the anti-reflective coating (240) is determined. The measured width of the gate electrode (230) is compared to a target gate electrode critical dimension to determine an overetch time based on the strip rate. The operating recipe of the strip tool (130) is modified based on the overetch time. A processing line (100) includes a first metrology tool (120), a strip tool (130), and a process controller (150). The first metrology tool (120) is adapted to measure the width of a gate electrode (230) formed on a wafer. The gate electrode (230) has an anti-reflective coating layer (240) formed over at least a portion of the gate electrode (230). The strip tool (130) is adapted to remove the anti-reflective coating (240). The process controller (150) is adapted to determine a strip rate for the strip tool (130), compare the width of the gate electrode (230) to a target gate electrode critical dimension to determine an overetch time based on the strip rate, and modify the operating recipe of the strip tool (130) based on the overetch time.

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