ABSTRACT

A STRAINED CHANNEL TRANSISTOR AND METHOD OF FABRICATION THEREOF

The present invention relates to semiconductor integrated circuits. More particularly, but not exclusively, the invention relates to strained channel complimentary metal oxide semiconductor (CMOS) transistor structures and fabrication methods thereof. A strained channel CMOS transistor structure comprises a source stressor region comprising a source extension stressor region; and a drain stressor region comprising a drain extension stressor region; wherein a strained channel region is formed between the source extension stressor region and the drain extension stressor region, a width of said channel region being defined by adjacent ends of said extension stressor regions.

Fig. 2L