ABSTRACT

A semiconductor memory device includes a memory cell array including a plurality of memory cell rows and a row hammer management circuit. The row hammer management circuit stores counted values in count cells of each of the plurality of memory cell rows as count data, and performs an internal read-update-write operation to read the count data from the count cells of a target memory cell row from among the plurality of memory cell rows, to update the count data that was read to obtain updated count data, and to write the updated count data in the count cells of the target memory cell row. The row hammer management circuit includes a hammer address queue. The row hammer management circuit changes the updated count data randomly, based on an event signal indicating a state change of the hammer address queue.

FIG. 3