PITCH MULTIPLICATION USING SELF-ASSEMBLING MATERIALS

Reference to Related Applications

[0001] This application is related to U.S. Patent Application No. 11/389,581 to Gurtej Sandhu, filed March 23, 2006, entitled Topography Directed Patterning (Attorney Docket No. MICRON.342A) and U.S. Patent Application No. 11/445,907 to Gurtej Sandhu, filed June 2, 2006, entitled Topography Based Patterning (Attorney Docket No. MICRON.349A). The entire disclosure of each of these references is incorporated by reference herein.

Background of the Invention

Field of the Invention

[0002] This invention relates to mask formation, including printing techniques for integrated circuit fabrication.

Description of the Related Art

[0003] As a consequence of many factors, including demand for increased portability, computing power, memory capacity and energy efficiency, integrated circuits are continuously being reduced in size. The sizes of the constituent features that form the integrated circuits, *e.g.*, electrical devices and interconnect lines, are also constantly being decreased to facilitate this size reduction.

[0004] The trend of decreasing feature size is evident, for example, in memory circuits or devices such as dynamic random access memories (DRAMs), flash memory, static random access memories (SRAMs), ferroelectric (FE) memories, etc. To take one example, DRAM typically includes millions of identical circuit elements, known as memory cells. A memory cell typically consists of two electrical devices: a storage capacitor and an access field effect transistor. Each memory cell is an addressable location that may store one bit (binary digit) of data. A bit may be written to a cell through the transistor and may be read by sensing charge in the capacitor. Some memory technologies employ elements that can act as

both a storage device and a switch (*e.g.*, dendritic memory employing silver-doped chalcogenide glass) and some nonvolatile memories do not require switches for each cell (*e.g.*, magnetoresistive RAM) or incorporate switches into the memory element (*e.g.*, EEPROM for flash memory).

[0005] In another example, flash memory typically includes millions of flash memory cells containing floating gate field effect transistors that may retain a charge. The presence or absence of a charge in the floating gate determines the logic state of the memory cell. A bit may be written to a cell by injecting charge to or removing charge from a cell. Flash memory cells may be connected in different architecture configurations, each with different schemes for reading bits. In a "NOR" architecture configuration, each memory cell is coupled to a bit line and may be read individually. In a "NAND" architecture configuration, memory cells are aligned in a "string" of cells, and an entire bit line is activated to access data in one of the string of cells.

[0006] In general, by decreasing the sizes of the electrical devices that constitute a memory cell and the sizes of the conducting lines that access the memory cells, the memory devices may be made smaller. Additionally, storage capacities may be increased by fitting more memory cells on a given area in the memory devices. The need for reductions in feature sizes, however, is more generally applicable to integrated circuits, including general purpose and specialty processors.

[0007] The continual reduction in feature sizes places ever greater demands on the techniques used to form the features. For example, photolithography is commonly used to pattern these features. Typically, photolithography involves passing light through a reticle and focusing the light onto a photochemically-active photoresist material. Just as a slide has an image to be projected onto a screen, the reticle typically has a pattern to be transferred to a substrate. By directing light or radiation through the reticle, the pattern in the reticle may be focused on the photoresist. The light or radiation causes a chemical change in the illuminated parts of the photoresist, which allows those parts to be selectively retained or removed, depending upon whether positive or negative photoresist is used, relative to parts which were in the shadows. Thus, the exposed and unexposed parts form a pattern in the photoresist.

[0008] Because lithography is typically accomplished by projecting light or radiation onto a surface, the ultimate resolution of a particular lithography technique depends upon factors such as optics and light or radiation wavelength. For example, the ability to focus well-defined patterns onto resist depends upon the size of the features and on the wavelength of the radiation projected through the reticle. It will be appreciated that resolution decreases with increasing wavelength, due, among other things, to diffraction. Thus, shorter wavelength radiation is typically used to form well-resolved features, as the sizes of the features decrease.

[0009] In conjunction with radiation of a particular wavelength, photolithography utilizes photoresist compatible with that radiation. After being developed, the photoresist acts as a mask to transfer a pattern to an underlying material. The photoresist is sufficiently robust to withstand the development step without deforming and is also sufficiently robust to withstand an etch for transferring the mask pattern to an underlying material. As feature sizes decrease, however, the widths of the photoresist mask features also decrease, but typically without a corresponding decrease in the heights of these mask features. Due to the high aspect ratio of these mask features, it may be difficult to maintain the structural integrity of these thin mask features during the development and pattern transfer steps. As a result, the availability of sufficiently robust photoresist materials may limit the ability of photolithography to print features, as those features continue to decrease in size.

[0010] Accordingly, there is a continuing need for high resolution methods to pattern small features.

Brief Description of the Drawings

[0011] Figure 1 is a schematic cross-sectional side view of a substrate with overlying masking layers, in accordance with some embodiments of the invention.

[0012] Figure 2 is a schematic cross-sectional side view of the structure of Figure 1 after patterning a selectively-definable layer, in accordance with some embodiments of the invention.

[0013] Figure 3 is a schematic cross-sectional side view of the structure of Figure 2 after etching through a hard mask layer, in accordance with embodiments of the invention.

[0014] Figure 4 is a schematic cross-sectional side view of the structure of Figure 3 after removing the selectively-definable layer, in accordance with some embodiments of the invention.

[0015] Figure 5 is a schematic, cross-sectional side view of the structure of Figure 4 after widening spaces between features in the hard mask layer, in accordance with some embodiments of the invention.

[0016] Figure 6 is a schematic, cross-sectional side view of the structure of Figure 5 after depositing a layer of a solution of self-organizing material, in accordance with some embodiments of the invention.

[0017] Figure 7 is a schematic, cross-sectional side view of the structure of Figure 6 after self-assembly of the self-organizing material, in accordance with some embodiments of the invention.

[0018] Figures 8 is a schematic, top plan view of the structure of Figure 7 showing an arrangement of domains of material resulting from the self-assembly of the self-organizing material, in accordance with some embodiments of the invention.

[0019] Figure 9 is a schematic, cross-sectional side view of the structure of Figure 7 after selectively removing some domains of self-organizing material to form mandrels, in accordance with some embodiments of the invention.

[0020] Figure 10 is a schematic, cross-sectional side view of the structure of Figure 9 after depositing a layer of a spacer material, in accordance with some embodiments of the invention.

[0021] Figure 11 is a schematic, cross-sectional side view of the structure of Figure 10 after a spacer etch, in accordance with some embodiments of the invention.

[0022] Figure 12 is a schematic, cross-sectional side view of the structure of Figure 11 after removing the mandrels to leave a pattern of free-standing spacers, in accordance with some embodiments of the invention.

[0023] Figure 13 is a schematic, cross-sectional side view of the structure of Figure 12 after transferring a pattern formed by the freestanding spacers to an underlying substrate, in accordance with some embodiments of the invention.

[0024] Figure 14 is a schematic, cross-sectional side view of the structure of Figure 12 after depositing a planarizing layer over the spacers, in accordance with some embodiments of the invention.

[0025] Figure 15 is a schematic, cross-sectional side view of the structure of Figure 14 after patterning the planarizing layer, in accordance with some embodiments of the invention.

Detailed Description of Some Embodiments

[0026] The ability of block copolymers to self-organize may be used to form mask patterns. Block copolymers are formed of two or more chemically distinct blocks. For example, each block may be formed of a different monomer. The blocks are immiscible or thermodynamically incompatible, *e.g.*, one block may be polar and the other may be non-polar. Due to thermodynamic effects, the copolymers will self-organize in solution to minimize the energy of the system as a whole; typically, this causes the copolymers to move relative to one another, *e.g.*, so that like blocks aggregate together, thereby forming alternating regions containing each block type or species. For example, if the copolymers are formed of polar and non-polar blocks, the blocks will segregate so that non-polar blocks aggregate with other non-polar blocks and polar blocks aggregate with other polar blocks. It will be appreciated that the block copolymers may be described as a self-organizing material since the blocks can move to form a pattern without active application of an external force to direct the movement of particular individual molecules, although heat may be applied to increase the rate of movement of the population of molecules as a whole.

[0027] In addition to interactions between the block species, the self-organization of block copolymers can be influenced by topographical features, such as steps on the surface on which the block copolymers are deposited. For example, a diblock copolymer, a copolymer formed of two different block species, may form alternating domains, or regions, which are each formed of a substantially different block species. When self-organization of block species occurs in the area between the walls of a step, the steps may interact with the blocks such that, *e.g.*, each of the alternating regions formed by the blocks is made to form a

regular pattern with features oriented parallel to the walls. In addition, the self-organization of block copolymers may be guided by photolithographicly modifying a surface, without forming steps in the surface, as disclosed in: Stoykovich *et al.*, Science 308, 1442 (2005); Kim *et al.*, Nature 424, 411 (2003); and Edwards *et al.*, Adv. Mater. 16, 1315 (2004). The entire disclosure of each to these references is incorporated by reference herein.

[0028] Such self-organization can be useful in forming masks for patterning features during semiconductor fabrication processes. For example, one of the alternating domains may be removed, thereby leaving the material forming the other region to function as a mask. The mask may be used to pattern features such as electrical devices in an underlying semiconductor substrate. Methods for forming a copolymer mask are disclosed in U.S. Patent Application No. 11/389,581 to Gurtej Sandhu, filed March 23, 2006, entitled Topography Directed Patterning, Attorney Docket No.: MICRON.342A (Micron Ref. No.: 2005-0865); and U.S. Patent Application No. 11/445,907 to Gurtej Sandhu, filed June 2, 2006, entitled Topography Based Patterning (Attorney Docket No. MICRON.349A (Micron Ref. No.: 05-0865), the entire disclosure of each of which is incorporated by reference herein. While self-organizing materials may be used to form relatively small mask features, further decreases in the sizes of the mask features are desired due to the constant miniaturization of integrated circuits.

[0029] Moreover, the lengths of block copolymers may be an intrinsic limit to the sizes of domains formed by the blocks of those block copolymers. For example, the copolymers may be chosen with a length that facilitates self-assembly into a desired pattern of domains, and shorter copolymers may not self-assemble as desired.

[0030] Embodiments of the invention allow for the formation of features smaller than those that may be formed by block polymers alone. In embodiments of the invention, a self-organizing material formed of different chemical species is allowed to organize to form domains composed of like chemical species. Some of those domains are selectively removed to form mandrels, or temporary placeholders. A pitch multiplication process is then performed using the mandrels formed from the self-organizing material. Features with a pitch smaller than a pitch of the mandrels are derived from the mandrels. In some embodiments, spacers are formed on sidewalls of the mandrels and the mandrels are

selectively removed. The spacers, or other mask features derived from the spacers, are used as part of a mask to pattern underlying materials, *e.g.*, during the fabrication of integrated circuits.

[0031] Embodiments of the invention may form the mask features may be formed without using newer, relatively complex and expensive lithography techniques and the burden on the robustness of photoresist may be reduced. For example, rather than using relatively soft and structurally delicate photoresist in a mask, spacers or mask features derived from the spacers may be used as a mask. The use of spacers allows the selection of a variety of materials for the spacers, and the materials may be selected for robustness and compatibility with underlying materials used in a process flow. Moreover, because copolymer material is not used as a mask for patterning underlying layers, the copolymer materials may be selected without regard to, *e.g.*, their robustness and suitability for forming masking layers. Rather, the copolymer material may be selected based upon their self-organizing behavior and suitability for use in mandrels, thereby increasing process latitude. Moreover, the self-organizing behavior of materials such as block copolymers allows the reliable formation of very small features, thereby facilitating the formation of a mask with a very small feature size. For example, features having a critical dimension of about 1 nm to about 100 nm, about 3 nm to about 50 nm or about 5 nm to about 30 may be formed.

[0032] Reference will now be made to the Figures, wherein like numerals refer to like parts throughout. It will be appreciated that the Figures are not necessarily drawn to scale.

[0033] In a first phase of methods according to some embodiments, a plurality of mandrels is formed from self-organizing material, such as block copolymers. Figures 1-8 illustrate a method for self-assembling the self-organizing material into a desired pattern using guides or step features to guide the self-assembly. In other embodiments, it will be appreciated that the self-assembly of the self-organizing material may be directed by any method known in the art.

[0034] With reference to Figure 1, a cross-sectional side view of a partially formed integrated circuit 100 is illustrated. Masking layers 120, 130 may be provided above a substrate 110 to form guides for copolymer self-assembly. The materials for the layers 120, 130 overlying the substrate 110 are chosen based upon consideration of the interaction of the

layers with block copolymer materials to be used and of the chemistry and process conditions for the various pattern forming and pattern transferring steps discussed herein. For example, because patterns in upper layers are transferred to lower layers, the lower masking layer 130 is chosen so that it can be selectively etched relative to at least some of the other exposed materials. It will be appreciated that a material is considered selectively, or preferentially, etched when the etch rate for that material is at least about 2-3 times greater, or at least about 10 times greater, or at least about 20 times greater, or at least about 50 times greater than that for surrounding materials.

[0035] It will be appreciated that the "substrate" to which patterns are transferred may include a single material, a plurality of layers of different materials, a layer or layers having regions of different materials or different structures in them, etc. These materials may include semiconductors, insulators, conductors, or combinations thereof. For example, the substrate may comprise doped polysilicon, a single crystal electrical device active area, a silicide, or a metal layer, such as a tungsten, aluminum or copper layer, or combinations thereof. In some embodiments, the mask features discussed below may directly correspond to the desired placement of conductive features, such as interconnects, in the substrate. In other embodiments, the substrate may be an insulator and the location of mask features may correspond to the desired location of insulation between conductive features, such as in damascene metallization. The mask features may be used as a hard mask to directly etch the substrate, or may be used to transfer a pattern to another underlying layer, *e.g.*, a carbon layer, such as a transparent carbon, layer, which is then used to transfer the pattern to one or more underlying layers, such as the substrate.

[0036] With continued reference to Figure 1, the selectively definable layer 120 overlies a hard mask, or etch stop, layer 130, which overlies the substrate 110. The selectively definable layer 120 may be photodefinable, *e.g.*, formed of a photoresist, including any photoresist known in the art. For example, the photoresist may be any photoresist compatible with extreme ultraviolet systems (*e.g.*, 13.4 nm wavelength systems), 157 nm, 193 nm, 248 nm or 365 nm wavelength systems, or 193 nm wavelength immersion systems. Examples of photoresist materials include argon fluoride (ArF) sensitive photoresist, *i.e.*, photoresist suitable for use with an ArF light source, and krypton fluoride

(KrF) sensitive photoresist, *i.e.*, photoresist suitable for use with a KrF light source. ArF photoresists are used with photolithography systems utilizing relatively short wavelength light, *e.g.*, 193 nm. KrF photoresists are used with longer wavelength photolithography systems, such as 248 nm systems. In addition, while the use of self-organizing material and pitch multiplication in embodiments of the invention may obviate the need to define extremely small features with expensive, relatively new direct formation techniques such as extreme ultraviolet systems (including 13.4 nm wavelength systems) or electron beam lithographic systems, such systems may also be used, if desired. In addition, maskless lithography, or maskless photolithography, may be used to define the selectively definable layer 120. In other embodiments, the layer 120 and any subsequent resist layers may be formed of a resist that may be patterned by nano-imprint lithography, *e.g.*, by using a mold or mechanical force to form a pattern in the resist.

[0037] The material for the hard mask layer 130 may comprise an inorganic material, which is not a polymer. Exemplary materials include silicon oxide (SiO_2), silicon nitride, silicon or a dielectric anti-reflective coating (DARC), such as a silicon-rich silicon oxynitride. The hard mask layer 130 comprises silicon nitride in the illustrated embodiment. The material for the hard mask layer 130 is selected to interact with the later-deposited self-organizing material to direct the self-assembly of the self-organizing material into a desired pattern.

[0038] With reference to Figure 2, the photodefinable layer 120 is exposed to radiation through a reticle and then developed to leave a pattern comprising features 122 which are formed of photodefinable material. It will be appreciated that the pitch of the resulting features 122, *e.g.*, lines, is equal to the sum of the width of a line 122 and the width of a neighboring space 124. In some embodiments, the pitch of the features 122 may be, *e.g.*, about 400 nm or less, about 300 nm or less, about 200 nm or less, or about 100 or less. In an exemplary embodiment, the features 122 may have a critical dimension of about 140 nm and a pitch of about 280 nm.

[0039] With reference to Figure 3, the pattern in the photodefinable layer 120 is transferred to the hard mask layer 130, thereby forming hard mask features 132 in the hard mask layer 130. The pattern transfer may be accomplished using an anisotropic etch, such as

an etch using a fluorocarbon plasma, although a wet (isotropic) etch may also be suitable if the hard mask layer 130 is sufficiently thin. Exemplary fluorocarbon plasma etch chemistries include CFH_3, CF_2H_2, CF_3H and CF_4/HBr. With reference to Figure 4, resist forming the photodefinable layer 120 may also be removed, *e.g.*, by plasma ashing.

[0040] With reference to Figure 5, the hard mask features 132 (Figure 4) are trimmed to form guides 134 for copolymer self-assembly. The hard mask features 132 may be trimmed using a wet or dry etch which selectively etches the hard mask material relative to other exposed matrials. The trim etch may be performed using, *e.g.*, a SO_2/O_2/Ar plasma. The trim allows the formation of features having smaller critical dimensions than could easily be formed using conventional photolithography. For example, hard mask features 132 having a critical dimension of about 140 nm and a pitch of about 280 nm may be trimmed to form copolymer self-assembly guides 134 having a critical dimension of about 35 nm and the same pitch of about 280 nm. In other embodiments, the photoresist features 122 (Figure 2) may be trimmed in addition to, or instead of, the hard mask features 132, thereby allowing guides 134 of the desired size to be formed without the need to trim the hard mask features 132.

[0041] A self-organizing material, *e.g.*, block copolymers, is next applied and allowed to self-assemble to form a mask pattern over the substrate 110. Method for forming self-organized block copolymer patterns are disclosed in Block, IEE Transactions in Nanotechnology, Vol. 3, No. 3, September 2004 and in U.S. Patent Application Nos. 11/389,581 and 11/445,907, the entire disclosure of each of which is incorporated by reference herein.

[0042] With reference to Figure 6, a film 160 of block copolymer material is deposited between and over the guides 134. The copolymer comprises blocks of polymer material which may be selectively etched relative to one another and which may self-organize in a desired and predictable manner, *e.g.*, the blocks are immiscible and will segregate under appropriate conditions to form domains predominantly containing a single block species. In the exemplary illustrated embodiment, the copolymer is a diblock copolymer, comprising, *e.g.*, polystyrene (PS) and poly-methylmethacrylate (PMMA). The diblock copolymers may be provided dissolved in a solvent, *e.g.*, toluene. It will be appreciated that the total size of each diblock copolymer and the ratio of the constituent blocks and monomers may be chosen

to facilitate self-organization and to form organized block domains having desired dimensions. For example, it will be appreciated that a block copolymer has an intrinsic polymer length scale, the average end-to-end length of the copolymer in film, including any coiling or kinking, which governs the size of the block domains. A copolymer solution having longer copolymers may be used to form larger domains and a copolymer solution having shorter copolymers may be used to form smaller domains. In some embodiments, the copolymers are selected to provide mandrels that provide a consistent spacing between spacers 175 (Figure 12). In other embodiments, the block copolymers are selected to facilitate self-assembly into a desired pattern, the mandrels are trimmed, *e.g.*, by a wet or dry etch, to provide a desired spacing between mandrels. The block copolymers may be deposited by various methods, including, *e.g.*, spin-on coating, spin casting, brush coating or vapor deposition.

[0043] The thickness of the copolymer film 160 may be chosen based upon the desired pattern to be formed by the copolymers. It will be appreciated that, up to a particular thickness related to the polymer length scale and the environment in which the polymers are disposed, *e.g.*, the distance between and the height of the guides 134, the copolymers will typically orient to form alternating, substantially lamellar domains that form parallel lines, as viewed in a top-down view (Figure 8). Such lamellae may be used to pattern, *e.g.*, interconnects, or the lateral extension of the lamellae may be limited to form isolated features, *e.g.*, transistor gates. Under some conditions, related to the thickness of the film 160, the polymer length scale and the environment in which the polymers are disposed, the copolymers may orient to form vertically-extending pillars, such as cylinders, or spheres.

[0044] For forming lamellae, the copolymer film thickness may be less than about the length scale of the copolymers forming the film. For example, where the copolymer length scale is about 35 nm, the thickness of the films is about 35 nm or less, about 30 nm or less, or about 25 nm or less.

[0045] It will be appreciated that the thickness of the film 160 may be greater than, equal to or less than the height of the guides 134. As illustrated and discussed further below, a thickness which is greater than the height of the guides 134 may be used to provide a copolymer reservoir. In other embodiments, a thickness which is equal to, or less than the

height of the guides 134 may be used to form isolated islands of copolymers between the guides 134, thereby preventing cross-diffusion of copolymers between the islands.

[0046] While the invention is not bound by theory, it will be appreciated that the different block species are understood to self-aggregate due to thermodynamic considerations in a process similar to the phase separation of materials. The self-organization is guided by the guides 134, which encourage the constituent blocks of the block copolymers to orient themselves along the length of the guides 134 due to interfacial interactions. It will be appreciated that the self-organization may result in a more efficient packing of the copolymer species. As a result, in some cases, the free copolymers available for the self-organization may be depleted if the copolymer film 160 extends over too large of an expanse, causing an area in the middle of the expanse to be formed without organized copolymers or with poorly organized copolymers. Thus, in some embodiments, the copolymer film 160 is sufficiently thick to extend above the guides 134 to provide a reservoir of copolymers for the self-organization which occurs between the guides 134. In addition, the distance between the guides 134 may be chosen to be sufficiently small to minimize the depletion effect that may occur over large expanses.

[0047] With reference to Figure 7, the block copolymers in the copolymer film 160 are allowed to self-organize. The self-organization may be facilitated and accelerated by annealing the partially-fabricated integrated circuit 100. The temperature of the anneal may be chosen to be sufficiently low to prevent adversely affecting the block copolymers or the partially fabricated integrated circuit 100. The anneal may be performed at a temperature of less than about 250°C, less than about 200°C or about 180°C in some embodiments. The anneal may also be used to cause cross-linking of the copolymers, thereby stabilizing the copolymers for later etching and pattern transfer steps.

[0048] A pattern of lamellae resulting after the anneal is shown in Figure 7. Domains 162 of one block species, *e.g.*, PS, and domains 164 of the other block species, *e.g.*, PMMA, alternate between the guides 134. It will be appreciated that the sizes of the block domains are determined by the sizes of the block species forming them.

[0049] With reference to Figure 8, a top-down view of the partially fabricated integrated circuit of Figure 7 is shown. The PS domains 162 can be seen alternating with the PMMA domains 164. Both domains 162 and 164 extend along the length of the guides 134.

[0050] With reference to Figure 9, the domains 164 are selectively removed, leaving behind the domain 162 and the guides 134 (not shown), which can function as mandrels for pitch multiplication. It will be appreciated that the domains 164 may be removed in a single step using a single etch chemistry or may be removed using multiple etches with different etch chemistries. For example, where the domains 164 are formed of PMMA and the domains 162 are formed of PS, the domains 164 may be removed by performing a selective wet etch, *e.g.*, using acetic acid as an etchant. In other embodiments, a dry or anisotropic etch may be appropriate where one of the domains may be etched at a faster rate than the other. It will be appreciated that the dimensions of the resulting features may vary, depending on the size of the copolymer used and process conditions. In some embodiments, the resulting pattern may comprise PS domains having a critical dimension of about 50 nm to about 2 nm, about 35 nm or less to about 3 nm, with a pitch of about 100 nm to about 4 nm, or about 70 nm to about 6 nm. It will be appreciated that in other embodiments, the domains 162 and/or the guides 134 may be removed instead, thereby leaving the domains 164, with or without the guides 134.

[0051] Next, with reference to Figure 10, a layer 170 of spacer material is blanket deposited conformally over exposed surfaces, including the substrate 110. The spacer material may be any material that may act as a mask for transferring a pattern to an underlying material. The spacer material: 1) may be deposited with good step coverage; 2) may be deposited at a temperature compatible with the mandrels 162; and 3) may be selectively etched relative to the mandrels 162 and guides 134, if present, and the underlying substrate 110. The spacer material may be, without limitation, an inorganic material, such as a silicon-containing material, or an organic material, such as a polymer. The silicon-containing spacer materials may be, without limitation, silicon, silicon oxide and silicon nitride. In the illustrated embodiment, the spacer material is silicon oxide.

[0052] Methods for spacer material deposition include atomic layer deposition, *e.g.*, using a self- limiting deposition with a silicon precursor and a subsequent exposure to an

oxygen or nitrogen precursor to form silicon oxides and nitrides, respectively. ALD may be performed at relatively low temperatures, *e.g.*, under about 200°C or under about 100°C, which may prevent thermal damage to underlying thermally sensitive materials. For example, ALD may be used to prevent damage to the polymer material forming the block domains 162. In other embodiments, chemical vapor deposition is used to deposit the spacer material.

[0053] The thickness of the layer 170 is determined based upon the desired width of the spacers 175 (Figure 12). For example, in some embodiments, the layer 170 is deposited to a thickness of about 10-80 nm or about 20-50 nm to form spacers of roughly similar widths. The step coverage is about 80% or greater and or about 90% or greater.

[0054] With reference to Figures 11, the silicon oxide spacer layer 170 is then subjected to an anisotropic etch to remove spacer material from horizontal surfaces 180 of the partially formed integrated circuit 100. Such an etch, also known as a spacer etch, may be performed using a fluorocarbon plasma, *e.g.*, a CF_4, CHF_3 and/or NF_3 containing plasma.

[0055] With reference to Figure 12, the block domains 162 and any remaining guides 134 are removed to leave freestanding spacers 175. The block domains 162 and guides 134 may be removed by wet or dry etches that selectively remove those features relative to the spacers 175. The etches may also selectively remove the block domains 162 and guides 134 relative to the underlying substrate 110. Depending upon the material forming the block domains 162 and the guides 134, the same or different etch chemistries may be applied. Etch chemistries include, without limitation, a O_2-based carbon trip etch to remove the PS block domains 162 and a phosphoric acid based wet etch to remove the silicon nitride guides 134.

[0056] Thus, pitch–multiplied mask features have been formed. In the illustrated embodiment, the pitch of the spacers 175 is roughly half that of the block domains 162 (Figure 9) formed by the block copolymers. For example, where the block domains 162 had a pitch of about 200 nm, spacers 175 having a pitch of about 100 nm or less may be formed and where the block domains 162 had a pitch of about 60 nm or less, spacers 175 having a pitch of about 30 nm or less may be formed. It will be appreciated that because the spacers 175 are formed on the sidewalls of the block domains 162, the spacers 175 generally follow

the outline of the block domains 162 and, so, typically form a closed loop. The spacers 175 form a first pattern 177. It will be appreciated that higher orders of pitch multiplication can be achieved in some embodiments by using the spacers 175 as mandrels to form other spacers or mask features.

[0057] With reference to Figure 13, the pattern 177 is transferred to the substrate 110. The pattern transfer may be accomplished using etch chemistries appropriate for selectively etching the material or materials of the substrate 110 relative to the spacers 175. The skilled artisan can readily determine suitable etch chemistries for substrate materials. It will be appreciated that where the substrate 110 comprises layers of different materials, a succession of different chemistries, *e.g.*, dry-etch chemistries, may be used to successively etch through these different layers, if a single chemistry is not sufficient to etch all the different materials. It will also be appreciated that, depending upon the chemistry or chemistries used, the spacers 175 may be etched. In the illustrated embodiment, the spacers 175 are sufficiently tall to complete the etch of the substrate 110 without being completely worn away.

[0058] With reference to Figure 14, the mask overlying the substrate 110, including the domain 162 and the guides 134, are stripped, leaving the patterned substrate 110. After the pattern transfer, the partially fabricated integrated circuit 100 is subjected to subsequent processing steps, including forming ancillary electrical devices and electrical interconnects, to form a completed integrated circuit, *e.g.*, a memory chip.

[0059] It will be appreciated that various modifications of the illustrated embodiments are possible. For example, while discussed in the context of diblock copolymers for ease of illustration and discussion, the copolymers may be formed of two or more block species. In addition, while the block species of the illustrated embodiment are each formed of a different monomer, the block species may share monomer(s). For example, the block species may be formed of different sets of monomers, some of which are the same, or may be formed of the same monomer, but in a different distribution in each block. The different sets of monomers form blocks having different properties which may drive the self-assembly of the copolymers.

[0060] In some embodiments, a supplemental layer 180 of self-organizing material may be deposited over the block domains 162 and 164 and guides 134, to vertically extend the pattern defined by those block domains and the guides 134. The self-organizing material forming the supplement layer 180 may be a copolymer, such as a block copolymer. The material forming the supplemental layer 180 is chosen to interact with the block domains 162 and 164 and guides 134 such that the domains 162, 164 and the guides 134 are able to direct the organization of the self-organizing material. For example, where the block domains 162 and 164 and guides 134 include polar and non-polar block species, the layer 180 may also have polar and non-polar block species. In some embodiments, supplemental block copolymers forming the layer 180 are the same as the block copolymers of the film 160. A method for vertically extending a pattern formed of self-organizing material is disclosed in U.S. Patent Application No. 11/445,907 to Gurtej Sandhu, filed June 2, 2006, entitled Topography Based Patterning (Attorney Docket No. MICRON.349A), the entire disclose of which is incorporated herein by reference.

[0061] It will be appreciated that, before or after transferring the mask pattern 177 to the substrate 110, additional mask patterns can be overlaid the mask pattern 177 (Figure 11). For example, a planarizing material can be deposited between and over the spacers 175 and the planarizing material can be patterned to form an additional pattern. The additional pattern, forming a combined pattern with the mask pattern 177, can be transferred to the underlying substrate 110. With reference to Figure 15, the planarizing material can be photoresist, such as negative or positive photoresist. With reference to Figure 16, the photoresist can be patterned by exposure to radiation to form the additional pattern. Negative photoresist can be used in embodiments in which the features of the mask pattern 177 are very closely spaced, *e.g.*, having a pitch of about 40 nm or less. It has been found that positive photoresist can be difficult to remove between spacers with such small pitches, due to difficulties in completely exposing the photoresist to light. On the other hand increasing the light intensity may undesirably cause polymerization of the photoresist, due to optical amplification by some transparent spacer materials, such as silicon oxide. Negative photoresist does not need to be exposed to light for removal, thereby facilitating the removal

of photoresist between spacers and the formation of clean patterns in combination with the mask pattern 177.

[0062] In some embodiments, the hard mask layer 130 overlying the substrate may be omitted. For example, the photodefinable material may be formed of or replaced by a material which is compatible with the temperatures and other conditions for copolymer self-organization and/or the spacers 175 may be used as a mask for etching the substrate 110 where an etch having sufficient selectivity for the substrate 110 is available.

[0063] In some other embodiments, additional masking levels may be provided over the substrate 110. For example, additional hard mask layers can be provided between the spacers 175 and the substrate 110. The pattern 177 may be transferred to one or more additional hard mask layers before being transferred to the substrate 110. The additional hard mask layers may be selected to provide higher resistance to etches used for etching the substrate. For example, the pattern 177 may be transferred to an amorphous carbon layer before being transferred to the substrate 110. Amorphous carbon has been found to be suitable as a hard mask for etching a variety of silicon-containing materials.

[0064] Also, while "processing" through a mask layer may encompass etching an underlying layer, processing through the mask layers may involve subjecting layers underlying the mask layers to any semiconductor fabrication process. For example, processing may involve ion implantation, diffusion doping, depositing, oxidizing (particularly with use of a hard mask under the polymer mask), nitridizing, etc. through the mask layers and onto underlying layers. In addition, the mask layers may be used as a stop or barrier for chemical mechanical polishing (CMP) or CMP may be performed on any of the layers to allow for both planarization and etching of the underlying layers, as discussed in U.S. Patent Application No. 11/216,477, filed August 31, 2005, the entire disclosure of which is incorporated by reference herein.

[0065] In addition, while the illustrated embodiments may be applied to fabricate integrated circuits, embodiments of the invention may be applied in various other applications where the formation of patterns with very small features is desired. For example, embodiments of the invention may be applied to form gratings, disk drives, storage media or templates or masks for other lithography techniques, including X-ray or imprint

lithography. For example, phase shift photomasks may be formed by patterning a substrate that has a film stack having phase shifting material coatings.

[0066] Consequently, it will be appreciated from the description herein that the invention includes various embodiments. For example, according to some embodiments of the invention, a method for patterning a semiconductor substrate is provided. The method comprises providing a layer comprising block copolymers. One block of the block copolymers is selectively removed to leave laterally separated mandrels comprising an other block of the block copolymers. Spacer material is blanket depositing on the mandrels. The spacer material is etched to form spacers on sidewalls of the mandrels. A pattern defined by the spacers is transferred to the substrate.

[0067] According to other embodiments the invention, a method for forming a mask for patterning a substrate is provided. The method comprises providing a layer of a self-organizing material. Like chemical species of the self-organizing material are aggregated to form a repeating pattern having domains defined by the chemical species. One of the chemical species is preferentially removed to form spaced apart mandrels Spacers are formed on sidewalls of the mandrels.

[0068] According to yet other embodiments of the invention, a method for integrated circuit fabrication is provided. The method comprises exposing a block copolymer layer to a wet etch to define free-standing, regularly-spaced, spaced-apart placeholders in the block copolymer layer. Spacers are formed on sidewalls of the placeholders. A pattern derived from the spacers is transferred to an underlying substrate.

[0069] In addition to the above disclosure, it will also be appreciated by those skilled in the art that various omissions, additions and modifications may be made to the methods and structures described above without departing from the scope of the invention. All such modifications and changes are intended to fall within the scope of the invention, as defined by the appended claims.

WE CLAIM:

1. A method for patterning a semiconductor substrate, comprising:

providing a layer comprising block copolymers;

selectively removing one block of the block copolymers to leave laterally-separated mandrels comprising an other block of the block copolymers;

blanket depositing spacer material on the mandrels;

etching the spacer material to form spacers on sidewalls of the mandrels; and

transferring a pattern defined by the spacers to the substrate.

2. The method of Claim 1, wherein providing the layer formed of block copolymers comprises:

depositing a block copolymer solution over the substrate; and

segregating blocks constituting the block copolymers to form a repeating pattern defined by blocks of the copolymers over the substrate.

3. The method of Claim 2, wherein providing the layer formed of block copolymers further comprises providing laterally spaced apart copolymer self-assembly guides over the substrate, wherein depositing the block copolymer solution comprises depositing the block copolymer solution between the copolymer segregation guides.

4. The method of Claim 3, wherein the guides are formed of a material which attracts or repels a block forming the block copolymers.

5. The method of Claim 3, wherein the guides are formed of a material selected from the group consisting of silicon oxide, silicon and a dielectric anti-reflective coating.

6. The method of Claim 1, further comprising removing the mandrels before transferring the pattern defined by the spacers to the substrate.

7. The method of Claim 6, further comprising transferring the pattern defined by the spacers to an underlying hard mask layer before transferring the pattern defined by the spacers to the substrate.

8. The method of Claim 7, wherein the hard mask layer comprises amorphous carbon.

9. The method of Claim 1, further comprising:

depositing a selectively-definable material over the spacers; and

defining an other pattern in the selectively-definable material,

wherein transferring the pattern defined by the spacers to the substrate comprises transferring a combined pattern formed from the pattern and the other pattern to the substrate.

10. The method of Claim 9, wherein the selectively-definable layer is deposited on and between the spacers.

11. The method of Claim 10, wherein the selectively-definable layer is photoresist.

12. The method of Claim 11, wherein the photoresist is negative photoresist.

13. The method of Claim 9, further comprising transferring the combined pattern formed from the pattern and the other pattern to an underlying hard mask layer before transferring the combine pattern to the substrate.

14. The method of Claim 9, wherein transferring the combined pattern to the substrate transfers the pattern defined by the spacers to an array region of a partially-fabricated integrated circuit and transfers the other pattern to a periphery region of the partially-fabricated integrated circuit.

15. The method of Claim 1, wherein transferring the pattern defined by the spacers to the substrate defines interconnects in the substrate.

16. A method for forming a mask for patterning a substrate, comprising:

providing a layer of a self-organizing material;

aggregating like chemical species of the self-organizing material to form a repeating pattern having domains defined by the chemical species;

preferentially removing one of the chemical species to form spaced apart mandrels; and

forming spacers on sidewalls of the mandrels.

17. The method of Claim 16, wherein the self-organizing material comprises a block copolymer.

18. The method of Claim 17 wherein the block copolymer is a diblock copolymer.

19. The method of Claim 18, wherein the diblock copolymer comprises polystyrene.

20. The method of Claim 19, wherein the diblock copolymer further comprises polymethylmethacrylate.

21. The method of Claim 16, further comprising extending a height of the repeating pattern defined by the chemical species.

22. The method of Claim 21, wherein extending the height of the repeating pattern defined by the chemical species comprises:

depositing additional self-organizing material over the repeating pattern defined by the chemical species; and

aligning like chemical moieties of the additional self-organizing material with the domains defined by the chemical species.

23. The method of Claim 22, wherein the self-organizing material and the additional self-organizing material are block copolymers.

24. The method of Claim 23, wherein the self-organizing material and the additional self-organizing material are a same block copolymers.

25. The method of Claim 22, wherein preferentially removing one of the chemical species comprises etching like chemical moieties of the additional self-organizing material and etching one of the chemical species.

26. A method for integrated circuit fabrication, comprising:

exposing a block copolymer layer to a wet etch to define free-standing, regularly-spaced, spaced-apart placeholders in the block copolymer layer;

forming spacers on sidewalls of the placeholders; and

transferring a pattern derived from the spacers to an underlying substrate.

27. The method of Claim 26, wherein the wet etch comprises acetic acid.

28. The method of Claim 27, wherein the block copolymer comprises blocks of polystyrene and polymethylmethacrylate.

29. The method of Claim 26, wherein the placeholders have a pitch of about 100 nm or less.

30. The method of Claim 29, wherein the placeholders have a pitch of about 50 nm or less.

31. The method of Claim 26, wherein the free-standing, spaced-apart placeholders comprise vertical lamellae.

32. The method of Claim 26, wherein the free-standing, spaced-apart placeholders comprise vertically extending isolated pillars.

33. The method of Claim 26, wherein the transferring the pattern comprises defining regularly spaced features in an array region of a partially fabricated intergrated circuit.

34. The method of Claim 26, wherein forming spacers comprises:

blanket depositing a layer of spacer material over the placeholders; and

anisotropically etching the layer of spacer material.

35. The method of Claim 26, further comprising, before exposing the block copolymer layer to the wet etch:

depositing a solution of block copolymers over the substrate; and

annealing the block copolymer solution to cause self-assembly of the block copolymers into regularly-spaced block domains.

36. The method of Claim 3, wherein depositing the block copolymer solution between the copolymer segregation guides comprises forming a block copolymer reservoir directly over the guides.