

Anti-Static Coating

Introduction

The present invention relates to improved coatings to reduce electrostatic charging
5 and discharge and methods for producing such coatings.

Background to the Invention

A large variety of deposition techniques are used to coat substrates. Vapor deposition
technology is typically used to form thin film deposition layers in various types of
10 applications, including microelectronic applications and heavy-duty applications. Such
deposition technology can be classified in two main categories. A first category of such
deposition technology is known as Chemical Vapor Deposition (CVD). CVD generally
refers to deposition processes occurring due to a chemical reaction. Common
examples of CVD processes include semiconducting Si layer deposition, epitaxy and
15 thermal oxidation.

A second category of deposition is commonly known as Physical Vapor Deposition
(PVD). PVD generally refers to the deposition of solid substances occurring as a result
of a physical process. The main concept underlying the PVD processes is that the
20 deposited material is physically transferred onto the substrate surface via direct mass
transfer. Typically, no chemical reaction takes place during the process and the
thickness of the deposited layer is independent of chemical reaction kinetics as
opposed to CVD processes.

25 Sputtering is a known physical vapor deposition technique for depositing compounds
on a substrate, wherein atoms, ions or molecules are ejected from a target material
(also called the sputter target) by particle bombardment so that the ejected atoms or
molecules accumulate on a substrate surface as a thin film.

30 Another known physical vapor deposition technique is cathodic vapor arc (CVA)
deposition methods. In this method, an electric arc is used to vaporize material from a
cathode target. Consequently, the resulting vaporized material condenses on a
substrate to form a thin film of coating.

Amorphous carbon is a free, reactive form of carbon which does not have a crystalline form. Various forms of amorphous carbon films exist and these are usually categorised by the hydrogen content of the film and the $sp^2:sp^3$ ratio of the carbon atoms in the film.

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In an example of the literature in this field, amorphous carbon films are categorised into 7 categories (see table below taken from "Name Index of Carbon Coatings" from Fraunhofer Institut Schich- und Oberflächentechnik):

Amorphous Carbon Films						
Hydrogen-Free			Hydrogenated			
Unmodified		Modified	Unmodified		Modified with	
		With metals			Metals	Non-metals
sp^2	sp^3	sp^2	sp^2 or sp^3	sp^3	sp^2	sp^2
Hydrogen-free amorphous carbon	Tetrahedral, hydrogen-free amorphous carbon	Metal-containing, hydrogen-free amorphous carbon	Hydrogenated amorphous carbon	Tetrahedral, hydrogenated amorphous carbon	Metal-containing, hydrogenated amorphous carbon	Non-metal containing hydrogenated amorphous carbon
a-C	ta-C	a-C:Me	a-C:H	ta-C:H	a-C:H:Me	a-C:H:X

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Tetrahedral hydrogen-free amorphous carbon (ta-C) is characterised in that it contains little or no hydrogen (less than 5%mol, typically less than 2%mol) and a high content of sp^3 hybridised carbon atoms (typically greater than 80% of the carbon atoms being in the sp^3 state).

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Whilst the term "diamond-like carbon" (DLC) is sometimes used to refer to all forms of amorphous carbon materials, the term as used herein refers to amorphous carbon materials other than ta-C. Common methods of DLC manufacture use hydrocarbons (such as acetylene), hence introducing hydrogen into the films (in contrast to ta-C films in which the raw material is typically hydrogen free high purity graphite).

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In other words, DLC typically has an sp^2 carbon content of greater than 50% and/or a hydrogen content of 20%mol and above. The DLC may be undoped or doped with metals or non-metals (see table above).

In recent years, the manufacture of electrical components has moved towards a greater reliance on automation, in order to lower staffing costs and reduce the risk of contamination posed by human presence and manual handling within the cleanroom. In particular, this move towards a greater reliance on automation has happened in the semiconductor manufacturing industry.

Automated robotic equipment now delivers the many process steps it takes to produce a finished semiconductor product wafer. This means there are now many more “pick-and-place” operations, moving the wafer from the front opening unified pod (FOUP) into the process system or an analytical tool. The scale of repetitive mechanical handling and movement throughout the manufacturing process is a significant factor in the potential for device damage in semiconductor production; through electrostatic charging and subsequent discharge (ESD) or electrostatic attraction of particles.

Semiconductor chip and wafer products are susceptible to static electricity, especially during handling and shipping. Electrostatic discharge can change the electrical characteristics of a semiconductor device in a degrading way and even destroy it. A build up of electrostatic charge and the subsequent electrostatic discharge is the main failure cause in the semiconductor industry.

At present, most of the static dissipative methods on the market are based on “wet” processes of spraying the integrated circuit and wafer products with anti-static coatings. However, these are known to have low surface wear resistance, reducing the lifetime of these products.

Current static dissipative methods involve coating the products being manufactured themselves. This can affect the properties of the resulting product and consequently reduce the quality and/or lifetime of these products.

There therefore exists the need for coatings which reduce electrostatic charging and discharge, but do not have the above-mentioned issue of low surface wear resistance or other disadvantages to the products being manufactured.

An object of the present invention is to provide coatings that are an alternative to and preferably offer improvements in relation to reducing the build up of electrostatic charge and therefore reducing electrostatic discharge (ESD), addressing one or more problems identified in the art.

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The Invention

The inventors of the present application have found that carbon coatings with one or more layers of ta-C and one or more layers of DLC have suitable static dissipative properties in order to reduce electrostatic build-up and subsequent electrostatic discharge.

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Accordingly, the present invention provides a substrate with a multi-layer coating, comprising in order:

- i. a substrate,
- 15 ii. a seed layer,
- iii. a ta-C containing layer, and
- iv. a DLC containing layer,

wherein the coating has a surface electrical resistance of from $10^5 \Omega/\text{sq}$ to $10^9 \Omega/\text{sq}$.

20 Similarly provided is a coating for a substrate, comprising in order:

- i. a seed layer,
- ii. a ta-C containing layer, and
- iii. a DLC containing layer,

wherein the coating has a surface electrical resistance of from $10^5 \Omega/\text{sq}$ to $10^9 \Omega/\text{sq}$.

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Suitably, as illustrated in the examples, the present invention provides a coated substrate, comprising in order:

- i. a metal substrate,
- ii. a conductive metal seed layer (e.g. titanium or chromium),
- 30 iii. a ta-C containing layer, and
- iv. a DLC containing layer,

wherein the coating has a surface electrical resistance of from $10^5 \Omega/\text{sq}$ to $10^9 \Omega/\text{sq}$.

The present invention additionally provides a coated substrate, comprising in order:

- i. a substrate comprising silicon or glass,
 - ii. a seed layer comprising silicon,
 - iii. a ta-C containing layer, and
 - iv. a DLC containing layer,
- 5 wherein the coating has a surface electrical resistance of from $10^5 \Omega/\text{sq}$ to $10^9 \Omega/\text{sq}$.

Also provided is a method of making a coated substrate, comprising providing the substrate, and coating onto the substrate, in order:

- i. a seed layer,
- 10 ii. a ta-C containing layer, and
- iii. a DLC containing layer

wherein the coating has a surface electrical resistance of from $10^5 \Omega/\text{sq}$ to $10^9 \Omega/\text{sq}$.

The surface electrical resistance can be altered by changing the thickness of the DLC
15 containing layer within the coating. The surface electrical resistance can also be altered by changing one or more of the CVD source design, the coating temperature, the gas flow, the bias voltage and the duty cycle. Thus, the invention provides static dissipative coatings with a tuneable surface resistance. These coatings reduce electrostatic build-up and subsequent electrostatic discharge, as illustrated by the
20 testing of embodiments of the invention described in more detail below.

Detailed Description of the Invention

As discussed above, the term “tetrahedral amorphous carbon” (ta-C or TAC) as used herein refers to amorphous carbon having a low hydrogen content and a low sp^2
25 carbon content.

Ta-C is a dense amorphous material described as composed of disordered sp^3 , interlinked by strong bonds, similar to those that exist in disordered diamond (see Neuville S, “New application perspective for tetrahedral amorphous carbon coatings”,
30 QScience Connect 2014:8, <http://dx.doi.org/10.5339/connect.2014.8>). Due to its structural similarity with diamond, ta-C also is a very hard material with hardness values often greater than 30 GPa.

For example, the ta-C may have a hydrogen content less than 10%, typically 5% or less, preferably 2% or less (for example 1% or less). The percentage content of hydrogen provided here refers to the molar percentage (rather than the percentage of hydrogen by mass). The ta-C may have an sp² carbon content less than 30%, typically 20% or less, preferably 15% or less. Preferably, the ta-C may have a hydrogen content of 2% or less and an sp² carbon content of 15% or less. The ta-C is preferably not doped with other materials (either metals or non-metals).

By contrast, the term “diamond-like carbon” (DLC) as used herein refers to amorphous carbon other than ta-C. Accordingly, DLC has a greater hydrogen content and a greater sp² carbon content than ta-C. For example, the DLC may have a hydrogen content of 20% or greater, typically 25% or greater, for example 30% or greater. The percentage content of hydrogen provided here again refers to the molar percentage (rather than the percentage of hydrogen by mass). The DLC may have an sp² carbon content of 50% or greater, typically 60% or greater. Typically, the DLC may have a hydrogen content of greater than 20% and an sp² carbon content of greater than 50%. The DLC may be undoped or doped with metals and/or non-metals.

The invention advantageously provides static dissipative coatings that lead to a reduced build up in electrostatic charge and therefore reduced electrostatic discharge.

Accordingly, the present invention provides a substrate with a multi-layer coating, comprising in order:

- i. a substrate,
- ii. a seed layer,
- iii. a ta-C containing layer, and
- iv. a DLC containing layer,

wherein the coating has a surface electrical resistance of from 10⁵ Ω/sq to 10⁹ Ω/sq.

DLC containing layer

The DLC containing layer allows coatings of the invention to conduct electricity. This is required in order for the coating to act as a static dissipative coating, by preventing electrostatic build-up and subsequent electrostatic discharge.

The uppermost layer of the coating (i.e. the layer exposed to the atmosphere) is a DLC containing layer. In preferred embodiments, the DLC containing layer is adjacent the ta-C containing layer. The layer may comprise greater than 70%, for example greater than 80%, preferably greater than 90% DLC by weight or the layer may consist of DLC.

- 5 In preferred embodiments, the DLC containing layer consists of DLC.

The DLC may have a hydrogen content of 20% or greater, typically 25% or greater, for example 30% or greater. The percentage content of hydrogen provided here again refers to the molar percentage (rather than the percentage of hydrogen by mass).

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The DLC may have an sp^2 carbon content of 60% or greater, typically 70% or greater, preferably 80% or greater or 90% or greater.

The DLC may have an sp^3 carbon content of 40% or less, typically 30% or less, preferably 20% or less or 10% or less.

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Typically, the DLC may have a hydrogen content of greater than 20% and an sp^2 carbon content of greater than 50%.

- 20 In particularly preferred embodiments, the DLC containing layer consists of DLC, wherein the DLC has a hydrogen content of greater than 20% and an sp^2 carbon content of greater than 50%.

The DLC may be undoped or doped with metals and/or non-metals.

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The DLC is usually deposited by a CVD method (preferably PACVD), as described in further detail below. The DLC containing layer is typically deposited by a method other than FCVA.

- 30 The DLC containing layer typically has a thickness of 0.5 μm or more, for example 1.0 μm or more, preferably 1.5 μm or more. The DLC coating also typically has a thickness of 4.5 μm or less, for example 4.0 μm or less, preferably 3.5 μm or less. Accordingly, the DLC coating may have a thickness of from 0.5 μm to 4.5 μm , for example from 1.0 μm to 4.0 μm , preferably from 1.5 μm to 3.5 μm .

Ta-C containing layer

The ta-C containing layer increases the hardness and therefore the wear resistance of coated substrates of the invention. This in turn increases the lifetime of coated substrates of the invention. The ta-C containing layer also increases the adhesion of the DLC layer to the seed layer, reducing delamination and consequently increasing the lifetime of coated substrates of the invention.

Typically, the ta-C containing layer is adjacent the DLC containing layer. Typically, the ta-C containing layer is adjacent the seed layer. In preferred embodiments, the ta-C containing layer is adjacent the DLC containing layer and the seed layer.

The ta-C containing layer may comprise greater than 70%, for example greater than 80%, preferably greater than 90% ta-C by weight or the layer may consist of ta-C. In preferred embodiments, the ta-C containing layer consists of ta-C.

The ta-C typically has a hydrogen content of 5% or less, preferably 2% or less and most preferably 1% or less.

The ta-C typically has an sp^2 carbon content of 20% or less, preferably 15% or less.

The ta-C typically has an sp^3 carbon content of 80% or greater, preferably 85% or greater.

Typically, the ta-C may have a hydrogen content of 5% or less and an sp^2 carbon content of 20% or less, preferably the ta-C may have a hydrogen content of 2% or less and an sp^2 content of 15% or less.

In particularly preferred embodiments, the ta-C containing layer consists of ta-C, wherein the ta-C has a hydrogen content of 5% or less and an sp^2 carbon content of 20% or less.

The thickness of the ta-C containing layer is typically 0.01 μm or more, for example 0.05 μm or more, preferably 0.1 μm or more. The ta-C containing layer also typically

has a thickness of 2.0 μm or less, for example 1.5 μm or less, preferably 1.0 μm or less. Accordingly, the ta-C containing layer may have a thickness of from 0.01 μm to 2.0 μm , for example from 0.05 μm to 1.5 μm , preferably from 0.1 μm to 1.0 μm .

- 5 The ta-C is preferably deposited via a PVD method, such as an CVA method (preferably FCVA).

Seed Layer

- 10 A seed layer is included to promote adhesion of ta-C containing layer to the underlying substrate. The seed layer increases adhesion between the substrate and the ta-C containing layer. This reduces the likelihood of delamination of the coating from the substrate.

- 15 Typically, the seed layer is adjacent the ta-C containing layer. Typically, the seed layer is adjacent the substrate. In preferred embodiments, the seed layer is adjacent the ta-C containing layer and the substrate.

- The seed layer is also typically conductive to provide an electrically conductive surface onto which the carbon-containing ta-C and DLC layers can be deposited.

- 20 The nature of the seed layer will therefore depend on the nature of the substrate. The thickness of the seed layer is typically 0.05 μm or more, for example 0.1 μm or more, preferably 0.3 μm or more. The thickness of the seed layer is also typically 2 μm or less, for example, 1 μm or less, preferably 0.8 μm or less. Accordingly, the thickness of the seed layer may be from 0.05 μm to 2 μm , for example from 0.1 μm to 1 μm , preferably from 0.3 μm to 0.8 μm .

- 30 Typically, the seed layer is a conductive metal. Typically, when the substrate is metallic, the seed layer is a conductive metal. When the substrate is metallic, the seed layer preferably comprises Ti or Cr. In the most preferred embodiments, when the substrate is metallic, the seed layer is Ti. When the substrate is silicon or glass, the seed layer typically comprises silicon.

The seed layer is typically deposited by a PVD method and preferably the seed layer is deposited by sputtering.

Substrate

- 5 Choice of the substrate material is broad, and many substrates made of a wide range of materials can be coated. The substrate is usually metallic and generally is or comprises a metal, an alloy, silicon, or glass.

10 In one embodiment suitable substrates include steels (e.g. steel, stainless steel, HSS, tool steel and alloy steel), copper or its alloys and aluminium or its alloys. Articles are generally made of the substrate and then have a coating of the invention applied / deposited.

In another embodiment suitable substrates include silicon and glass.

- 15 The substrate may be any apparatus where electrostatic discharge could be problematic, for example apparatus that comes into contact with semiconductors.

20 It is noted that the coating may be applied to the equipment rather than the products within the manufacturing apparatus. Therefore, preventing the need for antistatic coatings to be applied to the manufacturing products. This advantageously prevents any disadvantages associated with coating the products themselves. In particular, the quality and/or lifetime of these products is not reduced. In fact, the coatings on the equipment serve to increase the lifetime of the products being manufactured.

Overall Coated Substrate

- 25 The overall thickness of the coating (including seed layer, DLC containing layer and ta-C containing layer) is typically 0.7 μm or more, suitably 1.0 μm or more, for example 2.0 μm or more, preferably 3.0 μm or more. The overall thickness of the coating is also typically 9.0 μm or less, suitably 7.0 μm or less, for example 5.0 μm or less, preferably 4.0 μm or less. Accordingly, the overall thickness of the coating may be from 0.7 μm to 9.0 μm , suitably from 1.0 μm to 7.0 μm , for example from 2.0 μm to 5.0 μm , preferably 3.0 μm to 4.0 μm .

The coated substrate has tuneable electrical resistance, depending on the thickness of the DLC containing layer. The temperature and speed of application of the DLC containing layer may also affect the surface electrical resistance of the coated substrate. Typically, the coating has a surface electrical resistance of from $10^4 \Omega/\text{sq}$ to $10^{12} \Omega/\text{sq}$, suitably from $10^5 \Omega/\text{sq}$ to $10^{10} \Omega/\text{sq}$, preferably from $10^5 \Omega/\text{sq}$ to $10^9 \Omega/\text{sq}$ and most preferably from $10^6 \Omega/\text{sq}$ to $10^7 \Omega/\text{sq}$.

The coating typically has a hardness of 500 HV or more, preferably 1000 HV or more, most preferably 1500 HV or more. The coating also typically has a hardness of 3500 HV or less, preferably 3000 HV or less, most preferably 2000 HV or less. Accordingly, the coating may have a hardness of from 500 HV to 3500 HV, preferably from 1000 HV to 3000 HV, most preferably from 1500 HV to 2000 HV.

Hardness is suitably measured using the Vickers hardness test (developed in 1921 by Robert L. Smith and George E. Sandland at Vickers Ltd; see also ASTM E384-17 for standard test), which can be used for all metals and has one of the widest scales among hardness tests. The unit of hardness given by the test is known as the Vickers Pyramid Number (HV) and can be converted into units of pascals (GPa). The hardness number is determined by the load over the surface area of the indentation used in the testing. As examples, Martensite a hard form of steel has HV of around 1000 and diamond can have a HV of around 10,000 HV (around 98 GPa). Hardness of diamond can vary according to precise crystal structure and orientation but hardness of from about 90 to in excess of 100 GPa is common.

Typically, the ta-C containing layer and DLC containing layer are adjacent, i.e. there are no layers present between the ta-C containing layer and DLC containing layer. In addition, the seed layer and ta-C containing layer are preferably adjacent, i.e. there are no layers present between the seed layer and ta-C containing layer. The substrate and seed layer are preferably also adjacent, i.e. there are no layers present between the substrate and seed layer.

In preferred embodiments, the seed layer and ta-C containing layer are adjacent and the ta-C containing layer and DLC containing layer are adjacent. In other embodiments, the substrate and seed layer are adjacent and the ta-C containing layer

and DLC containing layer are adjacent. In other embodiments, the substrate and seed layer are adjacent and the seed layer and ta-C containing layer are adjacent. In particularly preferred embodiments, the substrate and seed layer are adjacent, and the seed layer and ta-C containing layer are adjacent, and the ta-C containing layer and DLC containing layer are adjacent.

In one embodiment of the invention a coated substrate is provided consisting of, in order:

- i. a substrate,
- ii. a seed layer,
- iii. a ta-C containing layer, and
- iv. a DLC containing layer,

wherein the coating has a surface electrical resistance of from $10^5 \Omega/\text{sq}$ to $10^9 \Omega/\text{sq}$.

The substrate, seed layer, ta-C containing layer and DLC containing layer may have the properties described above.

In further embodiments, the invention provides a coated substrate comprising in order:

- i. a metal substrate,
- ii. a conductive metal seed layer (e.g. titanium or chromium),
- iii. a ta-C containing layer, and
- iv. a DLC containing layer.

In another embodiment the invention provides a coated substrate comprising in order:

- i. a substrate comprising silicon or glass,
- ii. a seed layer comprising silicon,
- iii. a ta-C containing layer, and
- iv. a DLC containing layer.

Method

The invention additionally provides a method of making a coated substrate according to the disclosure above, comprising providing the substrate, and coating onto the substrate, in order:

- i. a seed layer,

- ii. a ta-C containing layer, and
- iii. a DLC containing layer

wherein the coating has a surface electrical resistance of from $10^5 \Omega/\text{sq}$ to $10^9 \Omega/\text{sq}$ (e.g. from $10^6 \Omega/\text{sq}$ to $10^7 \Omega/\text{sq}$).

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Conventional CVD and PVD methods, specifically CVA and FCVA processes, are known and used for a wide range of substrates and the methods of the invention are similarly suitable for coating a wide range of substrates. Solids, both conducting and non-conducting, are generally suitable and seed layers and adhesion layers can be used to improve coating adhesion and strength, and to render surfaces amenable to being coated. Substrates made of metal, alloy, ceramics and mixtures thereof can be coated. Typically, the substrate is prone to a build-up of electrostatic charge and therefore subsequent electrostatic discharge.

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- 15 Coating processes described herein may all be carried out at low temperature, for example at temperatures of 100°C or less, for example at temperatures of 70°C . Coating processes described herein may alternatively be carried out at temperatures of from 80°C to 220°C , optionally from 100°C to 200°C , typically from 100°C to 150°C , preferably from 110°C to 130°C , more preferably from 115°C to 125°C (e.g. 120°C).
- 20 This is an advantage since the method of coating the substrate may consequently be carried out at relatively low temperatures, in order to avoid the energy costs associated with the coating process.

- Coatings of the invention can be multilayered and the respective layers may independently be deposited using a range of known and conventional deposition techniques, including CVD, PVD, magnetron sputtering and multi-arc ion plating. Sputtering is one suitable method, especially for the seed layer. PVD is suitably used for the ta-C containing layers, e.g. CVA. The CVA process is typically a filtered cathodic vacuum arc (FCVA) process, e.g. as described below. Apparatus and methods for FCVA coatings are known and can be used as part of the methods of the invention. The FCVA coating apparatus typically comprises a vacuum chamber, an anode, a cathode assembly for generating plasma from a target and a power supply for biasing the substrate to a given voltage. The nature of the FCVA is conventional and not a part of the invention.

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CVD processes can make use of ion sources (including end-hall ion sources, Kaufman ion sources, anode layer sources, hot filament ion sources and hollow cathode ion sources) for the material being deposited. The CVD process may preferably be a plasma activated CVD process (PACVD, also referred to as a plasma enhanced CVD, PECVD). PACVD processes have a lower deposition temperature, higher purity and allow easier control of the reaction parameters compared to conventional (i.e. thermally activated) CVD processes. PACVD processes additionally have higher coating energy, resulting in better coating adhesion and greater coating hardness and density compared to conventional CVD processes. PACVD processes may also lead to better coating coverage and uniformity compared to conventional CVD processes. Alternatively, the coating material may be provided as a gas which is then charged/ionised using a power supply (e.g. DC power supply, pulsed DC power supply or RF power supply).

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In preferred embodiments the seed layer is deposited by sputtering. In other preferred embodiments the ta-C containing layer is deposited by FCVA. In further preferred embodiments the DLC containing layer is deposited by CVD, most preferably PACVD.

The surface electrical resistance (also referred to as surface resistance or sheet resistance) of the coating is determined by controlling the thickness of the DLC containing layer, controlling the speed and temperature of application of this layer, and controlling the gas flow, bias voltage and duty cycle during application of the DLC containing layer. Therefore, the method disclosed herein may include varying the thickness of the DLC layer in order to obtain a coated substrate with desired electrical resistance. The method may further include independently varying one or more of the temperature, gas flow, bias voltage and duty cycle of the application of the DLC containing layer in order to obtain a coated substrate with desired electrical resistance.

Increasing the thickness of the DLC containing layer, decreases the conductance of the coating and therefore increases the surface electrical resistance of the coating. Without wishing to be bound by theory, this is because increasing the thickness of the DLC containing layer increases the thickness of the conducting layer, and surface electrical resistance is inversely proportional to thickness.

The methods may also include independently varying the speed and/or temperature of application of the DLC and/or ta-C in order to obtain a coated substrate with desired electrical resistance. Suitable temperature ranges for depositing the DLC containing
5 layer are discussed above, since the same (or a similar) temperature may be used for the whole coating process.

During CVD deposition of the DLC containing layer, there is controlled gas flow through the deposition chamber. Gas flow may be from 50sccm to 200sccm, typically
10 from 75sccm to 150sccm, preferably from 80sccm to 120sccm, most preferably from 90sccm to 110sccm. The gas used may be selected from CH₄, C₂H₆ or C₂H₂, preferably the gas is C₂H₂. In preferred embodiments of the CVD deposition of the DLC containing layer as described herein, the gas is C₂H₂ and the gas flow is from 90sccm to 110sccm (e.g. 100sccm).

15 Deposition of the DLC containing layer as described herein, may be carried out at a negative bias voltage of from -50V to -1200V, optionally from -200V to -1200V, typically from -500V to -1200V, preferably from -800V to -1200V, most preferably from -1000V to -1200V. A duty cycle of from 3.2% to 100% may be used for deposition of
20 the DLC containing layer. Optionally the duty cycle is from 3.2% to 75%, typically from 3.2% to 50%, preferably from 3.2% to 20% and most preferably from 3.2% to 10%. In preferred embodiments of the CVD deposition of the DLC containing layer as described herein, the bias voltage is from -1000V to -1200V (e.g. -1200V) and the duty cycle is from 3.2% to 10% (e.g. 3.2%).

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Brief Description of the Drawings

Figure 1 shows a coating apparatus for producing coated substrates of the invention.

Examples

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Example 1 – Coating Method (1)

A coated substrate was produced using a coating apparatus having a Ti sputtering source, two FCVA sources, a CVD source and an ion beam source positioned around a central coating chamber as shown in Figure 1.

- 5 The coating apparatus 1 features a central coating chamber 6. Around the coating chamber there is an ion beam source 2, two FCVA sources 3 and a sputtering source 4. In use, a substrate (not shown) is mounted onto a coating fixture (not shown), the coating fixture is then loaded into the coating chamber and positioned centrally on the platform 5. The coating chamber 6 may then be sealed and pumped down to the
10 required vacuum before the substrate is coated.

The substrate was coated by carrying out the following steps in order:

1. A pre-cleaned steel substrate was mounted onto the coating fixture (also referred to as a substrate holder).
- 15 2. The coating fixture with mounted substrate was loaded into the coating chamber and this was pumped down to the vacuum required (see below for required pressure for each step). The heater temperature was set to 100°C and this was maintained throughout the coating process.
3. The substrate was etched using an ion beam source.
- 20 4. A Ti layer was applied by sputtering with a Ti target, until the desired thickness was achieved. The chamber pressure was around 2.0×10^{-3} Torr during sputtering. During the sputtering step, the substrate holder was biased at -300V with a 50% duty cycle.
5. A ta-C layer was applied by FCVA using a graphite source, until the desired
25 thickness was achieved. The FCVA coating pressure was below 2.0×10^{-5} Torr during FCVA. During the FCVA step, the substrate holder was biased at -1200V with a 3.2% duty cycle.
6. A DLC layer was applied by CVD with a C₂H₂ CVD source, until the desired thickness was achieved. The CVD pressure was around 2.0×10^{-3} Torr. During
30 the CVD step, the substrate holder was biased at -1200V with a 3.2% duty cycle.
7. The vacuum was relieved and the mounted coated substrate was removed from the coating chamber.
8. The coated substrate was removed from the coating fixture.

The resulting coated substrate had the following properties:

<u>Layer</u>	<u>Thickness</u>
DLC	2500 nm
Ta-C	400 nm
Ti	500 nm
Substrate	
Total Thickness	3400 nm

The DLC layer had a Young's modulus of 90 GPa and a density of 2.410 kg/m³. Some
5 further testing was carried out on the coated substrate and details of this are provided
below.

Example 2 – Testing Surface Electrical Resistance

Surface electrical resistance was measure using a PRS-801 Resistance System, and
10 the surface electrical resistance was measured to be $5.7 \times 10^7 \Omega/\text{sq}$.

Example 3 – Testing Hardness

The hardness of the coating of the invention described in example 1 was determined
using an NMT3 nano indentation tester with a maximum load of 500mN. However,
15 only 4mN were used to measure hardness. A load/unload rate of 16mN/min and a
pause of 30 seconds were used. From the loading/unloading curve which shows force
against indentation, the Vickers hardness value (HV) of the coating was determined
to be 3000HV.

20 Example 4 – Testing Wear Resistance

A Tribo test was conducted using a Bruker TriboLab System to determine the wear
resistance of the coatings under repeated, high force oscillating movements. The Tribo
test is a reciprocal “pin-on-disk” sliding test and mimics oscillating wear that may occur

during use. The coating passed the test at 400N with 1500 cycles. The coating also passed the test with a 750g load and CS-17 tip with 10000 cycles.

Example 5 – Coating Method (2)

- 5 A coated substrate was produced using a coating apparatus having a Ti sputtering source, two FCVA sources, a CVD source and an ion beam source positioned around a central coating chamber as shown in Figure 1. The CVD source was a PACVD source.

The substrate was coated by carrying out the following steps in order:

- 10 1. A pre-cleaned steel substrate was mounted onto the coating fixture (also referred to as a substrate holder).
2. The coating fixture with mounted substrate was loaded into the coating chamber and this was pumped down to the vacuum required (see below for required pressure for each step). The heater temperature was set to 120°C and this was maintained throughout the coating process.
- 15 3. The substrate was etched using an ion beam source.
4. A Ti layer was applied by sputtering with a Ti target, until the desired thickness was achieved. The chamber pressure was around 2.0×10^{-3} Torr during sputtering. During the sputtering step, the substrate holder was biased at -300V with a 50% duty cycle.
- 20 5. A ta-C layer was applied by FCVA using a graphite source, until the desired thickness was achieved. The FCVA coating pressure was below 2.0×10^{-5} Torr during FCVA. During the FCVA step, the substrate holder was biased at -1200V with a 3.2% duty cycle.
- 25 6. A DLC layer was applied by PACVD with a C_2H_2 PACVD source, until the desired thickness was achieved. The PACVD pressure was around 2.0×10^{-3} Torr. During the PACVD step, the substrate holder was biased at -1200V with a 3.2% duty cycle. During the PACVD step, there was gas flow of C_2H_2 into the coating chamber at 100sccm.
- 30 7. The vacuum was relieved and the mounted coated substrate was removed from the coating chamber.
8. The coated substrate was removed from the coating fixture.

The coated substrate was determined to have a surface electrical resistance of 10^7 Ω/sq . The coating additionally had desirable film hardness, density and uniformity.

Claims

1. A substrate coated with a multi-layer coating, comprising in order:
 - i. a substrate,
 - ii. a conductive metal seed layer (e.g. titanium or chromium),
 - iii. a ta-C containing layer, and
 - iv. a DLC containing layer,wherein the coating has a surface electrical resistance of from $10^5 \Omega/\text{sq}$ to $10^9 \Omega/\text{sq}$.
2. A coated substrate according to claim 1, wherein the ta-C containing layer has a thickness of from $0.1 \mu\text{m}$ to $1.0 \mu\text{m}$.
3. A coated substrate according to claim 1 or claim 2, wherein the DLC containing layer has a thickness of from $1.5 \mu\text{m}$ to $3.5 \mu\text{m}$.
4. A coated substrate according to any preceding claim, wherein the ta-C containing layer consists of ta-C and/or the DLC containing layer consists of DLC.
5. A coated substrate according to any preceding claim, wherein the coating has a surface electrical resistance of from $10^6 \Omega$ to $10^7 \Omega$.
6. A coated substrate according to any preceding claim, wherein the ta-C containing layer and the DLC containing layer are adjacent.
7. A coated substrate according to any preceding claim, wherein the seed layer is adjacent the ta-C containing layer.
8. A coated substrate according to any preceding claim, wherein the DLC of the DLC containing layer has a hydrogen content of 20% or greater.
9. A coated substrate according to any preceding claim, wherein the ta-C has a hydrogen content of 5% or less and an sp^2 content of 20% or less.

10. A coated substrate according to any preceding claim, wherein the DLC has a hydrogen content of 20% or greater and an sp^2 content of 50% or greater.
11. A coated substrate according to any preceding claim, wherein the substrate is made of metal (e.g. copper, aluminium, steel), silicon or glass.
12. A coated substrate according to any preceding claim, wherein the DLC containing layer is deposited by a CVD method.
13. A coated substrate according to any preceding claim, wherein the ta-C containing layer is deposited by a PVD method, such as an CVA method (preferably FCVA).
14. A coated substrate according to any preceding claim, wherein the DLC containing layer is deposited by a PACVD process with the following deposition parameters:
 - i. a coating temperature of from 100°C to 200°C,
 - ii. a gas flow of from 50sccm to 200sccm, wherein the gas is selected from CH_4 , C_2H_6 or C_2H_2 ,
 - iii. a bias voltage of from -50V to -1200V, and
 - iv. a duty cycle of from 3.2% to 75%.
15. A coated substrate according to any preceding claim, wherein the DLC containing layer is deposited by a PACVD process with the following deposition parameters:
 - i. a coating temperature of from 110°C to 120°C,
 - ii. a gas flow of from 80sccm to 120sccm, wherein the gas is C_2H_2 ,
 - iii. a bias voltage of from -800V to -1200V, and
 - iv. a duty cycle of from 3.2% to 20%.
16. A substrate coated with a multi-layer coating according to any preceding claim, consisting of in order:
 - i. a substrate,
 - ii. a seed layer,

- iii. a ta-C containing layer, and
- iv. a DLC containing layer,

wherein the coating has a surface electrical resistance of from $10^5 \Omega/\text{sq}$ to $10^9 \Omega/\text{sq}$.

17. A coated substrate according to any preceding claim, comprising in order:

- i. a metal substrate,
- ii. a conductive metal seed layer (e.g. titanium or chromium),
- iii. a ta-C containing layer having a thickness of from $0.1 \mu\text{m}$ to $1.0 \mu\text{m}$, and
- iv. a DLC containing layer having a thickness of from $1.5 \mu\text{m}$ to $3.5 \mu\text{m}$.

18. A method of making a coated substrate according to any preceding claim, comprising providing the substrate, and coating onto the substrate, in order:

- i. a seed layer,
- ii. a ta-C containing layer, and
- iii. a DLC containing layer

wherein the coating has a surface electrical resistance of from $10^5 \Omega/\text{sq}$ to $10^9 \Omega/\text{sq}$.

19. A method according to claim 18, wherein the ta-C is deposited by FCVA.

20. A method according to claim 16 or 17, comprising providing a substrate, and coating onto the substrate, in order:

- i. a seed layer,
- ii. a ta-C containing layer deposited by FCVA, and
- iii. a DLC containing layer deposited by a PACVD process with the following deposition parameters:
 - a. a coating temperature of from 100°C to 200°C ,
 - b. a gas flow of from 50sccm to 200sccm, wherein the gas is selected from CH_4 , C_2H_6 or C_2H_2 ,
 - c. a bias voltage of from -50V to -1200V , and
 - d. a duty cycle of from 3.2% to 75%,

wherein the coating has a surface electrical resistance of from $10^5 \Omega/\text{sq}$ to $10^9 \Omega/\text{sq}$.