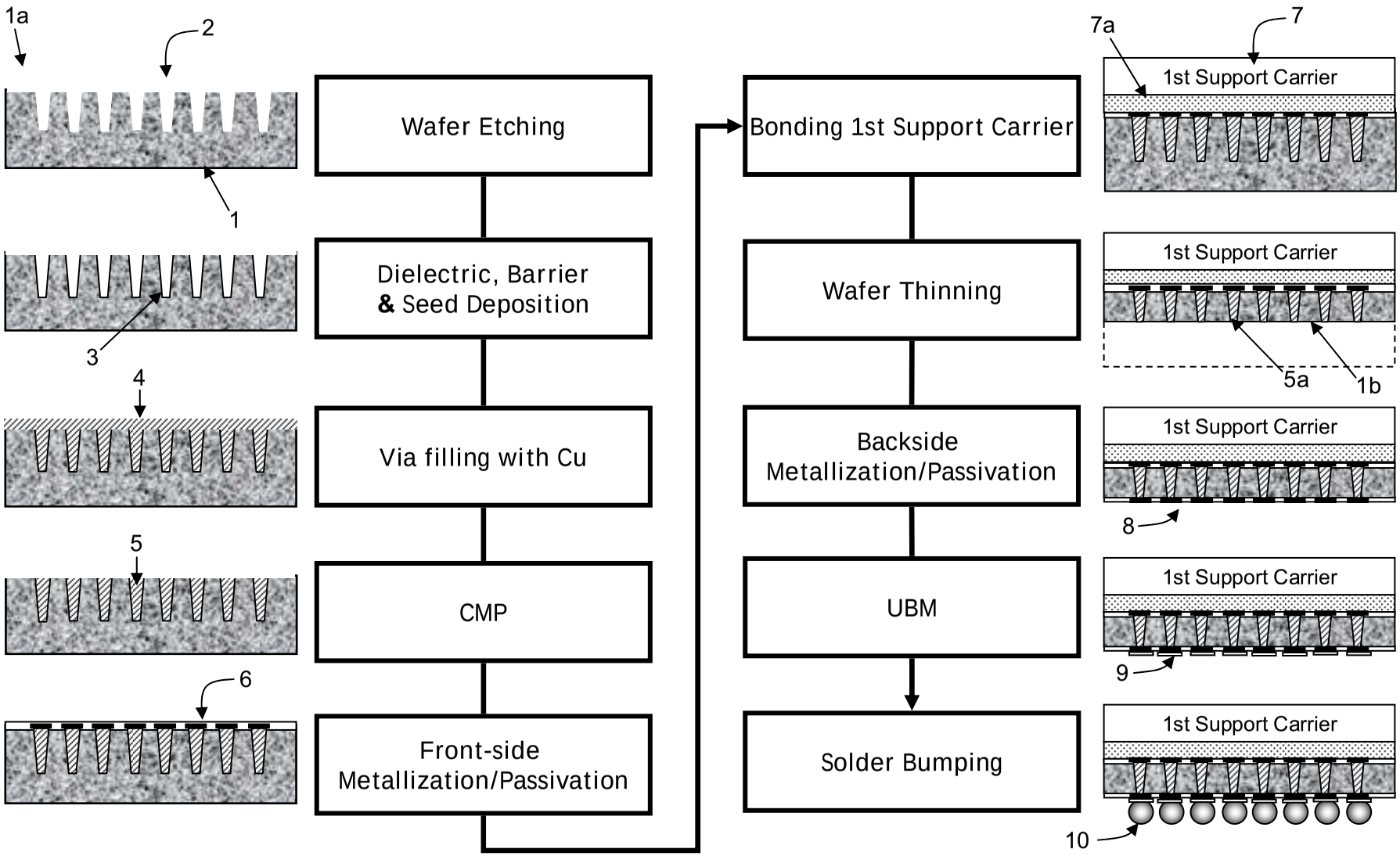


Figure 1(a)

Prior Art

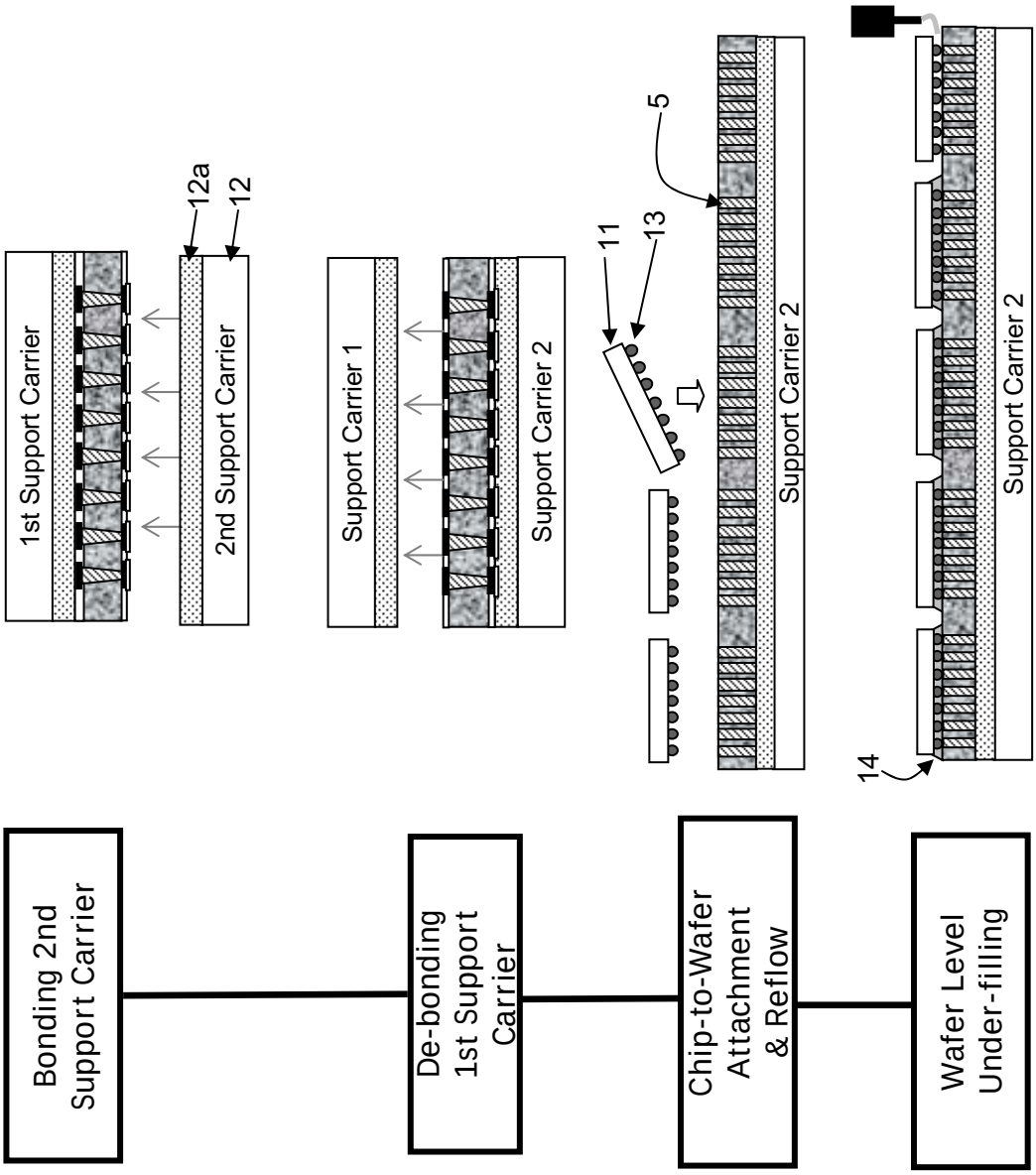


Figure 1(b)(i)
Prior Art

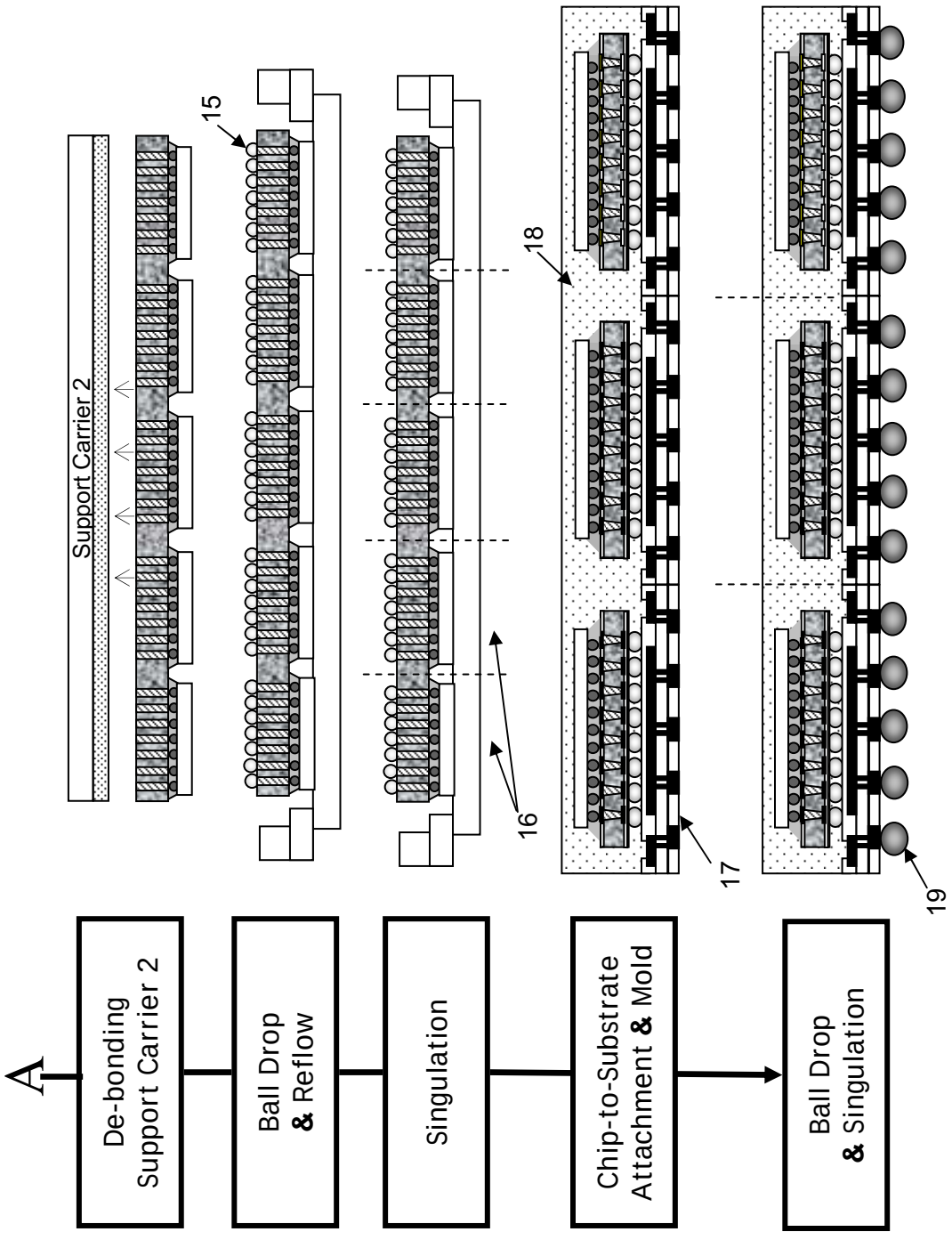


Figure 1(b)(ii)
Prior Art

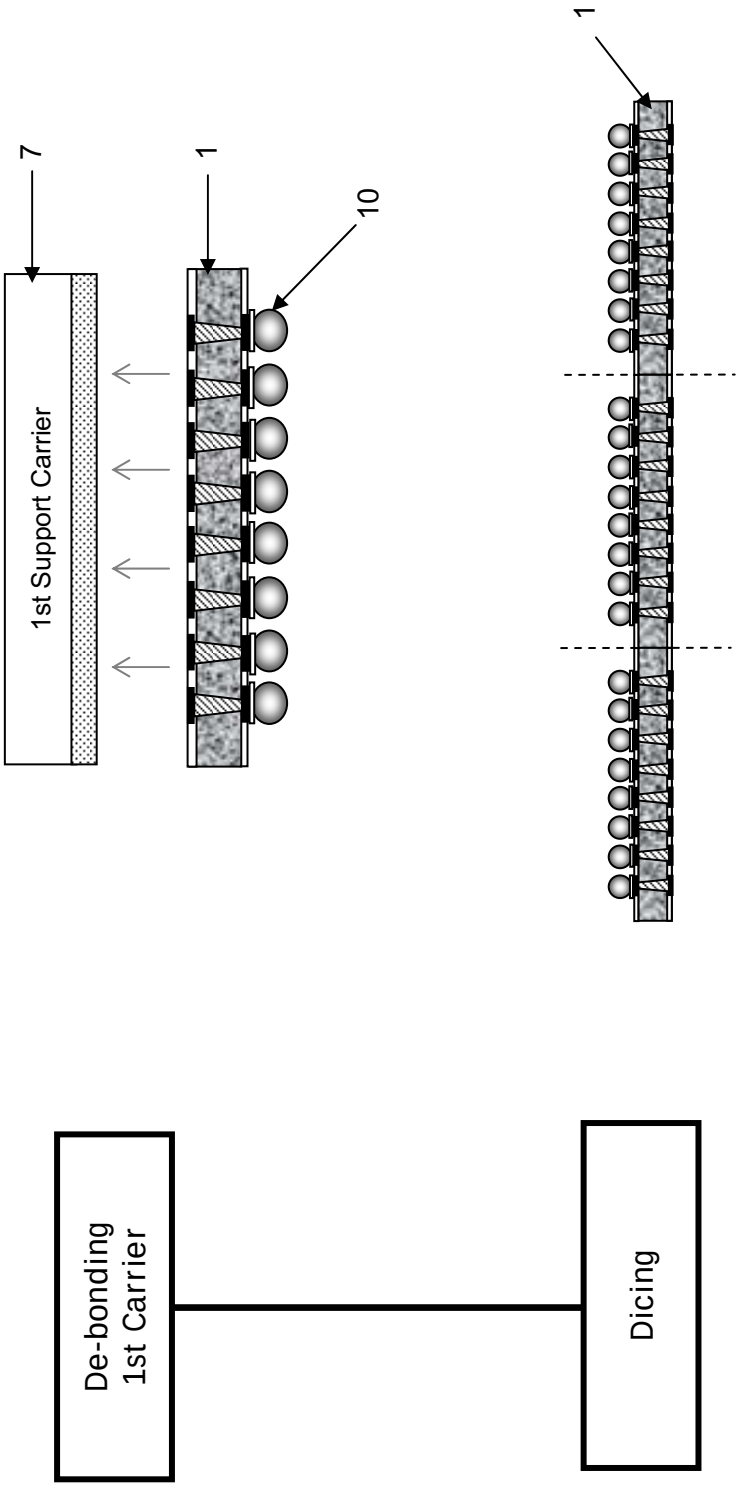


Figure 1(c)(i)
Prior Art

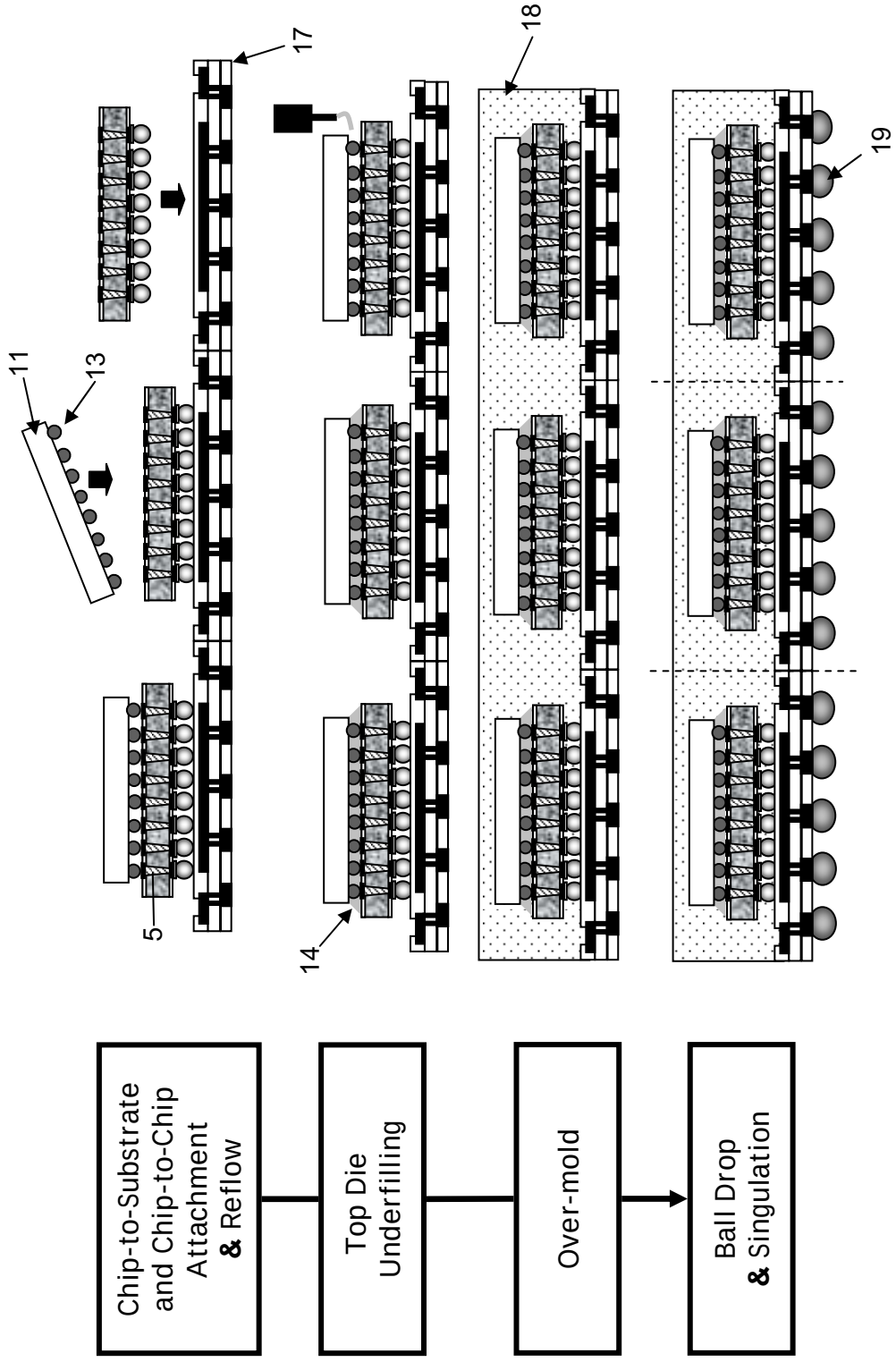


Figure 1(c) (ii)

Prior Art

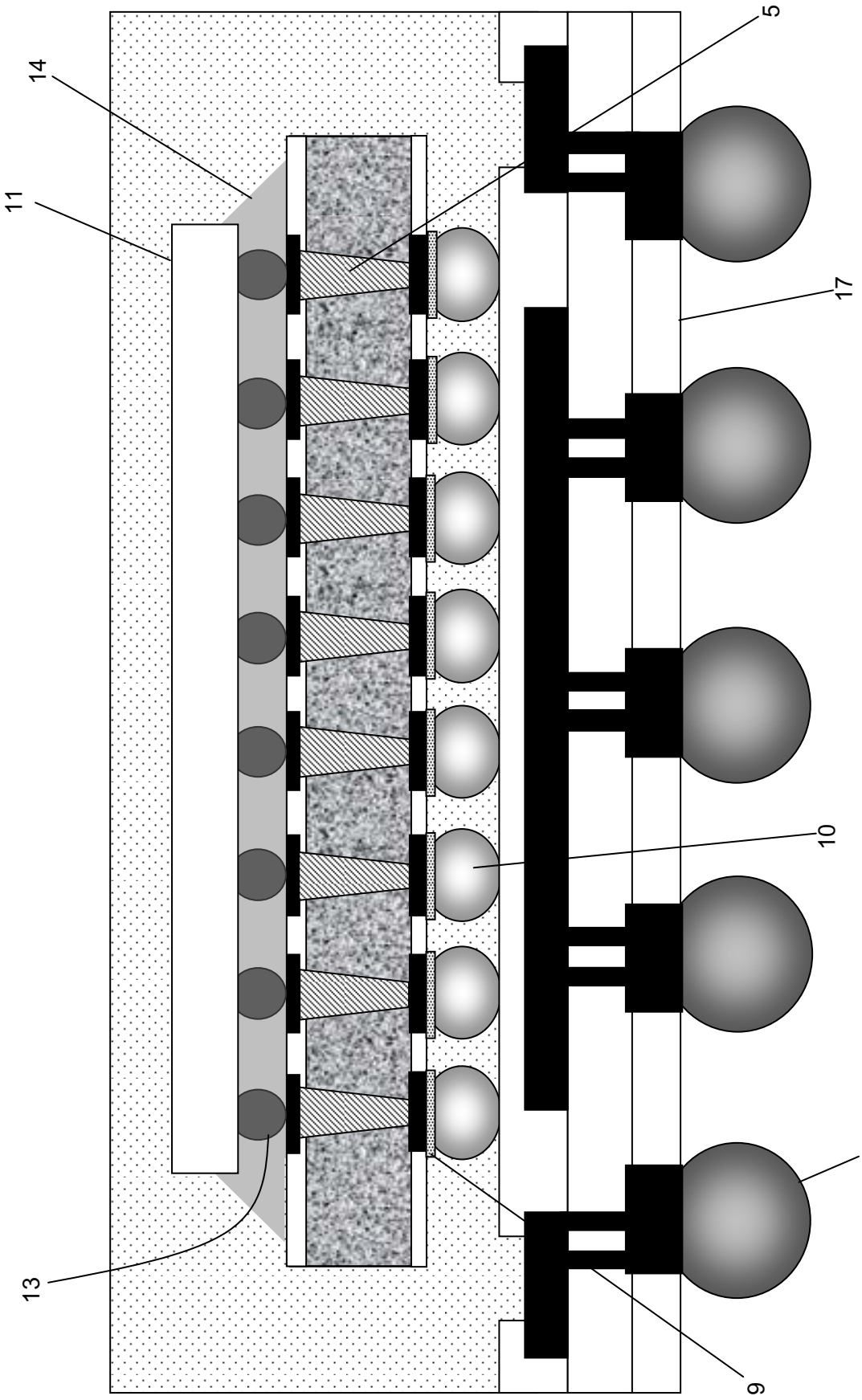
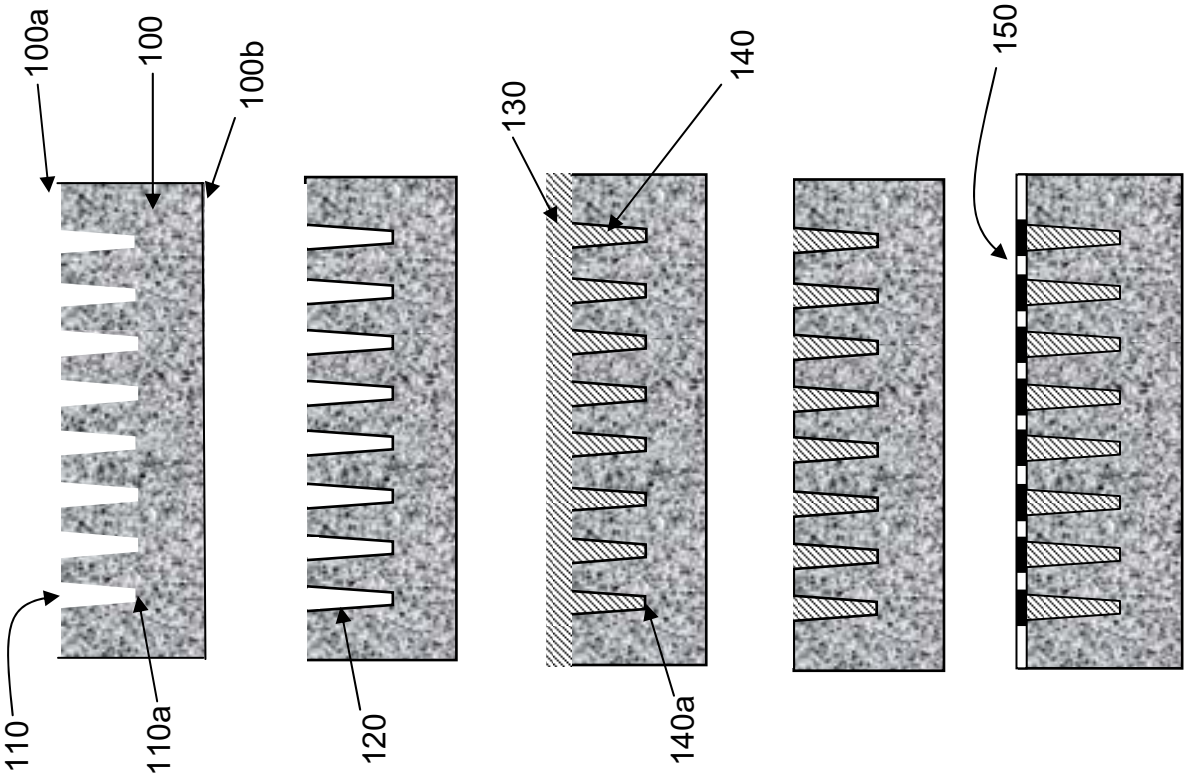


Figure 1(d)
Prior Art



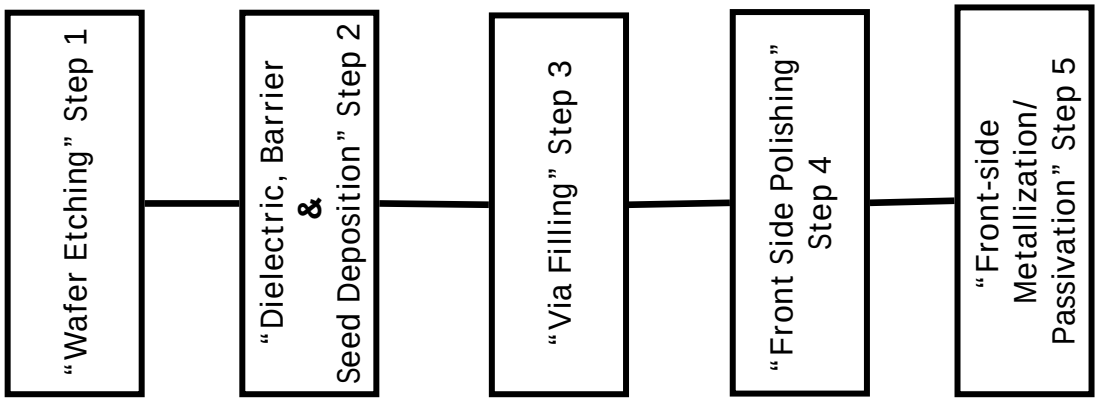
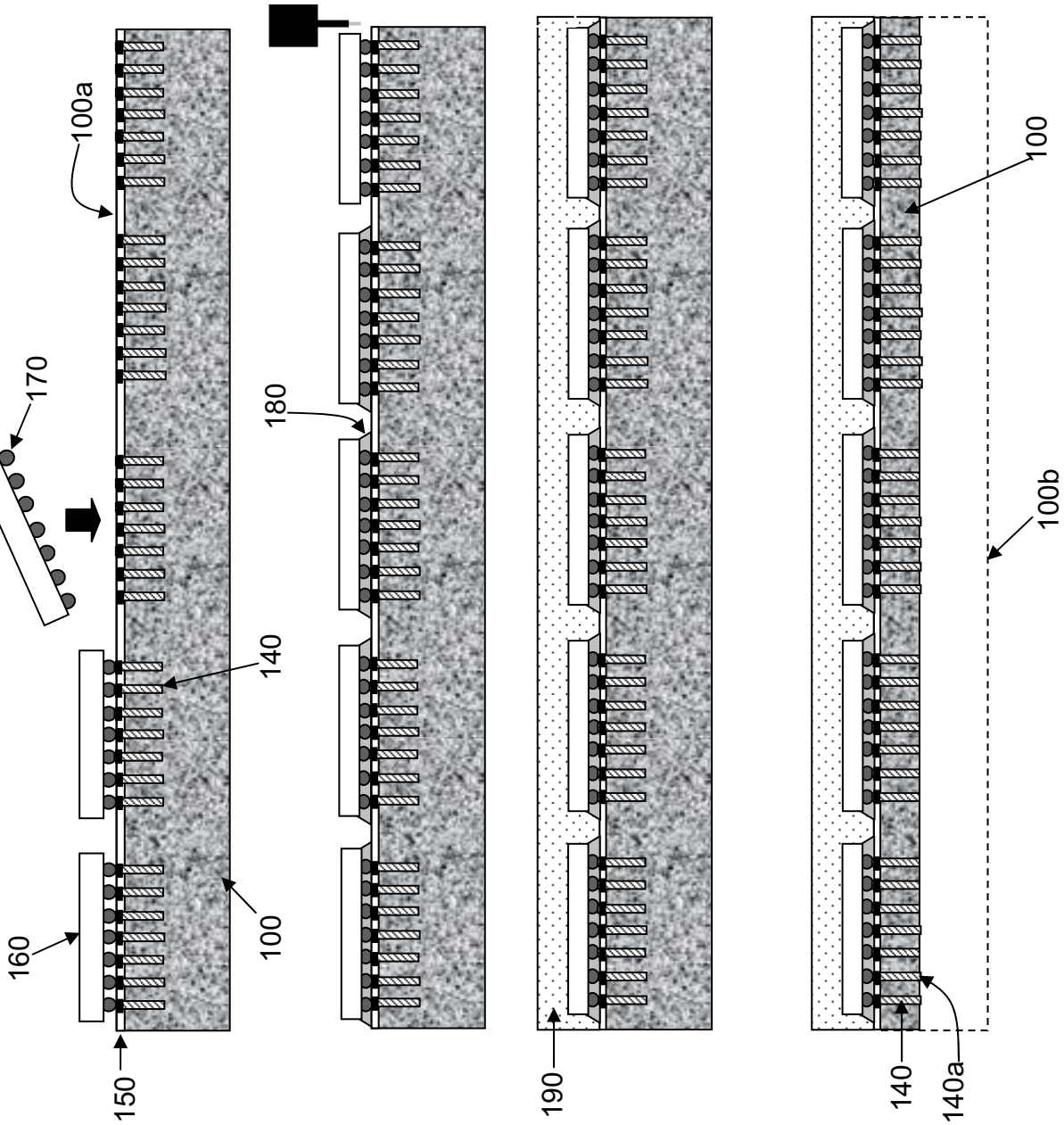


FIG. 2(a) FIG. 2(b) FIG. 2(c) FIG. 2(d) FIG. 2(e)



"Chip-to-Wafer Attachment" **Step 6**

FIG. 2(f)

"Under-filling" Step 7

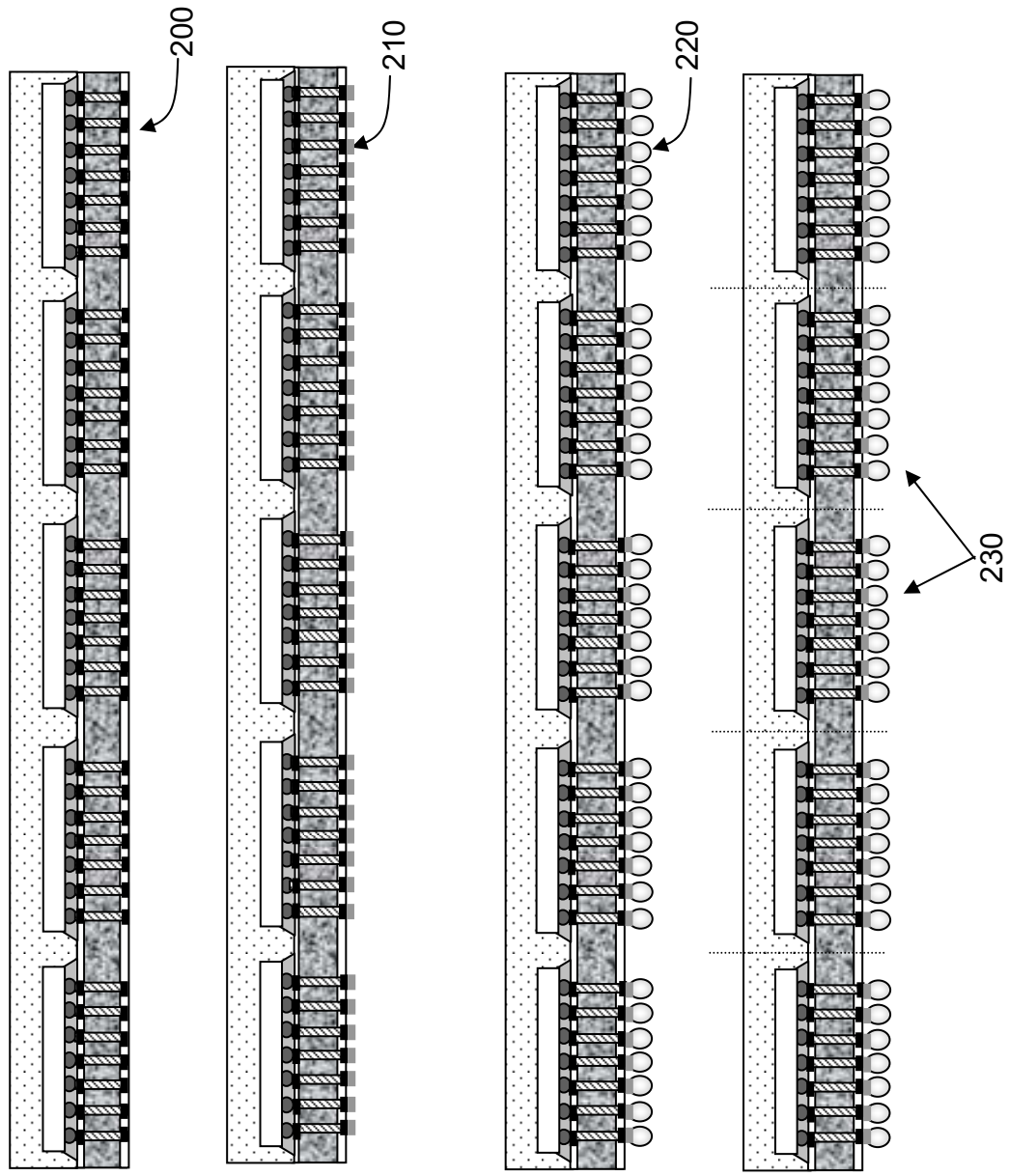
FIG. 2(g)

"Wafer Level Molding" Step 8

FIG. 2(h)

"Wafer Thinning" Step 9

FIG. 2(i)



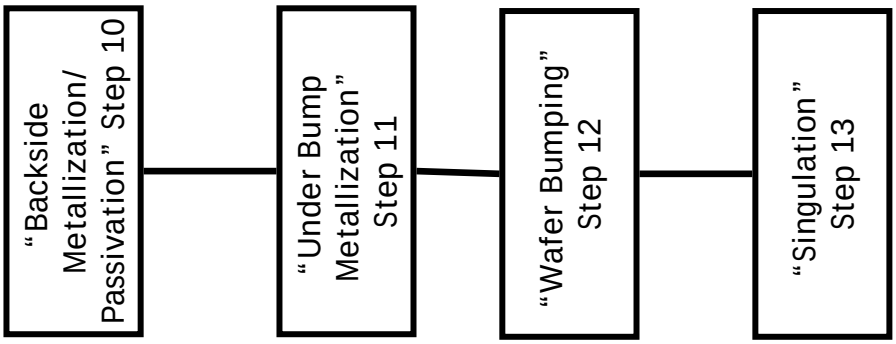
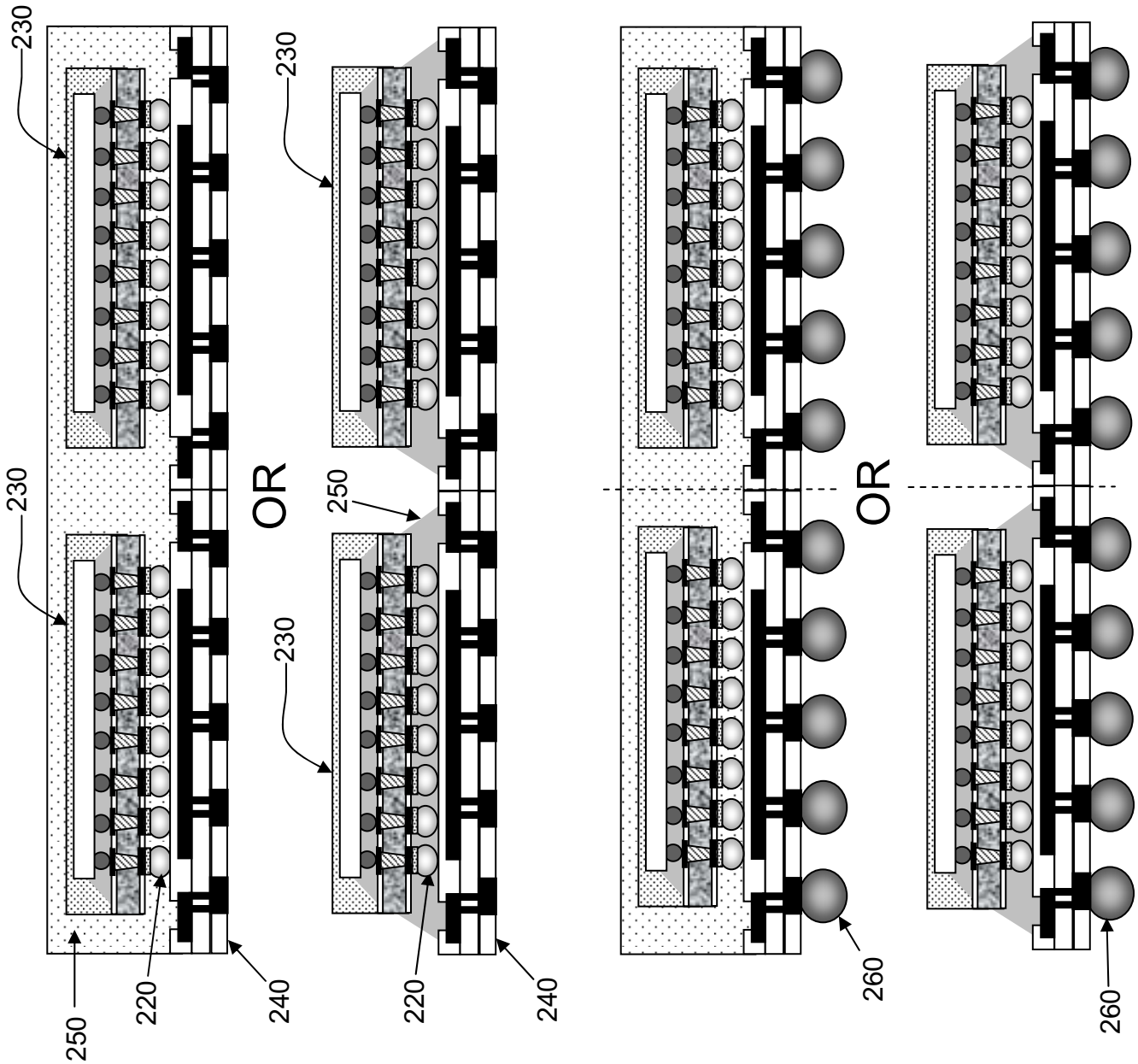


FIG. 2(j) FIG. 2(k) FIG. 2(l) FIG. 2(m)



"Chip-To-Substrate Attachment **&** Under-filling or Over-molding" Step 14

"Solder Ball Mounting & Singulation" Step 15

FIG. 2(n)(i)

FIG. 2(n)(ii)

FIG. 2(o)(i)

FIG. 2(o)(ii)

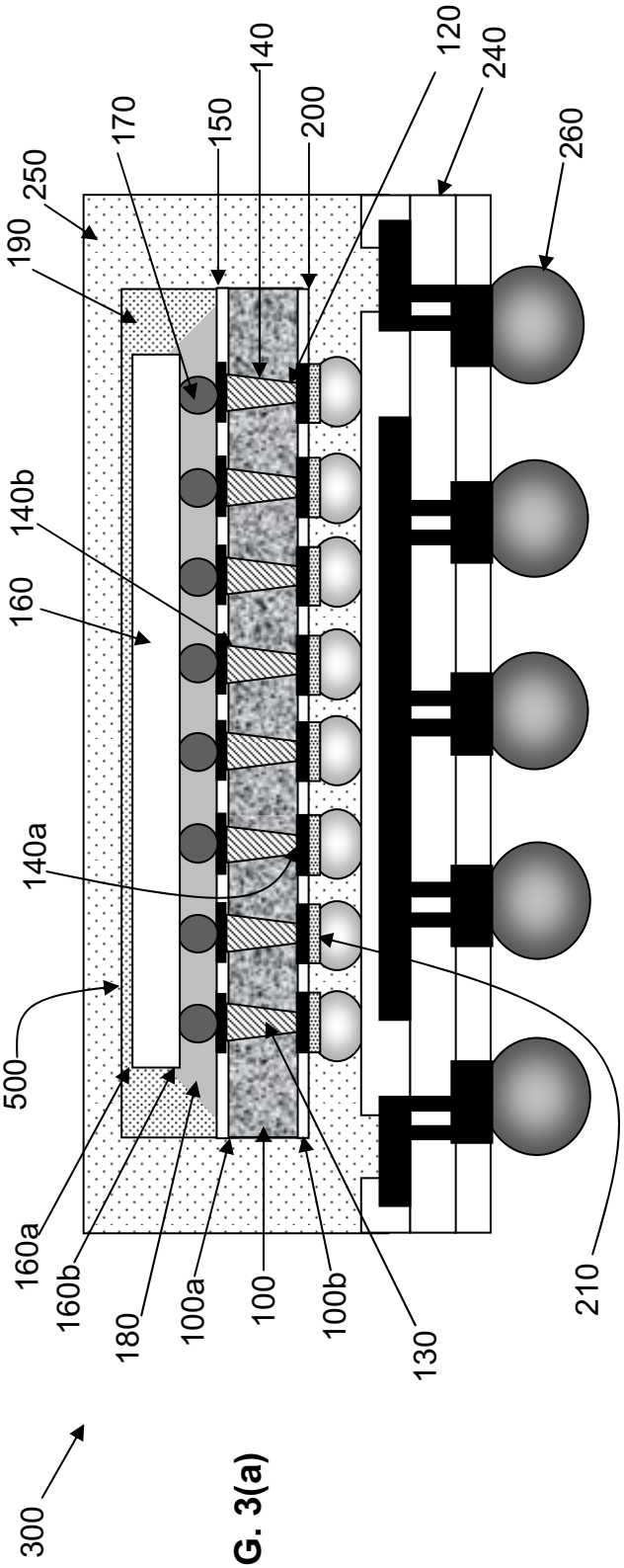

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FIG. 3(a)

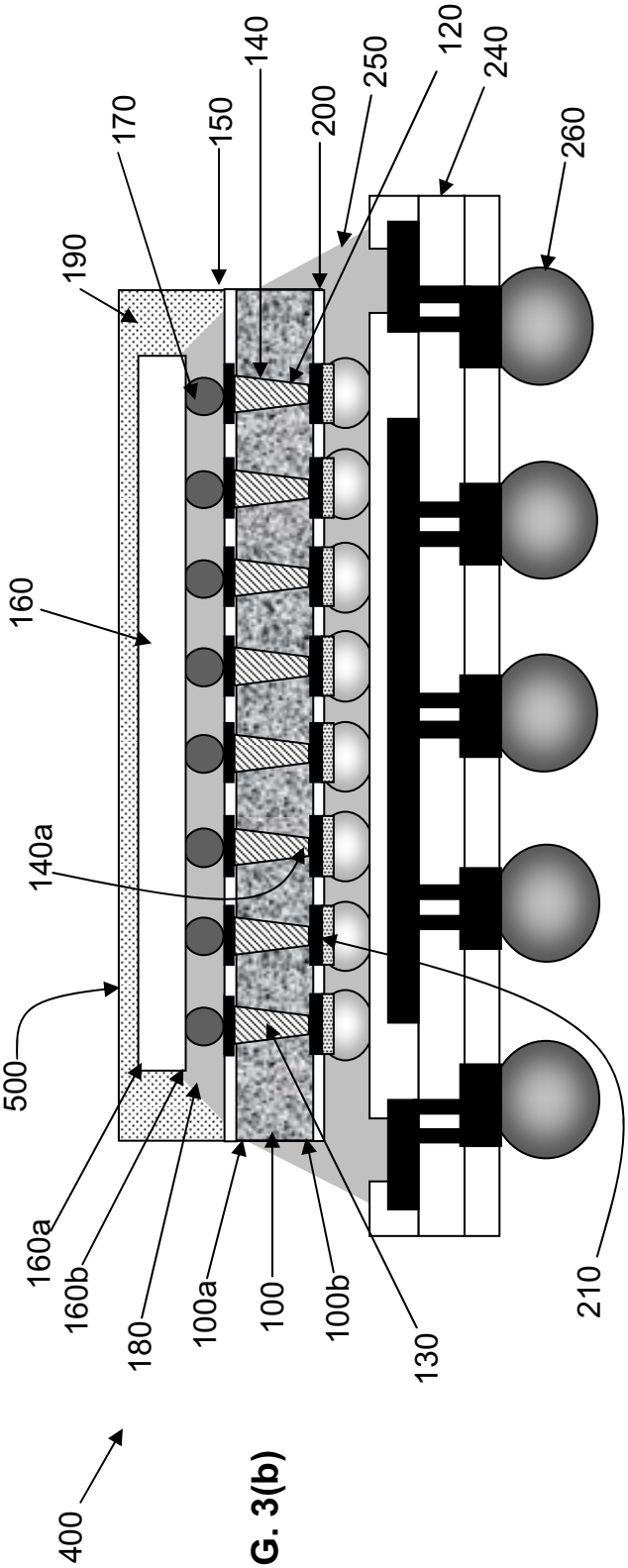
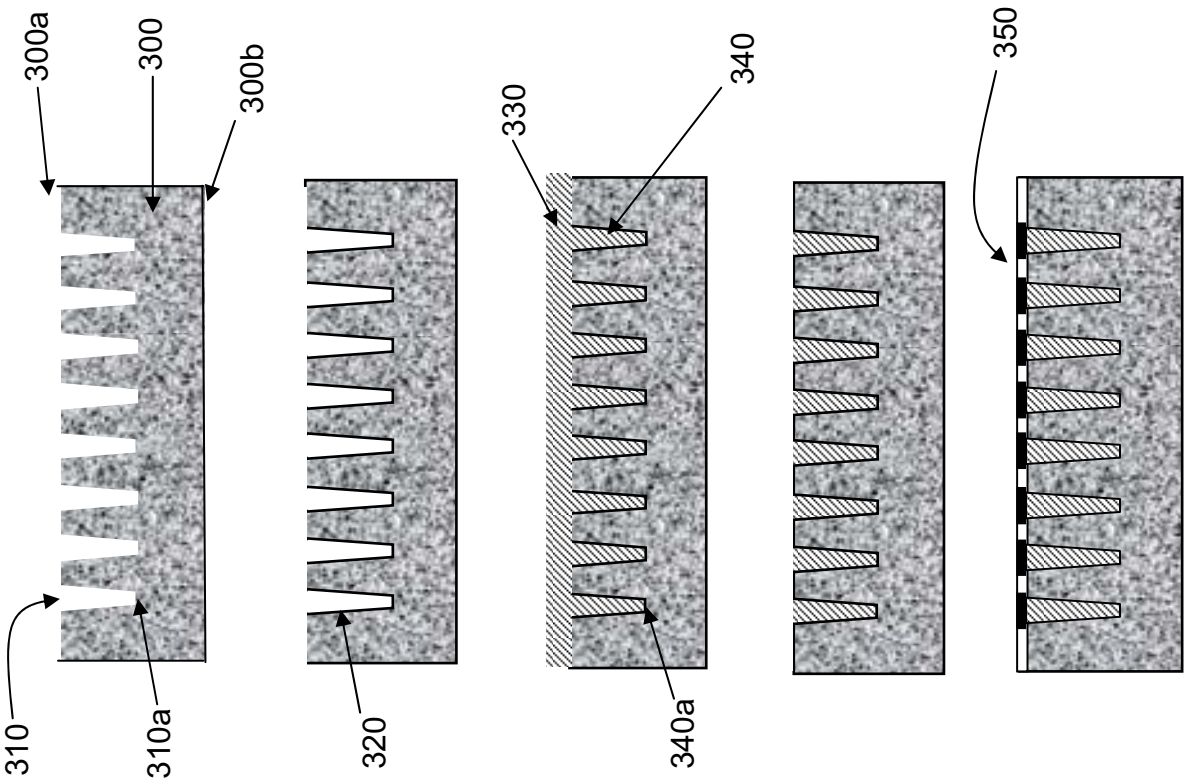

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FIG. 3(b)



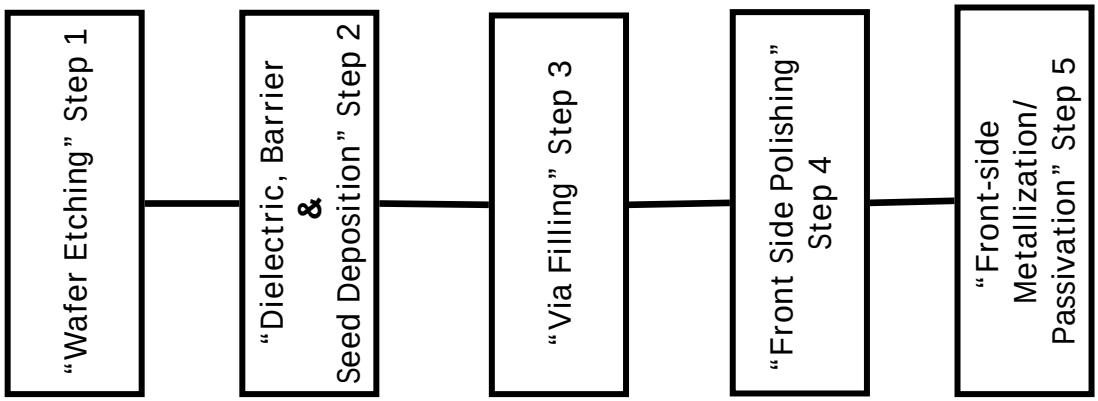


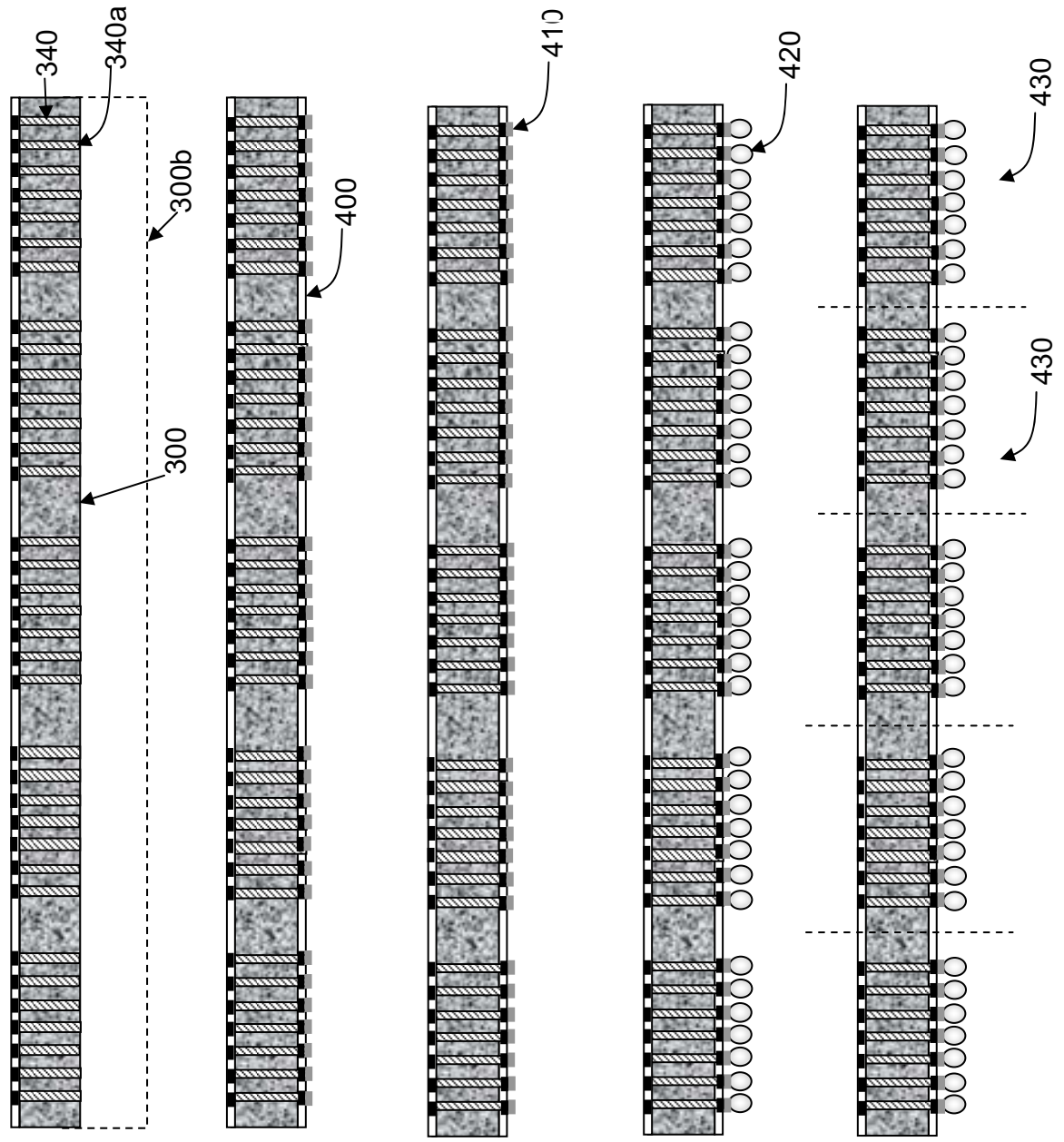
FIG. 4(a)

FIG. 4(b)

FIG. 4(c)

FIG. 4(d)

FIG. 4(e)



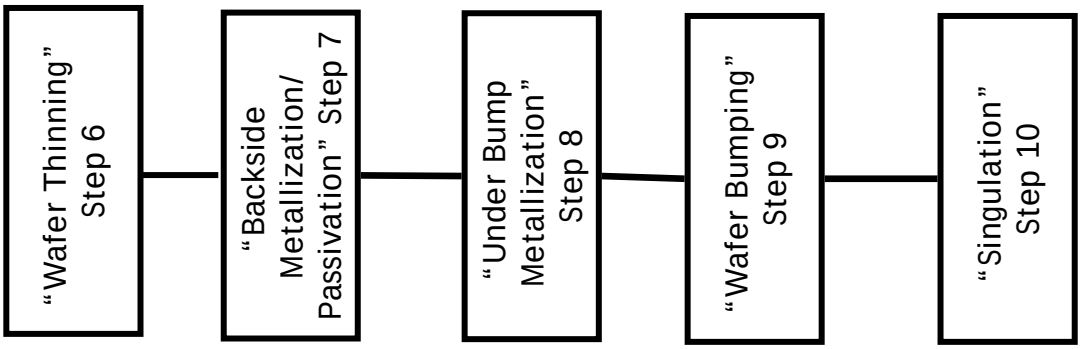
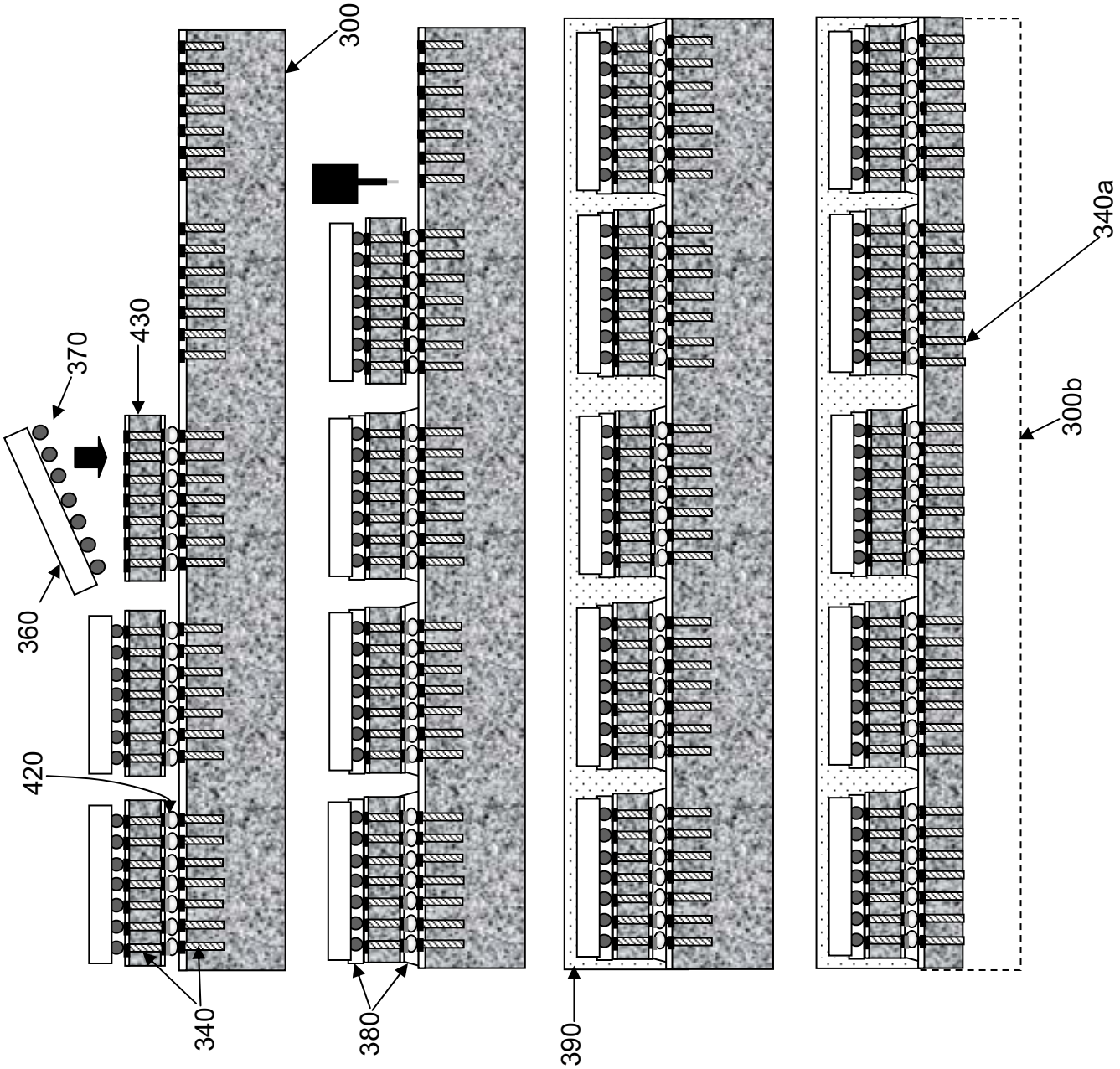


FIG. 4(f) FIG. 4(g) FIG. 4(h) FIG. 4(i) FIG. 4(j)



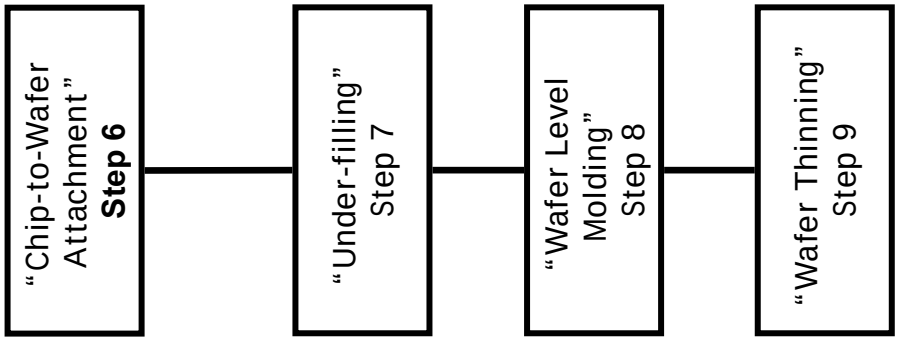
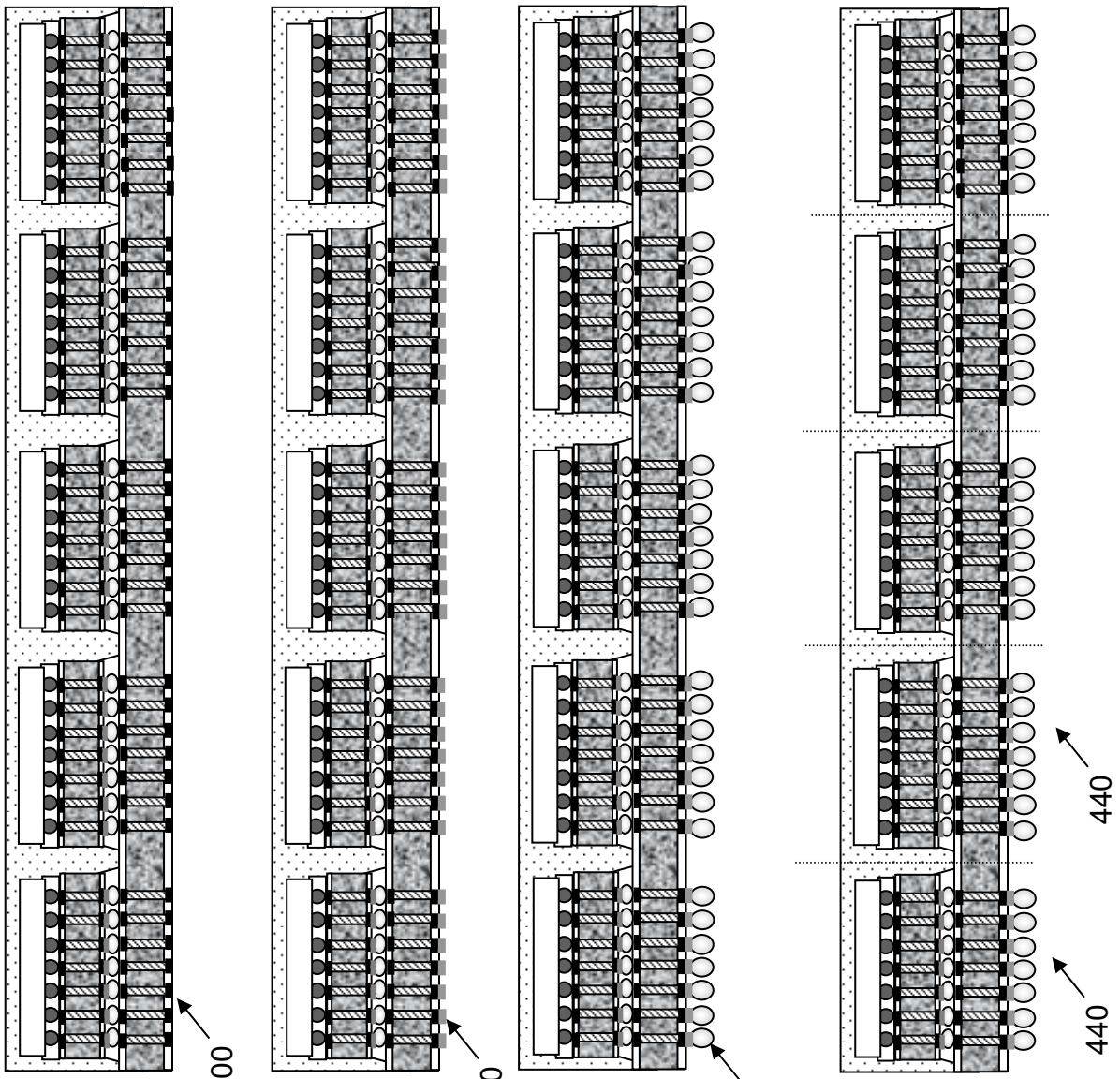


FIG. 5(a) FIG. 5(b) FIG. 5(c) FIG. 5(d)



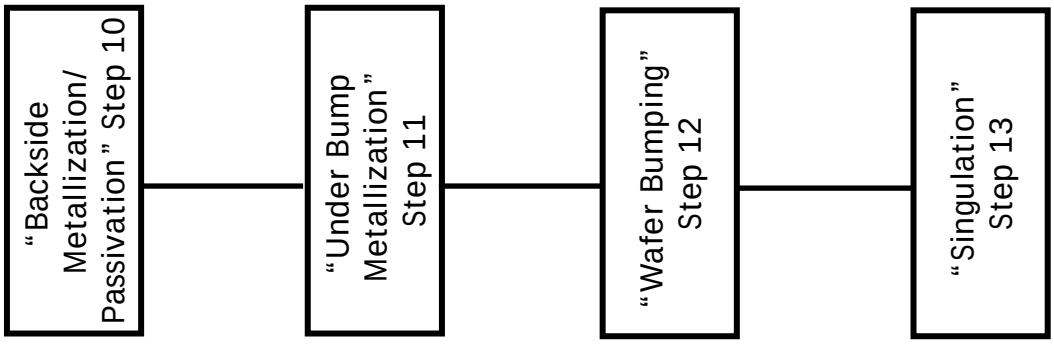
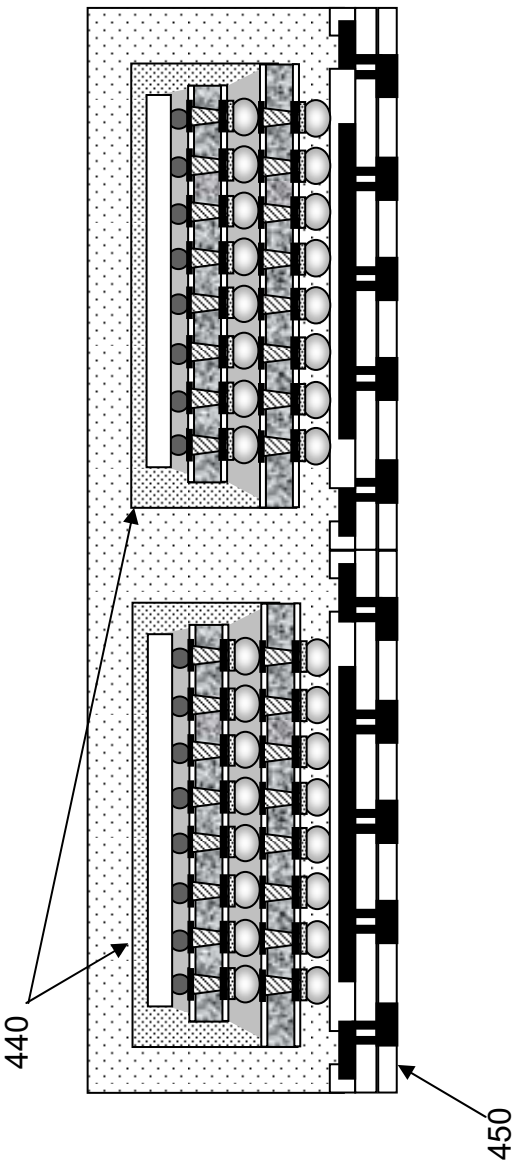
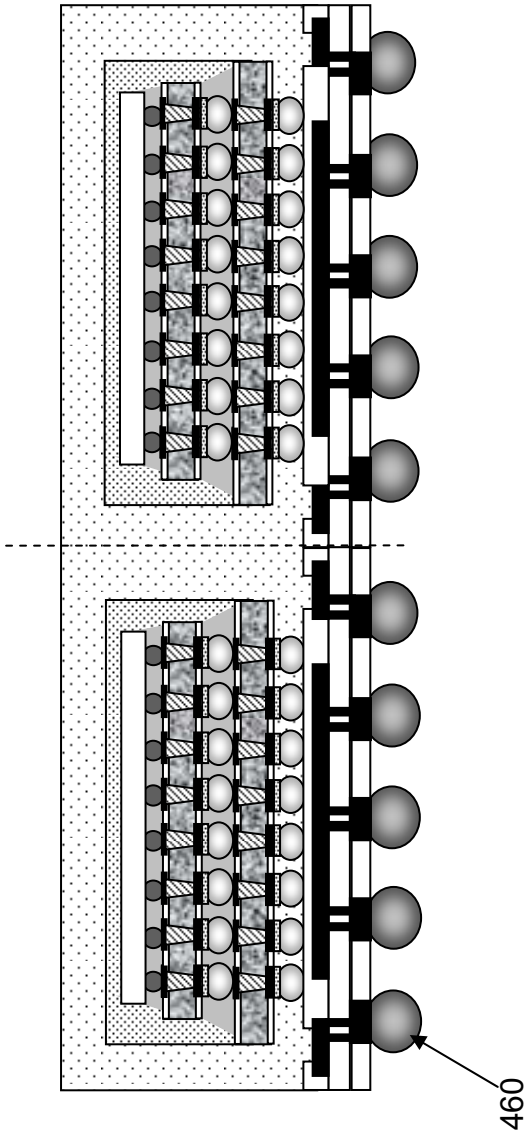


FIG. 5(e) FIG. 5(f) FIG. 5(g) FIG. 5(h)



"Chip-To-Substrate Attachment & Under-filling or Over-molding" Step 14

FIG. 5(i)



"Solder Ball Mounting & Singulation" Step 15

FIG. 5(j)

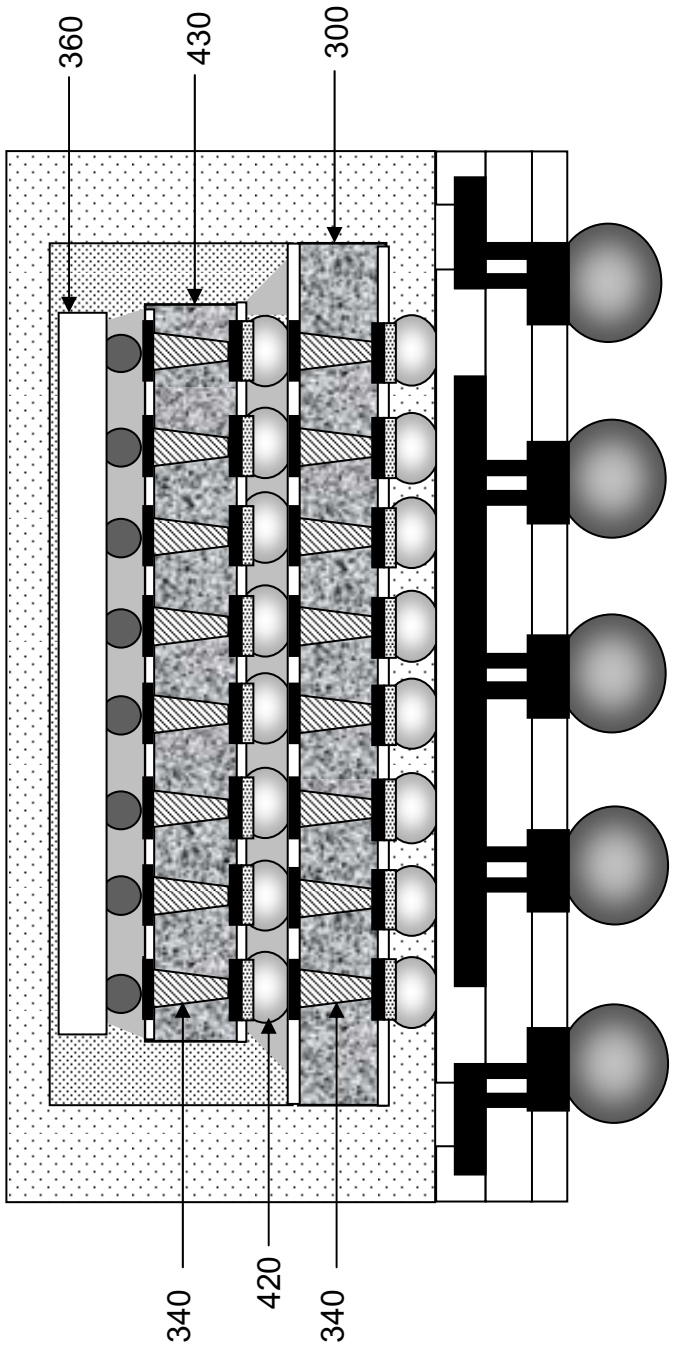


Figure 6