CLAIMS

1. A method, comprising:

forming a fin extending upward from a first source;

forming a material stack laterally adjacent to the fin, wherein the material stack includes, from bottom to top, a first spacer, a first sacrificial gate, a second spacer, a first placeholder, a third spacer, a second sacrificial gate, a fourth spacer, and a second placeholder;

removing the first and the second sacrificial gates to form trenches and to physically expose portions of sidewalls of the fin;

forming a first and second conductor layers inside the trenches;

removing the first placeholder and a portion of a drain to create an opening;

growing a faceted epitaxy within the opening on exposed surface of the drain, the faceted epitaxy includes two facets;

depositing a metal layer on top of the faceted epitaxy;

depositing an electrode on top of the metal layer; and

filling the opening between the electrode to create a contact layer.

2. The method of claim 1, wherein forming the fin comprises:

epitaxially growing following layers by an integrated epitaxy process:

the first source,

a first channel,

the drain,

a second channel, and

a second source;

depositing a hard mask on top of the second source; and

patterning the hard mask to form the fin.

3. The method of claim 2, wherein the first source, the second source, and the drain are doped with a dopant.

4. The method of claim 3, wherein the dopant is a p-type dopant.

5. The method of claim 3, wherein the dopant is an n-type dopant.

6. The method of claim 2, wherein the first source and the second source have a doping level of $4x10^{20}cm^{-3}$ to $1.5x10^{21}cm^{-3}$.

~~7. The method of claim 2, further comprising:~~

~~depositing a gate dielectric layer within the trenches, wherein the gate dielectric layer is in direct contact with sidewalls of the first and second channels.~~

~~8~~1. A method, comprising:

forming two vertical transport field effect transistors stacked one atop the other and separated by a resistive random access memory structure, wherein the two vertical transport field effect transistors comprise a source, a channel, and a drain, wherein a contact layer of the resistive random access memory structure functions as the drain of the two vertical transport field effect transistors.

~~9~~2. The method of claim ~~8~~1, wherein forming the two vertical transport field effect transistors further comprises:

forming a first source and a second source, wherein the first source is a bottom source and the second source is a top source; and

forming a gate conductor layer surrounding the channel.

~~10~~3. The method of claim ~~8~~1, wherein the resistive random access memory structure comprises:

faceted epitaxy defined by pointed tips, wherein the pointed tips of the faceted epitaxy extend vertically toward each other, wherein the faceted epitaxy is between the two vertical transport field effect transistors;

a metal layer in direct contact with each of the pointed tips of the faceted epitaxy; and

~~an~~ two electrode~~s~~, the two electrodes in direct contact with ~~each~~ the metal layer.

~~11~~4. A structure, comprising:

a first vertical field effect transistor, the first vertical field effect transistor comprises a first source, a first channel, and a drain, the channel separates the source from the drain;

a second vertical field effect transistor stacked above the first vertical field effect transistor, the second vertical field effect transistor comprises a second source, a second channel and the drain, the second channel separates the second source from the drain; and

a two resistive random access memory structure between the first vertical field effect transistor and the second vertical field effect transistor, the two resistive random access memory structure functioning as the drain of the first and the second vertical transport field effect transistors.

~~12~~5. The structure of claim ~~11~~4, wherein the two resistive random access memory structure~~s~~ comprise~~s~~:

<111> plane bound faceted epitaxy defined by two pointed shape tips, wherein the two pointed shape tips of the faceted epitaxy extend vertically toward each other;

a metal layer in direct contact with each of the two pointed shape tips of the faceted epitaxy; and

two electrodes in direct contact with the metal layer~~s~~.

~~13~~6. The structure of claim ~~12~~5, wherein the faceted epitaxy is doped with a dopant and has a doping level of $4x10^{20}cm^{-3}$ to $1.5x10^{21}cm^{-3}$.

~~14~~7. The structure of claim ~~13~~6, wherein the dopant is phosphorus or arsenic.

~~15~~8. The structure of claim ~~11~~4, further comprising:

a contact layer between the ~~electrodes of the~~ two resistive random access memory structure~~s~~, the contact layer connects the two resistive random access memory structures formed at the two pointed shape tips.

~~16~~9. The structure of claim ~~11~~4, wherein the first and the second vertical field effect transistors are n-type vertical field effect transistors.

~~17~~10. The structure of claim ~~11~~4, wherein the first and the second vertical field effect transistors are p-type vertical field effect transistors.

~~18~~11. The structure of claim ~~11~~4, wherein the first source and the second source have a doping level of $4x10^{20}cm^{-3}$ to $1.5x10^{21}cm^{-3}$.

12. A structure comprising:

a first vertical field effect transistor, the first vertical field effect transistor comprises a first source, a first channel, and a drain, the first channel separates the source from the drain;

a second vertical field effect transistor stacked above the first vertical field effect transistor, the second vertical field effect transistor comprises a second source, a second channel and the drain, the second channel separates the second source from the drain;

a two resistive random access memory structure between the first vertical field effect transistor and the second vertical field effect transistor, the two resistive random access memory structure functions as the drain of the first and the second vertical transport field effect transistors; and

a gate conductor layer surrounding the first and second channels, wherein the gate conductor layer is separated from the first and second channels by a gate dielectric layer.

13. The structure of claim 12, wherein the two resistive random access memory structures comprise:

<111> plane bound faceted epitaxy defined by two pointed shape tips, wherein the two pointed shape tips of the faceted epitaxy extend vertically toward each other;

a metal layer, the metal layer is in direct contact with the two pointed shape tips of the faceted epitaxy; and

two electrodes, the two electrodes are in direct contact with the metal layer.

14. The structure of claim 13, wherein the faceted epitaxy is doped with a dopant and has a doping level of $4x10^{20}cm^{-3}$ to $1.5x10^{21}cm^{-3}$.

15. The structure of claim 14, wherein the dopant is phosphorus or arsenic.

16. The structure of claim 12, further comprising:

a contact layer between the two resistive random access memory structures, the contact layer connects the two resistive random access memory structures formed at the two pointed shape tips.

17. The structure of claim 12, wherein the first and the second vertical field effect transistors are n-type vertical field effect transistors.

18. The structure of claim 12, wherein the first and the second vertical field effect transistors are p-type vertical field effect transistors.

19. The structure of claim 12, wherein the first source and the second source have a doping level of $4x10^{20}cm^{-3}$ to $1.5x10^{21}cm^{-3}$.

20. The structure of claim 12, wherein the first source is doped with phosphorus or boron and the second source is doped with phosphorus.