



- (51) **International Patent Classification:**
G06F 30/398 (2020.01) *G06F 30/00* (2020.01)
- (21) **International Application Number:**
PCT/IB2021/061753
- (22) **International Filing Date:**
15 December 2021 (15.12.2021)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
17/124,429 16 December 2020 (16.12.2020) US
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- (81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

- (84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH,

- (54) **Title:** PATH-BASED TIMING DRIVEN PLACEMENT USING ITERATIVE PSEUDO NETLIST CHANGES

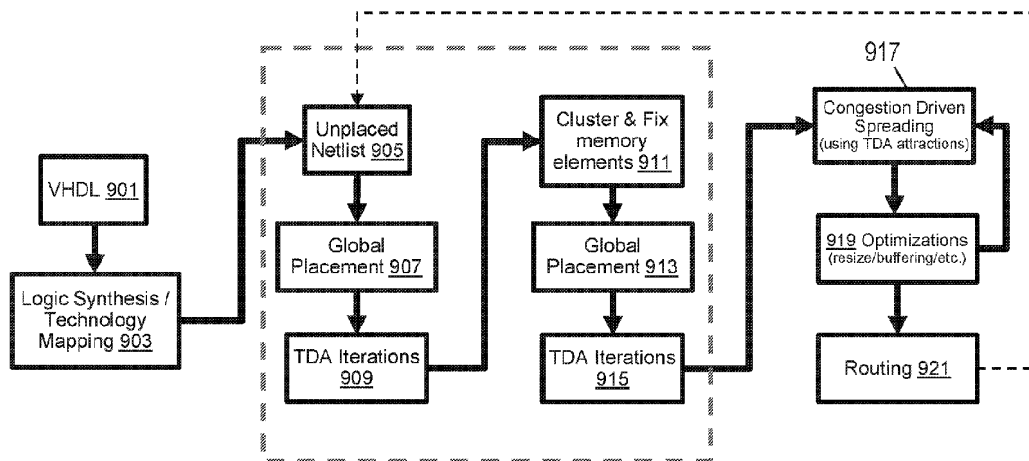


FIG. 8

- (57) **Abstract:** Carry out an initial wire-length-driven placement for an integrated circuit design embodied in an unplaced netlist, using a computerized placer, to obtain a data structure representing initial placements of logic gates. Identify at least one timing-critical source-sink path between at least one pair of source-sink endpoints in the data structure representing the initial placements. Create a new pseudo two-pin net for each pair of the at least one pair of source-sink endpoints to create an updated netlist. Carry out a revised wire-length-driven placement on the updated netlist to obtain a data structure representing revised placements.

GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))