

SPECIFICATION

Broadcast receiver including a search tuning circuit

The invention relates to a broadcast receiver including a search tuning circuit constructed to tune the receiver in succession to a plurality of nominal frequencies corresponding to respective members of a group of tuning data stored in a storage circuit and hence to cause the receiver to respond in succession to a plurality of reception frequency ranges, the receiver including a reception condition signal generator constructed to produce an output signal which is indicative of the field strength of any received transmission the frequency of which falls within the frequency range to which the receiver instantaneously responds, and a coupling from the output of said generator to a control input of said search tuning circuit in such manner that the output signal of said generator will deactivate the search action of said search tuning circuit when said output signal indicates that said field strength has at least a predetermined value.

Patent Specification 1,507, 684 describes a receiver of the above-mentioned type. A search action carried out in this receiver may sometimes stop when a transmission is received the frequency of which lies with the frequency range to which the receiver instantaneously responds but which does not correspond to the nominal frequency to which the search tuning circuit has tuned the receiver. Such a possibility could be prevented by deriving the reception condition signal generator output signal from a selective network which produces a voltage only when the received transmission lies within a very limited frequency range. However, this is liable to result in a slow search action.

It is an object of the invention to provide an alternative way of reducing the likelihood of the aforesaid possibility occurring while enabling the search action to remain rapid.

The invention provides a broadcast receiver including a search tuning circuit constructed to tune the receiver in succession to a plurality of nominal frequencies corresponding to respective members of a group of tuning data stored in a storage circuit and hence to cause the receiver to respond in succession to a plurality of reception frequency ranges, the receiver including a reception condition signal generator constructed to produce an output signal which is indicative of the field strength of any received transmission the frequency of which falls within the frequency range to which the receiver instantaneously responds, and a coupling from the output of said generator to a control input of said search tuning circuit in such manner that the output signal of said generator will deactivate the search action of said search tuning circuit when said output signal indicates that said field strength has at least a predetermined value, characterised in that the receiver also includes a frequency detector circuit constructed to generate an output signal

indicative of whether or not any difference between the frequency of any received transmission which falls within the frequency range to which the receiver instantaneously responds and the nominal frequency to which the receiver is instantaneously tuned is greater than a predetermined amount, and a coupling from the output of said frequency detector circuit to a control input of said search tuning circuit in such manner that the output signal of said frequency detector circuit will reactivate the search action of said search tuning circuit if said difference is greater than said predetermined amount.

The bandwidth of a frequency detector can be made sufficiently wide to enable it to produce an output signal very quickly, enabling a sufficiently accurate criterion to be rapidly obtained as regards the agreement or otherwise of the frequency of the received transmission with the nominal frequency to which the receiver is tuned.

An embodiment of the invention will now be described, by way of example, with reference to the accompanying drawing, the sole Figure of which shows a block diagram of the embodiment.

Details of the receiver which are irrelevant in the present context have been omitted from the Figure.

In the broadcast receiver shown in the drawing an aerial signal is applied to an input 1 of a high-frequency and mixing section 3 of the receiver and a signal originating from an oscillator 7 is applied to an input 5 thereof. An intermediate frequency signal is obtained from an output 9 of the high-frequency and mixing section 3 and applied to an intermediate frequency amplifier 11.

The oscillator 7 forms part of a frequency synthesizing circuit which is tuned by applying, to a multiple input 13 of a frequency divider 15, a tuning datum in the form of a digital code which determines the number by which the divider divides the frequency of a signal originating from the oscillator 7, which is applied to an input 17 of the divider. A signal, the frequency of which is determined by the oscillator frequency and the number by which the divider 15 divides, is obtained from an output 19 of the frequency divider 15. In a phase detector 21 this signal is compared with a reference signal coming from a reference oscillator 23 and its frequency and its phase is made equal thereto by means of a control signal obtained from a control signal output 25 of the phase detector 21 and applied to a control signal input 27 of the oscillator 7. The receiver thus becomes tuned to a frequency determined by the tuning datum.

The tuning datum applied to the multiple input 13 of the frequency divider 15 originates from a multiple output 29 or a multiple output 31 of a storage circuit 33, which outputs can be connected to the input 13 of the frequency divider 15 via gate circuits 35 and 37, respectively.

The storage circuit 33 comprises two circulating stores 39, 41, each storing a group of multi-bit tuning data. Each time a clock pulse is applied to an input 42 each store 39 and 41 offers

the next tuning datum of the corresponding group to its respective output 29 or 31. The tuning data in each given group have, for example, been chosen so that they all result in the receiver becoming tuned to transmitters which have the same character, such as, for example, transmitters broadcasting the same programme.

The gate circuits 35, 37 therefore enable a selection to be made as to from which circulating store and, consequently, from which group the tuning data are applied to the frequency divider 15. This selection is effected by means of a switching signal obtained from a switch 43 or a switch 45 included in a control device 47 when the relevant switch is closed. When one of these switches is closed an OR-gate 48 applies a signal to an AND-gate 49, so that clock pulses obtained from a clock signal generator 51 are applied to the input 42 of the storage circuit 33 via this AND-gate 49, when a reception condition signal corresponding to logic one is applied to a third input of the AND-gate 49. This signal is obtained from an OR-gate 53.

Closure of one of the switches 43 and 45 initiates a search action, which causes the tuning data of an aforesaid group to tune the receiver successively to frequencies corresponding to those tuning data. The search action stops when the reception condition signal coming from the OR-gate 53 becomes logic zero.

The reception condition signal is produced at the output of the OR-gate 53 in the following manner. On receipt of a signal from a transmitter the intermediate frequency section 11 supplies an intermediate frequency signal to an amplitude detector 54 and to a frequency detector 55. The amplitude detector 54 has an output 57 which supplies a rectified, intermediate frequency signal to an input 59 of a limiter 61. The limiter 61 converts the output signal of the amplitude detector 54 into a logic signal which appears at an output 63 of the limiter 61 and is applied to an inverting input of the OR-gate 53 and to an input of an AND-gate 65. This logic signal will be denoted a hereinafter and has the value logic one if the received signal has a satisfactory field strength and results in an input signal to intermediate amplifier 11 which is located within the bandwidth of the intermediate frequency amplifier 11. If the receiver is an FM receiver this bandwidth will be large and the signal a will very rapidly become logic one if such a signal is tuned in.

The signal at the output 57 of the amplitude detector 54 is also applied to an input 71 of a limiter 73 via a delay circuit formed by a resistor 67 and a capacitor 69. The limiter 73 produces a logic signal denoted b hereinafter at an output 75 and applies it to an input of an AND-gate 77. This signal b is somewhat delayed relative to the signal a .

The frequency detector 55 has two outputs 81, 83 at which signals appear from which unwanted alternating current components have been removed. These signals have mutually opposite

polarities with respect to a reference level and have the well-known S-shape as a function of the input frequency.

These signals are applied via two diodes 85, 87 to an input 89 of a limiter 91 which produces at an output 93, a logic signal denoted c which is "1" when the input signal to intermediate frequency amplifier 11 is outside the pass region of the intermediate frequency amplifier 11 and also when this signal lies within a very small frequency range around the intermediate frequency (to which detector 55 is tuned). The signal c is applied to a further input of the AND-gate 65 and to an inverting further input of the AND-gate 77. AND-gate 77 produces a logic signal bc' which is applied to a further input of the OR-gate 53.

The OR-gate 53 produces the reception condition signal having the logic formula $a' + bc'$. If no transmitted signal is received, the signals a and b are logic zero and c is logic one; the reception condition signal $a' + bc'$ is then logic one and the AND-gate 49 passes a clock signal when one of the switches 43, 45 is closed. The receiver then performs a search action. On receipt of a transmission which results in an intermediate frequency signal, a becomes logic one and b remains logic zero for a short time thereafter. The reception condition signal $a' + bc'$ becomes logic zero and the search action stops. The time constant of the network comprising the resistor 67 and the capacitor 69 is such that b becomes logic one when the control loop of the frequency synthesizer circuit has reached the rest condition and the receiver is, consequently, properly tuned to a frequency corresponding to a tuning datum from the selected group. When this occurs the reception condition signal $a' + bc'$ remains logic zero (because of the signal c) provided that the transmission gives rise to the proper intermediate frequency and the search action is the stopped permanently. If on the other hand the received transmission gives rise to an intermediate frequency which deviates somewhat from the proper intermediate frequency, the signal c becomes logic zero and the reception condition signal $a' + bc'$ becomes logic one and the search action is immediately started again.

The search action is therefore only stopped permanently on receipt of a transmission having a satisfactory field strength and the proper frequency. If a transmission is received which has a satisfactory field strength but a frequency which deviates from the correct one, the search action is only stopped temporarily during the very brief period of time required for tuning the receiver to the frequency determined by the tuning datum.

Assuming that the receiver is an FM receiver, the frequency detector 55 is provided with a further output 93 and produces thereat a low frequency or audio signal which is applied to a low frequency reproduction section 97 of the receiver via a switch 95. The switch 95 is operated by the output signal ac of the AND-gate 65 and is therefore closed only when the received

transmission has the proper frequency.

It will be apparent that the receiver can, if so desired, also be arranged to be tunable by tuning data other than those stored in the storage circuit 33. This facility is illustrated in the figure by means of dotted lines.

Although a frequency synthesizing circuit including an adjustable divider is shown in the receiver of the embodiment it is obvious that a different type of frequency synthesizing circuit can alternatively be used. In general, any search tuning circuit which does not require automatic frequency control by means of an output signal from the intermediate frequency section may be used.

Several functions which are performed simultaneously in the receiver of the above-described example can of course alternatively be performed sequentially, for example when the receiver is provided with a micro-processor.

Although the search tuning circuit described is particularly suitable for FM radio broadcast receivers, and for vehicle receivers in particular, the field of application is not limited thereto.

It will furthermore be obvious that it is possible to employ other combinations of gates, detection circuits and limiters to perform the functions described. The reception condition signal or the composite portions thereof can, for example, alternatively be applied together with the other signals to the AND-gate 49 and the OR-gate 48 or be combined in other ways.

Any wide-band detector capable of accurately determining whether its input signal has a predetermined frequency can be used as the frequency detector 55.

If desired, the storage circuit of the receiver may of course store only one group of tuning data.

40 CLAIMS

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2. A broadcast receiver including a search tuning circuit, substantially as described herein with references to the drawing.

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