Hybrid fully SOI-type multilayer structure

The invention concerns a SOI-type multilayer structure.

A SOI-type multilayer structure is a structure comprising a support layer, at least one working layer and an electrically insulating layer between the working layer(s) and the support layer.

More specifically, the invention concerns a SOI-type multilayer structure comprising at least two working layers having different crystalline orientations.

The invention also concerns a process for manufacturing this structure.

An advantageous application of such structure is the design and manufacturing of high performance CMOS circuits.

As an example, such a high performance may consist in boosting the speed of the NMOS and the PMOS transistor devices for a given power consumption.

This indeed allows building very complex circuits, such as million gate logic ones, whose performance in term of speed are very high without consuming too much power.

These kinds of circuits are usually known as LVLP circuits (Low Voltage Low Power).

Several approaches have been proposed in order to make such circuits.

A first approach consists in downscaling the channel size of the transistor devices.

This approach has been widely used for many years and has demonstrated its effectiveness.

Until now, the channel length of the transistor devices has been scalable on a path following Moore's law.

However said length becoming increasingly small, it now becomes increasingly difficult to keep the pace of this law.

Indeed, today the industry encounters many difficulties notably because it is approaching the fundamental physical limits of CMOS scaling.

Moreover, the apparatuses needed for the transistor fabrication process must push away the limits of accuracy.

Consequently, even if this approach remains attractive, the potential of performance improvements is limited today and alternative approaches have been investigated.

Another well known approach uses strained semiconductor substrates.

Indeed strained silicon technologies provide high electron mobility which translates into a performance enhancement of 20% to 30% for the NMOS transistor devices.

However, in this approach a particular attention must be brought to the electron to hole mobility ratio.

Indeed, when processing a classical non-strained bulk substrate for making CMOS circuits, this ratio is in the order of three, which means that the holes mobility is three times lower than the mobility of electrons, indicating thereby that a NMOS transistor device is usually three times faster than a PMOS transistor device.

Circuit designers are used to manage such ratio of the order of three.

They compensate this mobility imbalance by increasing the PMOS transistor width to length ratio when combining NMOS and PMOS transistors.

Consequently, for a fixed length value, the width and then the sizes of the PMOS transistor devices is increased.

Such compensation corresponds to limitations in term of area and overall circuit performance.

For example, increasing the width to length ratio increases the capacitances of the device which often penalizes the speed to power consumption ratio of the circuit (this is indeed the case when one electrical node connected to the PMOS device has critical effects on the transfer function of the circuit).

And in the case of strained silicon, the increase of electron mobility further increases the above mentioned ratio.

Therefore, despite the advantages associated to enhancing by 20% to 30% the electron mobility, strained silicon technology is associated to a high electron to hole mobility ratio and is exposed to the above mentioned limitations.

Another known solution consists of realizing PMOS and NMOS transistor devices with respective working layers having respectively a (1,1,0) and a (1,0,0) crystalline orientation.

It is indeed well-known that PMOS transistor devices exhibit better performance in a (1,1,0) crystal because their carriers mobility (the holes mobility) is enhanced.

As an example, in such a crystal, the holes mobility can be increased by a factor of 2,5 with respect to the one obtained in a (1,0,0) crystal.

Therefore, combining (e.g. in SOI structure) a first (1,0,0) semiconductor working layer with a second (1,1,0) semiconductor working layer in the same CMOS technology allows improving the mobility of both the NMOS and the PMOS transistor devices.

To this regard, such a SOI structure with a surface pattern based on two working layers, made respectively of a (1,0,0) and a (1,1,0) silicon has yet been proposed [1,2].

We will refer in this text to a "hybrid" structure for mentioning semiconductor multilayer structures with at least two working layers, made of respective semiconductor materials having different crystalline orientations.

Figures 1a to 1d illustrates an example of the manufacturing of such a hybrid structure which has been proposed.

The process begins on an intermediate structure S1 comprising a semiconductor working layer 10 placed on top of an insulator layer 11, the insulator layer covering a support semiconductor layer 20.

The layers 10 and 20 are typically made of silicon.

This intermediate structure is thus of the SOI type.

The working layer 10 and the support layer 20 have different crystal orientations. For example, the working layer 10 can have a (1,0,0) crystal orientation, and the support layer 20 can have a (1,1,0) crystal orientation.

Figure 1b further illustrates the removal of a portion of layers 10 and 11, in order to have a direct access to the corresponding portion of layer 20, through a free space 13.

As illustrated in figure 1c and 1d, the free space 13 thus created above layer 20 can be first partially filled with a vertical insulator 12, and then the remaining free space is filled with the same material as the material of layer 20, e.g. by epitaxial regrowth on support layer 20.

The layer of material thus created above the support layer forms an additional working layer 21 in the structure. This additional working layer is isolated from working layer 10 by the vertical insulator 12.

A hybrid multilayer structure S is thus created with two different working layers 10 and 21 having different crystal orientations.

In such a hybrid structure, NMOS transistor devices can be directly realized in the working layer 10.

Correspondingly, PMOS transistor devices can be directly built in the working layer 21.

However, such a hybrid substrate is associated with at least a major limitation: if the NMOS devices which will be built in working layer 10 shall be of the SOI type (since an insulating layer lies between layer 10 and the support 20), this shall not be the case concerning the PMOS devices made on layer 21.

Indeed, the layer 21 is directly in contact with the support layer 20, from which it is therefore not isolated. And the PMOS transistor devices that will be built in this working layer shall therefore be "bulk type" transistors.

Thus, such a structure is only capable to provide SOI NMOS transistor devices having a crystalline orientation (1,0,0) and bulk type PMOS transistor devices whose crystal orientation is (1,1,0).

The present invention has been conceived in order to overcome the above mentioned limitation.

An object of the invention is thus to provide a complete SOI hybrid structure, i.e. capable of providing both a (1,0,0) NMOS SOI transistor and a (1,1,0) PMOS SOI transistor.

A further object of the invention is to combine the full performance of an SOI substrate with the use of hybrid crystalline orientation structures.

And more generally, an object of the invention is to obtain a multilayer structure having at least two working layers corresponding to two different crystalline orientations, said working layers being electrically isolated from the support layer of the structure.

To that effect, the invention proposes, according to a first aspect, a SOI-type multilayer structure, comprising a support layer, at least two working layers having different crystalline orientations, an insulating layer extending over at least a portion of said support layer, characterized in that said insulating layer extends over the whole surface of said support layer, so as to extend between said support layer and said working layers.

Preferred aspects of such SOI-type multilayer structure according to the invention are the following:

- said at least two working layers are superimposed;
- the SOI-type multilayer structure comprises only two working layers;
- the working layers are made of silicon;
- a working layer is made of a (1,0,0) crystal and another working layer is made of a (1,1,0) crystal;
- said working layer made of a (1,0,0) crystal is adapted for the manufacturing of NMOS type transistors and said working layer made of a (1,1,0) crystal is adapted for the manufacturing of PMOS type transistors;
- the SOI-type multilayer structure comprises a plurality of different stacking areas, the layer composition of each stacking area being of one of the following types:

- first composition type: support layer – insulator layer – first working layer exposing its top surface,
- second composition type: support layer – insulator layer – first working layer – second working layer exposing its top surface,

so that within each of said stacking areas one of said first and second working layer exposes its top surface;

- the thickness of said first working layer in said first composition type is equal to the added thicknesses of said first and said second working layers in said second composition type so that the top surface of said structure is even;

- the working layers of a stacking area are electrically isolated from the working layers of the stacking areas placed around;

- this electrical isolation is performed by Shallow Trench Isolation;

- at least one working layer is mono-crystalline;

- at least one working layer is a strained semiconductor;

- this working layer is tensile or compressive strained;

- an additional electrical insulator layer lies between two working layers, so that said working layers are electrically isolated from each other;

- said insulating layer(s) is(are) made of oxide;

According to a second aspect, the invention provides a process for manufacturing a SOI-type multilayer structure according to the invention, said process using a layer transfer technique, characterized in that said process comprises the following steps:

- forming an intermediate structure including said support layer, a first working layer, and said insulating layer,
- forming on top of said intermediate structure a second working layer having a crystalline orientation which is different from the crystalline orientation of said first working layer.

Preferred aspects of this manufacturing process are the following:

- the process further comprises the following steps:
  - forming an intermediate structure by:
    - insulating layer above the support layer,
    - implanting species in a first source substrate in order to form an embrittlement zone which defines within said first source substrate a layer corresponding to a first working layer of said structure,
    - bonding said first source substrate to said insulating layer,
    - splitting said first source substrate at said embrittlement zone formed in said first source substrate, so that the portion of the first substrate source which remains bonded to the insulating layer becomes the first working layer of the intermediate structure,
  - forming on top of said intermediate structure a second working layer, by:
    - implanting species in a second source substrate in order to form an embrittlement zone which defines within said second source substrate a layer corresponding to a second working layer of said structure,
    - bonding said second source substrate to said first working layer,
    - splitting said second source substrate at said embrittlement zone formed in said second source substrate, so that the portion of the second substrate source which remains bonded to the first working layer becomes a second working layer of the SOI-type multilayer structure.

- the process further comprises a step of treating the surface of said intermediate structure before forming on top of said intermediate structure a second working layer;

- the process further comprises selective removing of desired portions of said second working layer, so that the SOI-type multilayer structure comprises two types of layer stacking:
  - first stacking type: support layer – insulator layer – first working layer,
  - second stacking type: support layer – insulator layer – first working layer – second working layer.

- the process further comprises selective forming of desired trenches which expose said insulating layer to the outer environment;
- the process further comprises filling said trenches with an electrical insulator;
- the working layers of said structure are semiconductor layers;
- the working layers are mono-crystalline layers;
- one of said working layers is made of a (1,0,0) crystal and another of said working layers is made of a (1,1,0) crystal;
- at least one of the working layers is strained;
- the working layer is tensile or compressive strained;
- before bonding the two working layers, said process comprising forming an additional insulating layer between said two working layers;
- said insulating layer(s) is(are) made of oxide.

Further aspects, objects and advantages of the present invention will be more clearly apparent on reading the following detailed description of a preferred implementation of the invention, this being given by way of non limiting example and with reference to appended drawings in which:

- figures 1 which has been commented above shows different steps of a prior art manufacturing process of a SOI-type multilayer structure comprising two working layers having different crystalline orientations,

- figure 2 schematically illustrates main steps of a process of manufacturing a SOI-type multilayer structure according to the invention when starting from an intermediate structure,
- figure 3 illustrates an example of steps for forming the intermediate structure,
- figure 4 illustrates in a more detailed manner the steps of the process of manufacturing a SOI-type multilayer structure according to the invention when starting form the intermediate structure,
- figure 5 shows a SOI-type multilayer structure according to the invention which comprises regions having respective different types of layer stacking,
- figure 6 shows a SOI-type multilayer structure according to the invention which comprises a trench which can be filled by an insulator,
- figure 7 shows a SOI-type multilayer structure according to the invention in which two working layers are separated by an insulator.

Referring now to figure 2, a SOI-type multilayer structure 105 according to the invention is obtained starting from an intermediate structure 100.

The intermediate structure 100 comprises a support layer 101 supporting an insulating layer 102.

This insulating layer 102 extends between said support layer 101 and a working layer 103.

Therefore this intermediate structure comprises a support layer, an insulating layer and a working layer.

However, other layers could be formed within such structure, the main idea being that the intermediate structure is at least composed of the three layers mentioned above.

To this regard, one draws the attention that in the invention, a working layer of a SOI-type structure is understood as a layer located above the insulating layer of the structure, and in which a channel of electrical current may be formed.

In other words, a working layer may serve as a layer for carrier transport.

As a non limitative example, in a NMOS SOI transistor, a working layer is a layer in which electrons are passing from a source to a drain of said transistor, so as to generate a controlled drain to source current.

Accordingly, it might happen that a working layer comprises more than one layer.

Additionally the material of such layers which form the working layer may be of any type.

As a non limitative example each of these layers may be made of material chosen independently in the non limitative list given below;

- semiconductor such as Ge, SiGe, Si,
- compound semiconductor such as GaAs, GaN, InSb, InP, etc.

Furthermore, each of these layers may be strained if desired (tensile and/or compressive).

Each of these layers may also consist in mono-crystalline materials with crystalline orientation substantially identical.

In order to obtain a SOI-type structure according to the invention, a second working layer 104 having a crystalline orientation which is different from the crystalline orientation of the working layer 103 is formed on top of said intermediate structure 100 (figure 2B).

Therefore in the hybrid structure 105 thus created, the second working layer 104 is in contact with the first working layer 103 and extends above it.

According to the invention the respective crystalline orientations of both the first and second working layers are chosen so as to optimize the mobility of the carriers which will get involved in these respective layers.

As a non limitative example, the first working layer 103 may be made of a (1,0,0) crystal in silicon and the second working layer 104 in a (1,1,0) crystal in silicon.

Such an arrangement makes it possible to obtain a SOI-type multilayer structure in which the first working layer is very well adapted for the manufacturing of NMOS type transistors while the second working layer is very well adapted to the manufacturing of PMOS type transistors.

As a further non limitative example, the first working layer 103 made of a (1,0,0) crystal in silicon may be tensile strain while the second working layer 104 in a (1,1,0) crystal in silicon may be compressive strain.

The method of forming the second working layer on top of the intermediate structure can be implemented in several ways know by the one skilled in the art.

As an example, an epitaxial growth can be performed using well known techniques such as CVD (for Chemical Vapour Deposition) or MBE (for Molecular Beam epitaxy) techniques.

However, according to a preferred method of the invention, the SOI-type multilayer structure is generally manufactured using a layer transfer technique which is especially described in the document entitled « Silicon On Insulator Technology: Materials to VLSI, 2nd edition » from Jean Pierre Colinge (Kluwer Academic Publishers).

To this regard, a detailed example of such a manufacturing method is shown in figure 3 for manufacturing the intermediate structure 100 whereas figure 4 describes detailed steps of such a method when used to manufacture the hybrid SOI-type multilayer structure 105, being understood that the method presented in figure 4 starts from said intermediate structure 100.

As can be seen in figure 3A, for manufacturing the intermediate structure one starts from the support layer 101 which can be made in materials such as silicon, sapphire, diamond, etc..., and which supports the insulator 102 over an entire surface (figure 3A).

Preferably, the insulator 102 may be a silicon oxide, also called silica or SiO2, because it is able to exhibit good adhesion with the support layer 101.

The insulator layer may also be composed of multiple layers having different distinct compositions.

It is to be noted here, that the silicon oxide may have been deposited over said surface of the support layer 101 by thermal oxidation or by other known techniques.

In figure 3B, a source substrate 107 having for example a (1,0,0) crystalline orientation is considered.

Atom species are implanted in this source substrate in order to form an embritllement zone 106 at a predefined depth within said source substrate.

As can be seen in this figure, such an implantation defines within said source substrate 107 a layer which will correspond to the first working layer 103 of the SOI-type structure which shall be obtained.

Thereafter, the source substrate 107 is brought into intimate contact with said silicon oxide 102 supported by layer 101 and both of these layers are bonded advantageously by molecular adhesion.

This bonding technique, as well as variants, is described for example in the document entitled "Semiconductor Wafer Bonding" (Science and Tecnhology, Interscience Technology) by Q. Y. Tong, U. Gösele and Wiley.

If necessary, bonding is accompanied by an appropriate prior treatment of at least one of the respective surfaces to be bonded.

As a non limitative example, such a treatment can be performed in order to allow the bond to be strengthened.

Once bonding has been performed as shown in figure 3C, the layer part 107' of the source substrate 107 which does not correspond to the working layer 103 is removed by splitting.

To that effect, energy is supplied in particular to the source substrate so that, due to mechanical constraints, said layer part 107' detaches from said source substrate 107 at the depth defined by the embritllement zone which is weakened.

Typically, said supply of energy can be performed with a heat treatment or other treatment known by the skilled man in the art.

In any case, figure 3D shows the resulting intermediate structure 100 composed successively, from top to bottom, of the (1,0,0) crystalline orientation working layer 103, the silicon oxide 102 and the support layer 101.

Referring now to figure 4, a method is illustrated for forming on top of said intermediate structure 100 a second working layer 104 having a crystalline orientation which is different from the crystalline orientation of the (1,0,0) working layer 103 of the intermediate structure.

According to the example mentioned above, said second working layer 104 may have a (1,1,0) crystalline orientation.

A preliminary step of this method consists in implanting atom species in a (1,1,0) source substrate 109 (figure 4B).

Once again an embritllement zone 108 is thus created at a predetermined depth within the source substrate 109, which can be different from the one mentioned previously, and defines within said second source substrate 109 a layer corresponding to said second working layer 104.

Then, the surface of the second source substrate corresponding to a surface of the second working layer 104 is brought into intimate contact with the surface of the first working layer 103 extending on top of the intermediate structure 100, and bonding is performed (figure 4C) with a heat treatment for example.

Finally, as shown in figure 4D, the layer part 109' of the second source substrate 109 which does not correspond to the second working layer 104 is removed by splitting said source substrate 109 at the embrittlement zone 108 and the hybrid SOI-type multilayer structure 105 of the invention is thus obtained.

Naturally, other steps in the methods described above may be included in the method of the invention.

In particular, one may integrate a step of treating the surface of the second working layer 104 after it has been bonded to the intermediate structure 100, and/or treating the surface of said intermediate structure 100 before forming on top of it the second working layer 104.

Indeed, after a splitting step, the surface of the working layer thus formed may comprise little roughness which can be cured with for example a thermal treatment such as an annealing treatment.

Further steps could also be accomplished after having created said hybrid SOI-type multilayer structure 105.

As an example, a further step consists in removing a desired portion of said second working layer 104.

Figure 5 shows such a kind of removal, but performed over the entire depth of the layer 104 in question.

Therefore, observed from the top, the surface of the hybrid SOI structure 105 shows regions where the apparent layer is the first working layer and regions where the apparent layer is the second working layer.

This makes it possible to access to both of them in the case for example of fabricating transistors of two different types.

In figure 5 however, such a kind of hybrid SOI structure is seen in cross-section.

A doted line I clearly distinguishes two stacking areas 200 and 201.

A stacking area corresponds to an elementary layer pattern comprising either the support layer 101, the insulating layer 102 and the first working layer, or the support layer, the insulating layer, the first working layer and the second working layer 104.

Typically, removing a desired portion from the second working layer as illustrated in figure 5 can be performed by selective chemical etching, but the skilled man will be able to choose any other techniques known in the state of the art which will be best appropriate in particular cases.

Further, it may be also understood that, if desired, the overall thickness of the working layers in a stacking area (for example, the thickness of the

working layer 103 in the stacking area 201) can be made equal to the overall thickness of the working layers in another staking area (in the above example, the added thickness of the first and the second working layer 103 and 104 in the stacking area 201), so that the top surface of the structure 105 is even

Figure 6 shows another additional step which can be implemented in order to electrically isolate the working layer(s) of a stacking area 202 from the working layer(s) of other stacking areas around.

To that effect, a trench 100 is formed through the entire depth of the working layers of the stacking area which has to be isolated (figure 6A).

As can be understood, such a trench is also formed so as to surround the working layer(s) of said stacking area 202, and this along its(their) depth.

Then the trench 110 is filled with an electrical insulator (figure 6B), preferably the same insulator than the one 102 used to electrically isolate the working layers from the support layer 101, e.g. the SiO2 layer.

Consequently, said trench may be in the form of shallow trench isolation (STI).

A particular advantage of such a further step resides in the fact that a transistor fabricated in a stacking area is electrically isolated from components, such as other transistors, fabricated in other stacking areas and more particularly from components fabricated in adjacent stacking areas.

It is to be noted too that in a stacking area thus manufactured, the first working layer 103 extending just above the second working layer 104 may be used to bias said second working layer 104.

To do so, at least a via may be provided to contact specifically the first working layer 103 to an electrical source generating the bias voltage or the bias current.

In this manner, the threshold voltage of the second working layer 104 may be modified as desired and in a very convenient way.

In particular, such a solution may also help saving layout area.

Another embodiment of the invention is also illustrated in figure 7.

As can be seen, the hybrid SOI-type structure comprises an additional insulating layer 111 which is interposed between the first and second working layers 103 and 104 having respectively different crystalline orientations.

An advantage of such a structure resides in the fact that, the working layers of a stacking area being electrically isolated one another, a component, such as transistor, which may be manufactured from the second working layer 104 is no more subjective to electrical perturbations which would be present in the first working layer 103.

To this end, the method of manufacturing the hybrid SOI-type structure proposed by the invention can be completed by an additional step of forming said second insulating layer 111.

As a non limitative example, this insulating layer 111 may be obtained by oxide deposition on the top surface of the first working layer before having transferred the second working layer to the structure.

As another example, said insulating layer 111 may be first deposited on the second source substrate 107 represented in figure 3B.

Then implantation of atom species is performed trough such a temporary structure in order to create a weakened zone, namely an embritllement zone, within said second source substrate 107.

The free surface of the insulating layer 111 is brought into intimate contact with the top surface of the first working layer 103 and bonded with one of the techniques sus-mentioned.

Naturally, the scope of the invention is not limited to the various embodiments described above as examples.

In particular, a working layer of the SOI-type multilayer structure of the invention may have a (1,1,1) crystalline orientation to manufacture for example a PMOS transistor.

CLAIMS

1. SOI-type multilayer structure (105), comprising a support layer (101), at least two working layers (103, 104) having different crystalline orientations, an insulating layer (102) extending over at least a portion of said support layer (101), characterized in that said insulating layer (102) extends over the whole surface of said support layer (101), so as to extend between said support layer (101) and said working layers (103, 104).

2. SOI-type multilayer structure according to claim 1, characterized in that said at least two working layers (103, 104) are superimposed.

3. SOI-type multilayer structure according to the preceding claim, characterized in that the structure comprises only two working layers (103, 104).

4. SOI-type multilayer structure according any of the preceding claims, characterized in that the working layers (103, 104) are made of silicon.

5. SOI-type multilayer structure according any of the preceding claims, characterized in that a working layer (103) is made of a (1,0,0) crystal and another working layer (104) is made of a (1,1,0) crystal.

6. SOI-type multilayer structure according to the preceding claim, characterized in that said working layer (103) made of a (1,0,0) crystal is adapted for the manufacturing of NMOS type transistors and said working layer (104) made of a (1,1,0) crystal is adapted for the manufacturing of PMOS type transistors.

7. SOI-type multilayer structure according to any of the preceding claims, characterized in that it comprises a plurality of different stacking

areas (200, 201), the layer composition of each stacking area being of one of the following types:

- first composition type: support layer – insulator layer – first working layer exposing its top surface,
- second composition type: support layer – insulator layer – first working layer – second working layer exposing its top surface,

so that within each of said stacking areas one of said first and second working layer exposes its top surface.

8. SOI-type multilayer structure according to the preceding claim, further characterized in that the thickness of said first working layer (103) in said first composition type is equal to the added thicknesses of said first and said second working layers (103, 104) in said second composition type so that the top surface of said structure is even.

9. SOI-type multilayer structure according to any of the two preceding claims characterized in that the working layers (103, 104) of a stacking area (200) are electrically isolated from the working layers of the stacking areas (201) placed around.

10. SOI-type multilayer structure according to the preceding claim characterized in that said isolation is performed by Shallow Trench Isolation.

11. SOI-type multilayer structure according to any of the preceding claims, characterized in that at least one working layer is mono-crystalline.

12. SOI-type multilayer structure according to any of the preceding claims, characterized in that at least one working layer is a strained semiconductor.

13. SOI-type multilayer structure according to the preceding claim characterized in that the working layer is tensile or compressive strained.

14. SOI-type multilayer structure according to any of the preceding claims, characterized in that an additional electrical insulator layer (111) lies between two working layers (103, 104), so that said working layers are electrically isolated from each other.

15. SOI-type multilayer structure according to any of the preceding claims, characterized in that said insulating layer(s) (102, 111) is(are) made of oxide.

16. Process for manufacturing a SOI-type multilayer structure (105) according to one of the preceding claims said process using a layer transfer technique, characterized in that said process comprises the following steps:

- forming an intermediate structure (100) including said support layer (101), a first working layer (103), and said insulating layer (102),
- forming on top of said intermediate structure (100) a second working layer (104) having a crystalline orientation which is different from the crystalline orientation of said first working layer (103).

17. Process according to the preceding claim, characterized in that it further comprises the following steps:

- forming an intermediate structure (100) by:
  - insulating layer above the support layer (101),
  - implanting species in a first source substrate (107) in order to form an embrittlement zone (106) which defines within said first source substrate a layer corresponding to a first working layer (103) of said structure,
  - bonding said first source substrate (107) to said insulating layer (102),
  - splitting said first source substrate (107) at said embrittlement zone (106) formed in said first source substrate, so that the

portion of the first source substrate which remains bonded to the insulating layer (102) becomes the first working layer (103) of the intermediate structure,

- forming on top of said intermediate structure (100) a second working layer (104), by:
  - implanting species in a second source substrate (109) in order to form an embrittlement zone (108) which defines within said second source substrate a layer corresponding to a second working layer (104) of said structure,
  - bonding said second source substrate (109) to said first working layer (103),
  - splitting said second source substrate (109) at said embrittlement zone (108) formed in said second source substrate, so that the portion of the second substrate source which remains bonded to the first working layer (103) becomes a second working layer (104) of the SOI-type multilayer structure.

18. Process according to the preceding claim, characterized in that said process comprises a step of treating the surface of said intermediate structure (100) before forming on top of said intermediate structure a second working layer (104).

19. Process according to any of the two preceding claims characterized in that it further comprises selective removing of desired portions of said second working layer (104), so that the SOI-type multilayer structure (105) comprises two types of layer stacking (200):

- first stacking type: support layer – insulator layer – first working layer,
- second stacking type: support layer – insulator layer – first working layer – second working layer.

20. Process according to any of the three preceding claims, characterized in that it further comprises selective forming of desired trenches (110) which expose said insulating layer (102) to the outer environment.

21. Process according to the preceding claim, characterized in that the process further comprises filling said trenches (110) with an electrical insulator.

22. Process according to any of the five preceding claims, characterized in that the working layers (103, 104) of said structure (105) are semiconductor layers.

23. Process according to any of the six preceding claims, characterized in that the working (103, 104) layers are mono-crystalline layers.

24. Process according to any of the seven preceding claims, characterized in that one (103) of said working layers is made of a (1,0,0) crystal and another (104) of said working layers (103, 104) is made of a (1,1,0) crystal.

25. Process according to any of the eight preceding claims, characterized in that at least one of the working layers (103, 104) is strained.

26. Process according to the preceding claim, characterized in that the working layer is tensile or compressive strained.

27. Process according to any of the ten preceding claims, characterized in that, before bonding the two working layers (103, 104), said process comprising forming an additional insulating layer (111) between said two working layers (103, 104).

28. Process according to any of the eleven preceding claims, characterized in that said insulating layer(s) (102, 111) is(are) made of oxide.