METHOD FOR FORMING FULLY SILICIDED GATE ELECTRODES AND UNSILICIDED POLY RESISTORS

BACKGROUND

[0001] The present invention relates generally to integrated circuits, and more particularly to methods for fabricating integrated circuits. Still more particularly, the present invention relates to methods for forming fully silicided gate electrodes while also providing unsilicided resistors.

[0002] As technology becomes more advanced, the design of integrated circuits (ICs) becomes more complicated. To further increase performance and reduce cost, improvements to the structural design of the IC as well as the processing methods to fabricate the ICs are of paramount importance. For example, scaling to lower gate oxide thickness to achieve higher gate capacitance is required as transistor channel lengths are decreased in order for the gate electrode to maintain control of the channel. In doped poly-silicon gate electrodes, the finite solubility of dopant atoms places a lower limit on gate resistance and leads to the formation of a finite thickness space charge layer depleted of free charge carriers at the gate electrode/oxide interface. This insulating poly-depletion layer increases the effective oxide thickness, decreasing overall gate capacitance, and poses a severe limitation to device scaling.

[0003] Replacing the poly-silicon gate electrode with a metal gate electrode relieves the problem of poly-depletion due to the high carrier concentration available in the metal. However, metal gates face numerous challenging process integration issues including metal etch process development, thermal budget constraints, and metal contamination. One attractive option is to alloy a metal with a conventionally patterned poly-silicon gate electrode in its entirety to form a fully silicided gate electrode. Since conventional IC processes already rely on a single silicide formation process to concurrently fabricate

contacts to poly gate electrodes and source/drains, a fully-silicided gate can potentially be integrated with minimal process modification.

[0004] In conventional IC fabrication, silicide contacts to the source/drains and the doped poly-silicon gate electrodes are formed after source/drain implants are annealed and before deposition of device passivating dielectric layer. Sputter deposition of a blanket metal film is followed by a thermal process to react the metal with exposed silicon areas on the wafer forming silicide contacts to the source/drain and the gate electrode. Since the source/drain silicide contact depth must be minimized to prevent excess junction leakage and the poly-silicon gate electrode is typically thicker than the depth of the source/drain silicide contact, only the top portion of the poly-silicon gate electrode is silicided. Excess unreacted metal including metal deposited on dielectric spacers and isolation is then removed by a wet etch. Since only areas with exposed silicon are silicided, the process is self-aligned, and often referred to as a salicide process.

[0005] The primary process modification required to form an IC with fully-silicided gate electrodes is to maintain shallow the source/drain silicide contacts while achieving full-silicidation of the gate electrodes. One method of decoupling source/drain silicidation from full gate silicidation is to perform the conventional silicidation followed by an additional silicidation of the gate alone. To prevent additional silicidation of the source/drains, the second silicidation is performed after dielectric layers are blanket deposited to passivate the source/drains and polished back to expose only the gate electrode.

[0006] In a conventional IC process the same doped poly-silicon layer used to form the gate electrode also serves to form poly silicon resistors which are of high value for various circuit designs. The resistivity of silicided polysilicon is substantially lower than that of un-silicided doped polysilicon, therefore it is desirable to use un-silicided doped polysilicon in order to minimize the chip surface area required to accommodate a resistor of a given resistor. In the conventional IC process, this is achieved by patterning an additional dielectric layer after source/drain implant and before silicidation in order to

protect the polysilicon resistors from silicidation. In the full silicidation process, since there are two silicidation steps, additional measures must be taken to prevent silicidation of polysilicon resistors. As such, desirable in the art of IC fabrication are additional structural designs and processing methods that may enable and simplify concurrent formations of fully silicided gate electrodes and high resistance poly-silicon resistors.

SUMMARY

[0007] In view of the foregoing, this invention provides a design and method that both enable and simplify concurrent formations of gate electrode and resistor 2.

[0008] In one embodiment, after patterning a semiconductor material for the gate electrode and resistor structures, a first dielectric layer is used to protect a poly resistor that is not to be silicided, then a first silicidation is performed for partially siliciding the gate electrode of the transistor. If the gate electrode is thick, a second dielectric layer is used to protect the resistor that is not to be silicided, then a second silicidation is performed for fully siliciding the gate electrode.

[0009] The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIGs. 1A to 1E are partial sectional views of semiconductor structures that illustrate the processing steps required to fabricate a thin gate poly transistor in accordance with a first embodiment of the present invention.

[0011] FIGs. 2A to 2G are partial sectional views of semiconductor structures that illustrate the extra processing steps required to fabricate a thick gate poly transistor in accordance with a second embodiment of the present invention.

[0012] FIG. 3 presents a flow chart illustrating the processing steps in both the first and the second embodiments of the present invention.

DESCRIPTION

[0013] In the following two embodiments, this present invention provides an improved method for the production of metal-oxide-semiconductor field-effect-transistor (MOSFET) integrated circuits (ICs). The improved design provides simultaneous production of both silicided MOSFETs and unsilicided polycrystalline silicon or amorphous silicon resistors. The sources and drains in the substrate of the MOSFETs are partially silicided. The polysilicon or amorphous silicon gates of the MOSFETs are fully silicided. In certain situations, the prevention of silicidation of the resistors requires a dielectric silicide-blocking layer, typically oxide, to block contact of a deposited metal layer with the polycrystalline or amorphous silicon material of the resistor.

[0014] FIGs. 1A to 1E are partial sectional views of semiconductor structures that illustrate the processing steps required to fabricate a thin gate poly transistor in accordance with a first embodiment of the present invention. When using the thin gate poly, the thickness thereof is preferred to be under 500 angstroms. FIG. 1A presents a partial sectional view 100 in accordance with the first embodiment of the present invention. The partial sectional view 100 includes a MOS transistor 102 and a resistor poly 104, both of which are formed and diffused with sidewall spacers 106. The MOS transistor 102 overlies a semiconductor substrate 107. The resistor poly 104 may or may not be diffused. The MOS transistor 102 includes a gate poly 108, that is deposited on a gate dielectric 109, that is preferably a thermally grown oxide, a source 110, and a drain 112. The resistor poly 104 overlies an isolation structure 113, such as shallow trench isolation (STI) or local oxidation of silicon. It is however understood by those skilled in the art that the positions of the source 110 and the drain 112 are typically interchangeable.

[0015] FIG. 1B presents a partial sectional view 114 in accordance with the first embodiment of the present invention. A first dielectric layer 116 is deposited onto both the

gate poly 108 and the resistor poly 104. The first dielectric layer 116 is a silicide-blocking layer that may be made of one or more predetermined oxides.

[0016] FIG. 1C presents a partial sectional view 118 in accordance with the first embodiment of the present invention. The first dielectric layer 116 is partially etched (for embodiment, using a wet etching process) from the gate poly 108, the source 110 and the drain 112. It is however noted that the first dielectric layer 116 remains on the resistor poly 104.

[0017] FIG. 1D presents a partial sectional view 120 in accordance with the first embodiment of the present invention. A first metal layer 122 is deposited on the gate poly 108, the source 110 and the drain 112, with the first dielectric layer 116 protecting the resistor poly 104.

[0018] FIG. 1E presents a partial sectional view 124 in accordance with the first embodiment of the present invention. A high-temperature process alloys the first metal layer 122, shown in FIG. 1D, into the exposed silicon of the gate poly 108, shown in FIG. 1D, and the exposed silicon of both the source 110 and the drain 112. The result is the formation of a fully silicided thin gate poly 126, a silicided source 128, and a silicided drain 130. The first dielectric layer 116 protects the resistor poly 104 from the metal silicidation process. Excess, unalloyed metal is also removed in this step.

[0019] FIGs. 2A to 2G are partial sectional views of semiconductor structures that illustrate extra processing required to fabricate a thick gate poly transistor in accordance with a second embodiment of the present invention. A thick gate poly is so defined when its thickness exceeds 500 angstroms. FIG. 2A presents a partial sectional view 200 in accordance with the second embodiment of the present invention. The partial sectional view 200 is formed by the processing steps as illustrated in FIGs. 1A through 1D, but with thick poly, and it includes the MOS transistor 202 and the resistor poly 204, both of which are formed and diffused with sidewall spacers 206. The MOS transistor 202 overlies a semiconductor substrate 207. The MOS transistor 202 includes a thick gate poly 208, which

is deposited on a gate dielectric 209, a source 210, and a drain 212. The resistor poly 204 overlies an isolation structure 213, such as shallow trench isolation or local oxidation of silicon, and it is protected by the first dielectric layer 214 .

[0020] After a first silicidation, the silicided upper portion 216 of the thick gate poly 208, the silicided source 218 and the silicided drain 220 are formed. While both FIGs. 1E and 2A illustrate a silicidation process, a smaller proportion of total thickness of the thick gate poly 208 is converted to silicide in FIG. 2A.

[0021] FIG. 2B presents a partial sectional view 222 in accordance with the second embodiment of the present invention. An inter-layer dielectric (ILD) layer 224 is first deposited. At this stage, it is understood that the thick gate poly 208 has the silicided upper portion 216, while the source 210 and the drain 212 of the MOS transistor 202 are fully silicided as silicided source 218 and silicided drain 220. Again, the resistor poly 204 is protected from this process by the first dielectric layer 214.

[0022] FIG. 2C presents a partial sectional view 226 in accordance with the second embodiment of the present invention. The ILD layer 224 is planarized by a planarization process such as a chemical-mechanical polish (CMP), thereby exposing the silicided upper portion 216 and the resistor poly 204 .

[0023] FIG. 2D presents a partial sectional view 228 in accordance with the second embodiment of the present invention. A second dielectric layer 230 is deposited onto both the silicided upper portion 216 and the resistor poly 204. The second dielectric layer 230 is effectively a silicide-blocking layer, typically oxide, which is used to block contact of a deposited metal layer with the polycrystalline or amorphous silicon body of the resistor.

[0024] FIG. 2E presents a partial sectional view 232 in accordance with the second embodiment of the present invention. The second dielectric layer 230 is etched from the silicided upper portion 216, and is left protecting the resistor poly 204 .

[0025] FIG. 2F presents a partial sectional view 234 in accordance with the second embodiment of the present invention. A second metal layer 236 is deposited on both the silicided upper portion 216 of the thick gate poly 208 and the remaining second dielectric layer 230. It is noted that the second metal layer 236 is in contact with none of the resistor poly 204, the silicided source 218, or the silicided drain 220.

[0026] FIG. 2G presents a partial sectional view 238 in accordance with the second embodiment of the present invention. A second high-temperature process alloys the second metal layer 236, shown in FIG. 2F, into the silicided upper portion 216 of the thick gate poly 208, shown in FIG. 2F, thereby forming a fully silicided thick gate poly 240. Typically, about 90 percent of the thick gate poly 208/gate dielectric 209 interface area, shown in FIG. 2A, is silicided. The gate poly is now deemed to be fully silicided. Meanwhile, the silicided source 218 and the silicided drain 220 are protected from further silicidation by the ILD layer 224. The resistor poly 204 is not silicided because it is protected from this second alloy process by the second dielectric layer 230. Excess, unalloyed metal is removed from the ILD layer 224 and from the second dielectric layer 230. This second silicidation cycle (FIGs. 2B to 2G) continues from the earlier partial silicidation (FIG. 2A) of the gate poly, and achieves the expected full silicidation result.

[0027] FIG. 3 presents a flow chart 300 illustrating the processing steps in both the first and the second embodiments of the present invention. In step 302, the dielectric layer 116 is deposited, as also illustrated in FIG. 1B. In step 304, the dielectric layer 116 is etched from the MOS transistor 102, as also illustrated in FIG. 1C. In step 306, the first metal layer 122 is deposited on the gate poly 108, the source 110 and the drain 112, as also illustrated in FIG. 1D. In step 308, the high-temperature process alloys the first metal layer 122, thereby forming the fully silicided thin gate poly 126, the silicided source 128 and the silicided drain 130 as also illustrated in FIG. 1E. In step 310, it is determined whether the semiconductor device is a thin gate poly device or a thick gate poly device. If the semiconductor device is a thin gate poly device, the flow ends. By contrast, if the semiconductor device is a thick gate poly device (e.g., the thickness is more than 500

angstroms), the flow continues to step 312, where the ILD layer 224 is deposited as also illustrated in FIG. 2B. In step 314, the ILD layer 224 is planarized by CMP, thereby exposing the silicided upper portion 216 and the resistor poly 204, as also illustrated in FIG. 2C. In step 316, the second dielectric layer 230 is deposited onto both the silicided upper portion 216 and the resistor poly 204, as also illustrated in FIG. 2D. In step 318, the second dielectric layer 230 is etched away, thereby exposing the silicided upper portion 216, as also illustrated in FIG. 2E. In step 320, the second metal layer 236 is deposited on both the silicided upper portion 216 of the thick gate poly 208 and the remaining second dielectric layer 230, as also illustrated in FIG. 2F. In step 322, the high-temperature process alloys the second metal layer 236 with the thick gate poly 208, thereby completing the silicidation of the thick gate poly 208, as also illustrated in FIG. 2F. After excess metal may be etched away, a thick gate poly transistor device is fabricated.

[0028] The semiconductor substrate can be silicon, silicon/germanium, or germanium. The semiconductor substrate can be a bulk substrate or constructed as a semiconductor on insulator (SOI) substrate. The gate dielectric can be silicon dioxide, nitrogen containing silicon oxide, or a material with a dielectric constant >4. The metal silicide can be formed by alloying cobalt, nickel, cobalt/nickel, tungsten, platinum, zirconium, or titanium with a silicon substrate or poly. The resistor material can be poly or amorphous silicon, or silicon/germanium alloy with no silicide formation, as there is for the gate structure. The sidewall spacer can be formed of silicon dioxide, nitrogen containing dielectric, or a combination of the two. The silicide-block layer can be formed of a dielectric, such as, silicon dioxide, silicon nitride, nitrogen-containing dielectric or a similar material.

[0029] The above invention provides many different embodiments or embodiments for implementing different features of the invention. Specific embodiments of components and processes are described to help clarify the invention. These are, of course, merely embodiments and are not intended to limit the invention from that described in the claims.

[0030] Although the invention is illustrated and described herein as embodied in a design and method for, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims. Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the invention, as set forth in the following claims.

WHAT IS CLAIMED IS:

1. A method for forming a transistor and unsilicided resistor on a semiconductor substrate, comprising:

forming at least one gate electrode for the transistor and a resistor region using a semiconductor material;

forming a first dielectric layer covering the resistor region;

performing a first silicidation process for partially siliciding the gate electrode without siliciding the resistor region;

forming a second dielectric layer covering the resistor region; and

performing a second silicidation process for fully siliciding the gate electrode.

2. The method of claim 1 wherein the step of forming a second dielectric layer covering the resistor region comprises:

forming a second dielectric layer covering both the transistor and the resistor region;

removing a portion of the second dielectric layer for exposing the gate electrode and the resistor region;

forming a third dielectric layer covering the exposed resistor region

3. The method of claim 1 wherein the semiconductor substrate is a bulk substrate.

4. The method of claim 1 wherein the semiconductor substrate is a semiconductor on insulator (SOI) substrate.

5. The method of claim 1 wherein the semiconductor substrate is made of silicon, germanium, or silicon/germanium alloy.

6. The method of claim 1 further comprising forming a gate dielectric layer for the transistor on the semiconductor substrate before the forming at least one gate electrode.

7. The method of claim 6 wherein the gate dielectric layer is made of silicon oxide, nitrogen containing silicon oxide, or any dielectric material having a dielectric constant greater than 4.

8. The method of claim 1 further comprising forming an isolation structure in the semiconductor substrate.

9. The method of claim 8 wherein the resistor region overlies the isolation structure.

10. The method of claim 8 wherein the gate electrode overlies the semiconductor substrate at a location absent from the isolation structure.

11. The method of claim 1 wherein the semiconductor material is a polycrystalline silicon, amorphous silicon, or silicon/germanium alloy.

12. The method of claim 1 furthering comprising forming one or more spacers covering sidewalls of the gate electrode or the resistor region.

13. The method of claim 12 wherein the spacer is made of silicon oxide or a nitrogen containing dielectric material.

14. The method of claim 1 wherein the step of performing the first or second silicidation process further includes placing a metal layer on the gate electrode; and performing a high-temperature process for alloying the metal into the gate electrode.

15. The method of claim 14 wherein the metal layer includes nickel, cobalt, tungsten, platinum, zirconium, titanium or an alloy thereof.

16. The method of claim 1 wherein the gate electrode is at least 90 percent silicided after the second silicidation process.

17. The method of claim 1 wherein the gate electrode has a thickness of more than 500 angstroms.

18. The method of claim 1 wherein the first or third dielectric layer includes silicon oxide.

19. The method of claim 1 wherein the first or third dielectric layer includes a nitrogen containing dielectric material.