

DECISION FEEDBACK EQUALIZATION WITH COMPOSITE TRELLIS SLICER

CROSS REFERENCE TO RELATED APPLICATIONS

- 5 [0001] This application claims priority under 35 USC §119(e) from provisional application no. 60/752,620, filed December 20, 2005 and entitled ITERATION DECODING FOR ATSC STANDARD (inventor: Yuwei Zhang), which is incorporated herein in its entirety for all purposes.

TECHNICAL FIELD

10 [0002] The invention relates to processing of digital input signals and more particularly to an improved method, system and apparatus to decode trellis-encoded communication signals such as signals encoded according to an Advanced Television Systems Committee (ATSC) standard.

BACKGROUND

15 [0003] A conventional decision feedback equalizer system 100 is shown as Fig. 1. An input digital signal $r(n)$ 102 is a trellis-encoded communication signal, such as a signal that is trellis-encoded according to an ATSC standard. The input digital signal $r(n)$ 102 of equalizer system 100 is typically multipath contaminated. The multipath contamination is caused by multiple signal propagation paths. Multipath contamination is typically a primary contributor to intersymbol interference in information carried within a communication signal.

20 [0004] The input digital signal 102 is provided to a feed-forward linear filter (FFE) 104. After passing the FFE 104, the thus-filtered input signal 106 can be represented as $Y(n)$ by the formula shown in Equation (1):

$$Y(n) = d_n + n_n + isi_n \quad (1)$$

25 In Equation (1), d_n is the data to be recovered from the input digital signal 102, n_n is white noise in the input digital signal 102, and isi_n is the inter-symbol-interference component of the input digital signal 102. The inter-symbol-interference component is nominally cancelled out by the decision feedback filter (DFE) 108. In Figure 1, the DFE input 110 comes from a simple slicer 112. However, phase jitter in the output of the FFE 104 reduces the effectiveness of the DFE output in canceling out the inter-symbol-interference in the FFE 104 output.

SUMMARY

[0005] In accordance with an aspect, a decision feedback equalizer is configured to equalize an input signal to generate a recovered output signal. Linear feed-forward
5 filter circuitry is configured to provide a linearly filtered output signal based on the input signal. Composite trellis decoder circuitry configured to process a combined signal that is based on a combination of at least the linearly feed-forward filtered output signal and on output of linear or non-linear feedback filter circuitry, in accordance with state metrics generated by processing a composite trellis diagram
10 relative to the combined signal, to provide a trellis-decoded output signal as input to the linear or non-linear feedback filter circuitry. The composite trellis decoder circuitry is further configured to provide a particular phase output of the combined signal, based on the state metrics, as the decoded output signal.

BRIEF DESCRIPTION OF THE DRAWINGS

- 15 [0006] Fig. 1 illustrates a conventional decision feedback equalizer system.
- [0007] Fig. 2 is similar to Fig. 1, but discloses using a partial trellis decoder in place of a simple slicer.
- [0008] Fig. 3 illustrates a portion of a trellis encoder that conforms to an ATSC
20 standard.
- [0009] Fig. 4 illustrates a decision feedback equalizer system in which a carrier recovery loop portion is included, as well as an equalizer portion.
- [0010] Fig. 5 illustrates an equalizer in which a carrier recovery loop is placed after the FFE.
- 25 [0011] Fig. 6 illustrates a composite trellis decoder being employed in place of a simple slicer or of a partial trellis decoder.
- [0012] Fig. 7 shows a system ideal constellation of 8VSB for a jitter-free condition.
- [0013] Fig. 8 illustrates an example of the constellation of 8VSB under a phase jitter condition.
- 30 [0014] Fig. 9 illustrates a composite trellis slicer.
- [0015] Fig. 10 illustrates a simulation model of phase jitter.
- [0016] Fig. 11 illustrates simulation results, of decoding using a decoder like the Fig. 6 decoder, of the simulation model of Fig. 10.

DETAILED DESCRIPTION

[0017] Referring to Fig. 1 discussed in the Background, reducing the slicing error of the simple slicer 112 will improve the accuracy of DFE output isi_n 114. Since the DFE output isi_n 114 is used to cancel the intersymbol interference from the output of the FFE 104, improving the accuracy of the DFE output isi_n 114 should result in an overall improvement in performance of the equalizer system 100.

[0018] N. Hulyalkar et al. has disclosed using a partial trellis decoder in place of the simple slicer 112, as shown in Fig. 2. The partial trellis decoder is shown as element 112' in Fig. 2. Fig. 3 illustrates a portion of a trellis coder (i.e., on the encoding side, as opposed to the decoding side) that conforms to an ATSC standard. With the trellis coding that conforms to the ATSC standard, the partial trellis decoder (112', Fig. 2) outperforms the simple slicer (112, Fig. 1) by about 4 to 6 dB (in terms of decision error probability) under an additional white Gaussian noise channel condition.

[0019] Thus, the use of the partial trellis decoder 112' theoretically results in a significant improvement of equalizer performance, as opposed to using the simple slicer 112. However, the above discussion assumes an ideal case, that is, a case in which the input signal of the equalizer is free from carrier offset and/or phase jitter. However, the actual situation is typically much different from the ideal case.

[0020] To address the carrier offset, carrier recovery functionality may be included. Fig. 4 shows a system block diagram of a decision feedback equalizer system 400 in which a carrier recovery loop portion 402 is included, as well as an equalizer portion 404. We now discuss a theory of operation of the decision feedback equalizer system 400 shown in Fig. 4.

[0021] Let ω_c denote the signal carrier frequency and ω_l denote the local carrier frequency. The carrier offset $\Delta\omega$ is characterized as shown in Equation (2):

$$\Delta\omega = \omega_c - \omega_l \quad (2)$$

Thus, the input to the equalizer portion 404 (i.e., the output of the carrier recovery loop 402) can be expressed as $r(n)e^{j\Delta\omega n}$. If $W(n)$ denotes the FFE 406 output, then:

$$\begin{aligned} W(n) &= \sum_{i=0}^{N-1} C_i r(n-i) e^{j\Delta\omega(n-i)} \\ &= e^{j\Delta\omega n} \sum_{i=0}^{N-1} C_i r(n-i) e^{-j\Delta\omega i} \\ &= Y(n) e^{j\Delta\omega n} \end{aligned} \quad (3)$$

In Equation (3), N denotes the number of taps of the FFE 406, and C_i ($i = 0, 1, \dots, N-1$) is the coefficient of taps.

[0022] When the carrier recovery loop 402 gets lock, $\Delta\omega$ will trend to close to zero, with a small residual offset that is independent of time. So, in equation (3), $e^{-j\Delta\omega i}$ ($i = 0, 1, \dots, N-1$) is independent of time and can be compensated by the FFE 406 with properly adjusted tap coefficients. On the other hand, the phase factor, $e^{j\Delta\omega n}$ is a time related variable and should be the major source of phase jitter. Therefore, under a phase jitter condition, the FFE 406 should produce the same output as in the ideal case, except for the phase factor.

[0023] With the effect of the phase factor, however well the slicer (e.g., either the simple slicer 112 in Fig. 1 or the partial trellis decoder 112' in Fig. 2) performs, the final output of the equalizer 100 or 200 will be

$$\begin{aligned} E(n) &= Y(n)e^{j\Delta\omega n} + ISI_n \\ &= (d_n + n_n + ISI_n)e^{j\Delta\omega n} + ISI_n \quad (4) \\ &= (d_n + n_n)e^{j\Delta\omega n} + ISI_{offset} \end{aligned}$$

where ISI_{offset} is the total equivalent inter-symbol-interference. Even if the inter-symbol-interference could approach zero, the equalizer output will still contain a phase factor, which will lower the signal-to-noise ratio of the final output.

[0024] From equation (3), it can be seen that the phase property of the FFE input 102 (using the reference numerals of Figs. 1 and 2) can be transparently transferred to the FFE output 106. For example, as shown in Fig. 5, the carrier recovery loop (shown as 502 in Fig. 5) can be moved to after the FFE. However, with this structure, the phase factor is still an issue for the slicing functionality. In addition, function blocks ahead of the FFE (for example, a channel estimator) will be operating under the carrier offset condition.

[0025] For decoding a signal encoded according to a continuous phase modulation (CPM) encoding scheme, R. Huff proposed a composite trellis concept for carrier recovery based on the inherent phase trellis structure of CPM. See US Patent No. 5,974,091, issued October 26, 1999. Huff also discloses generalizing the composite trellis concept to other modulation schemes.

[0026] Referring to Fig. 6, the inventor has realized that the composite trellis decoder technique (composite trellis decoder 602) can be utilized to process the output of the FFE 604 and of the DFE 606. Referring to Fig. 9 as well, from the output of the FFE

604 and of the DFE 606, the composite trellis decoder 602 determines a signal 610 to feedback as input to the DFE 606, as well as determining the equalizer output 608.

For example, the same state metrics comparator 902 (and even the same state metrics comparator 902 output signal) may be used to determine each of the equalizer output

5 608 and the signal 610 to feedback as input to the DFE 606.

[0027] Thus, for example, to account for the effect of the phase factor, as discussed extensively above, the composite trellis technique may be employed. For 8VSB (8-level vestigial sideband, the RF modulation scheme used by digital television, in accordance with the ATSC encoding standard), Fig. 7 shows a system ideal

10 constellation for a jitter-free condition.

[0028] An example of the constellation of 8VSB is shown in Fig. 8 under a phase jitter condition. To address the effect of the phase jitter, the composite trellis decoder is included, such as shown in Fig. 9. A simulation model of phase jitter is shown in Fig. 10, and the simulation results are shown in Fig. 11.

15 [0029] Details of operation of a simple composite trellis decoder are provided in US Patent No. 5,974,091, incorporated herein by reference in its entirety. As mentioned above, in the Fig. 9 composite trellis decoder, the same output of the state metrics comparator 902 is used to determine each of the equalizer output 608 and the signal 610 to feedback as input to the DFE 606. It can be said, then, that the composite

20 trellis decoder 902 operates to reliably decode the output of the FFE, even in the presence of significant phase jitter in the signal being output from the FFE.

[0030] The simulation results shown in Fig. 11 illustrate that the performance of a conventional partial trellis slicer is dominated by the maximum phase offset value, rather than by the time variation of phase offset. When the maximum offset value is less than $\pi/16$, the partial trellis slicer works well and is not very much affected by

25 phase jitter. When the maximum offset value reaches $\pi/8$, however, the performance of the partial trellis slicer is obviously degraded. When the maximum offset value reaches $\pi/4$, the performance of the partial trellis slicer is overwhelmed by the phase jitter effect, while the composite trellis decoder still works well under the same

30 condition.

What is claimed is:

1. A decision feedback equalizer configured to equalize an input signal to generate a output signal, comprising:
 - linear feed-forward filter circuitry configured to provide a linearly
5 filtered output signal based on the input signal;
 - linear or non-linear feedback filter circuitry;
 - composite trellis decoder circuitry configured to
10 process a combined signal that is based on a combination of at least the linearly feed forward filter output signal and on output of the linear or non-linear feedback filter circuitry, in accordance with state metrics generated by processing a composite trellis diagram relative to the combined signal, to provide a trellis-decoded output signal as input to the non-linear feedback circuitry; and
15 provide a particular phase output of the combined signal, based on the state metrics, as the decoded output signal.
2. The equalizer of claim 1, wherein:
 - carrier recovery circuitry is configured to offset time-dependent phase
information from the input signal prior to the input signal being provided to the linear
equalizer circuitry.
- 20 3. A method of decoding an input signal to generate a decoded output signal, comprising:
 - linearly equalizing the input signal to provide a linearly equalized output
signal based on the input signal;
 - processing a combined signal that is based on a combination of at least the
25 linearly feed-forward filtered output signal and on output of linear or non-linear feedback filter circuitry, in accordance with state metrics generated by processing a composite trellis diagram relative to the combined signal, to
provide a trellis-decoded output signal as input to the linear or non-linear feedback circuitry; and
30 provide a particular phase output of the combined signal, based on the state metrics, as the decoded output signal.
4. The method of claim 3, further comprising:
 - offsetting time-dependent phase information from the input signal prior to the
input signal being linearly equalized.

5. The method of claim 3, wherein:
the input signal is a trellis-encoded communications signal.
6. The method of claim 5, wherein:
the trellis-encoded communications signal is encoded according to a process
- 5 substantially compliant with an Advanced Television Systems Committee standard.