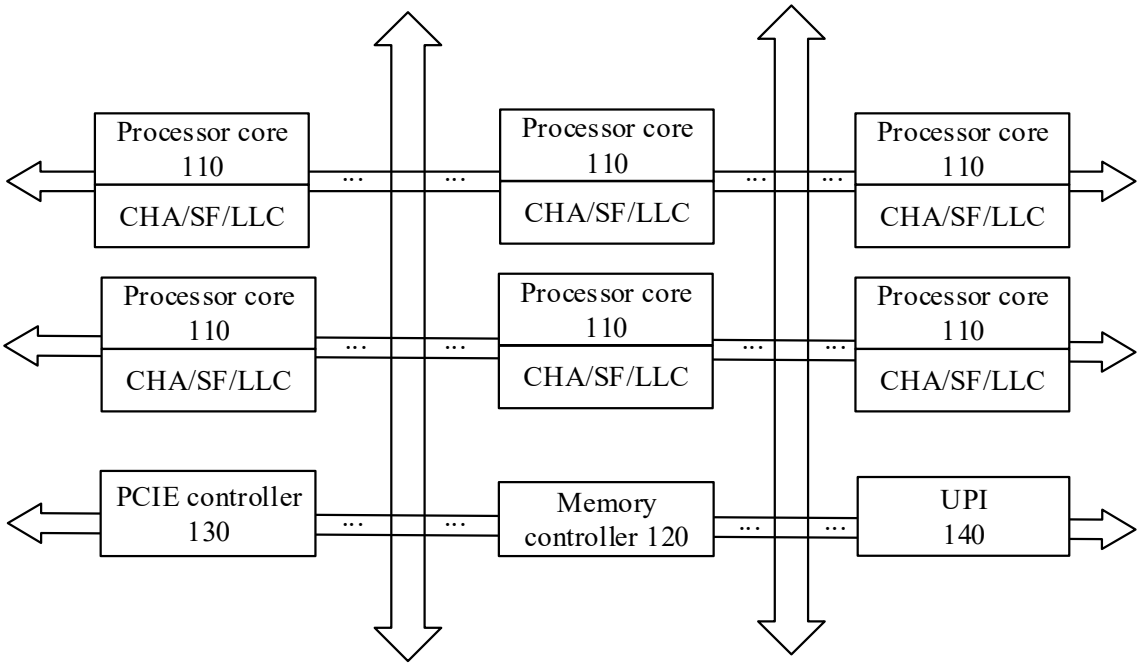



FIG. 1

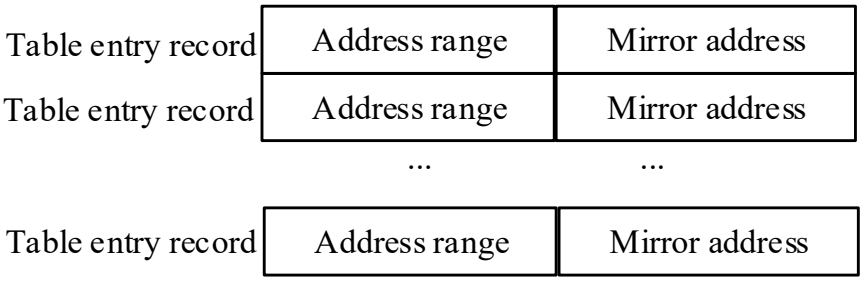



FIG. 2

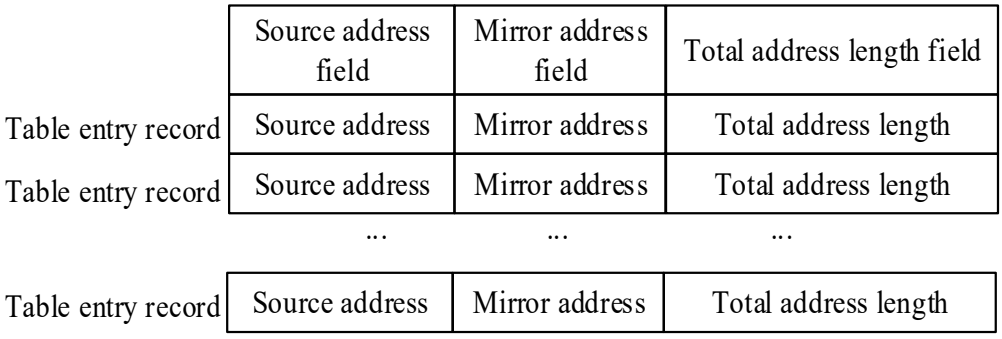



FIG. 3

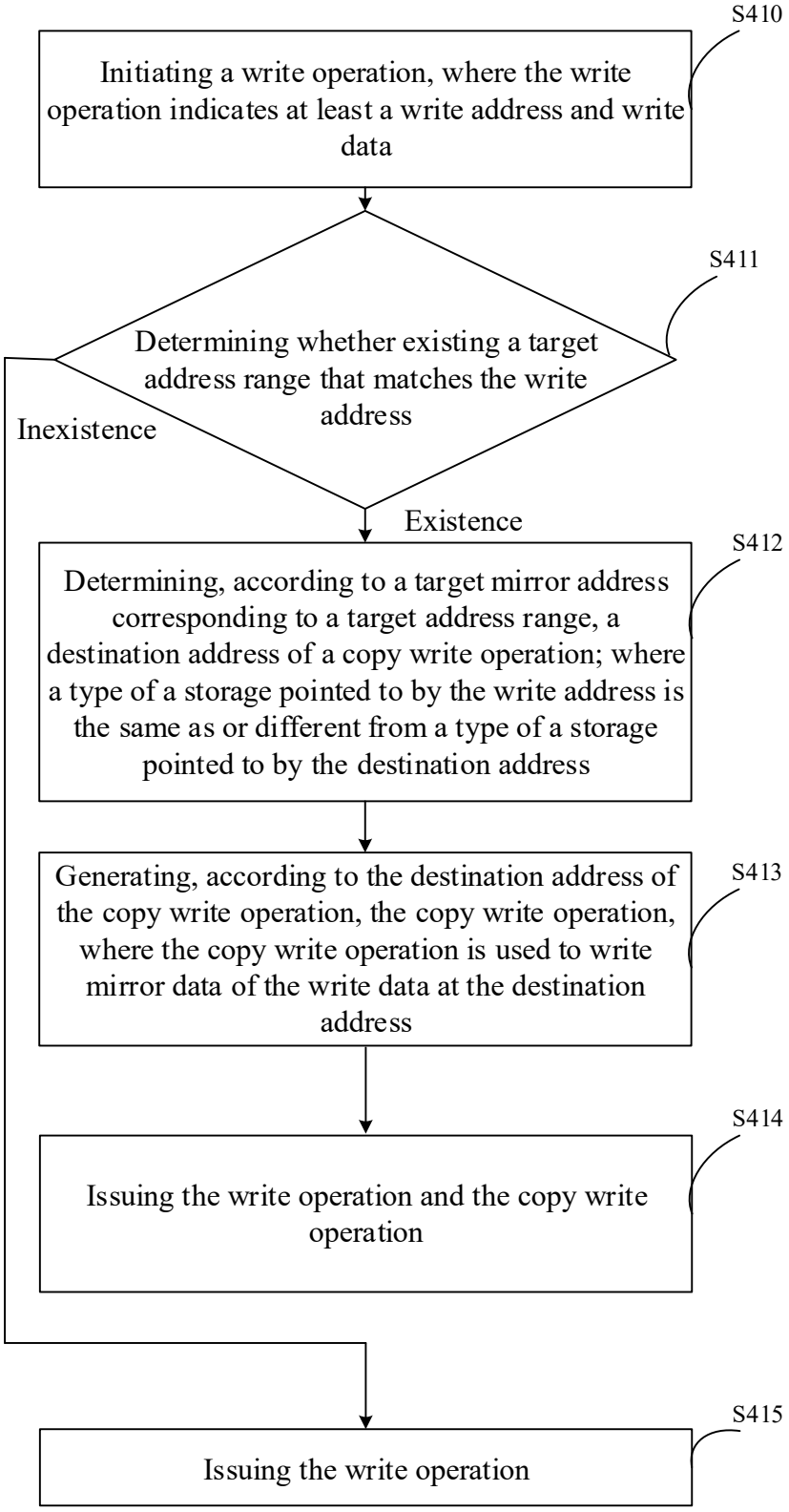

S410
Initiating a write operation, where the write operation indicates at least a write address and write data
S411
Determining whether existing a target address range that matches the write address
Inexistence
Existence
S412
Determining, according to a target mirror address corresponding to a target address range, a destination address of a copy write operation; where a type of a storage pointed to by the write address is the same as or different from a type of a storage pointed to by the destination address
S413
Generating, according to the destination address of the copy write operation, the copy write operation, where the copy write operation is used to write mirror data of the write data at the destination address
S414
Issuing the write operation and the copy write operation
S415
Issuing the write operation

FIG. 4

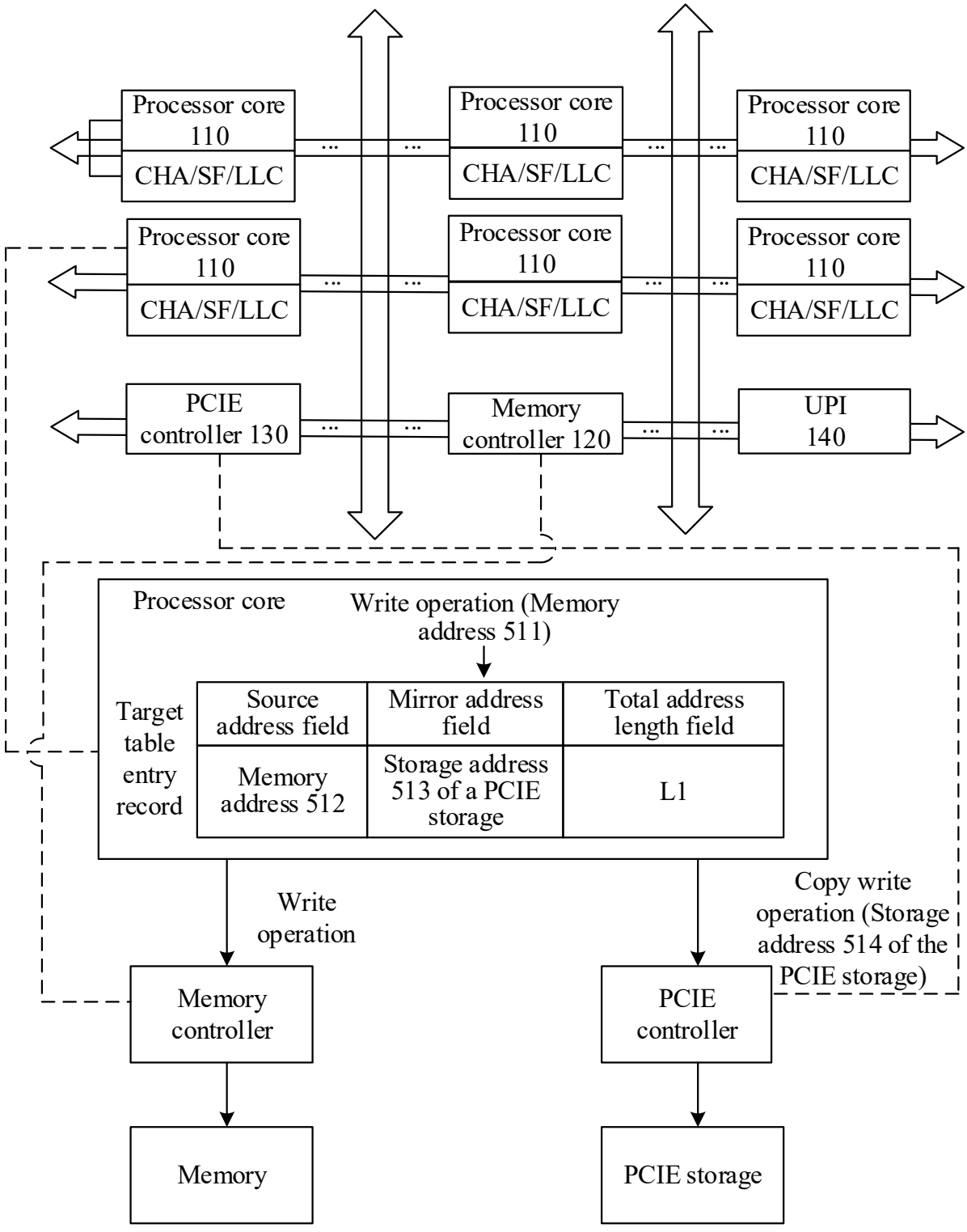

Processor core 110
CHA/SF/LLC
Processor core 110
CHA/SF/LLC
Processor core 110
CHA/SF/LLC
Processor core 110
CHA/SF/LLC
Processor core 110
CHA/SF/LLC
Processor core 110
CHA/SF/LLC
PCIE controller 130
Memory controller 120
UPI 140
Processor core
Write operation (Memory address 511)
Target table entry record
Source address field
Mirror address field
Total address length field
Memory address 512
Storage address 513 of a PCIE storage
L1
Write operation
Copy write operation (Storage address 514 of the PCIE storage)
Memory controller
PCIE controller
Memory
PCIE storage

FIG. 5A

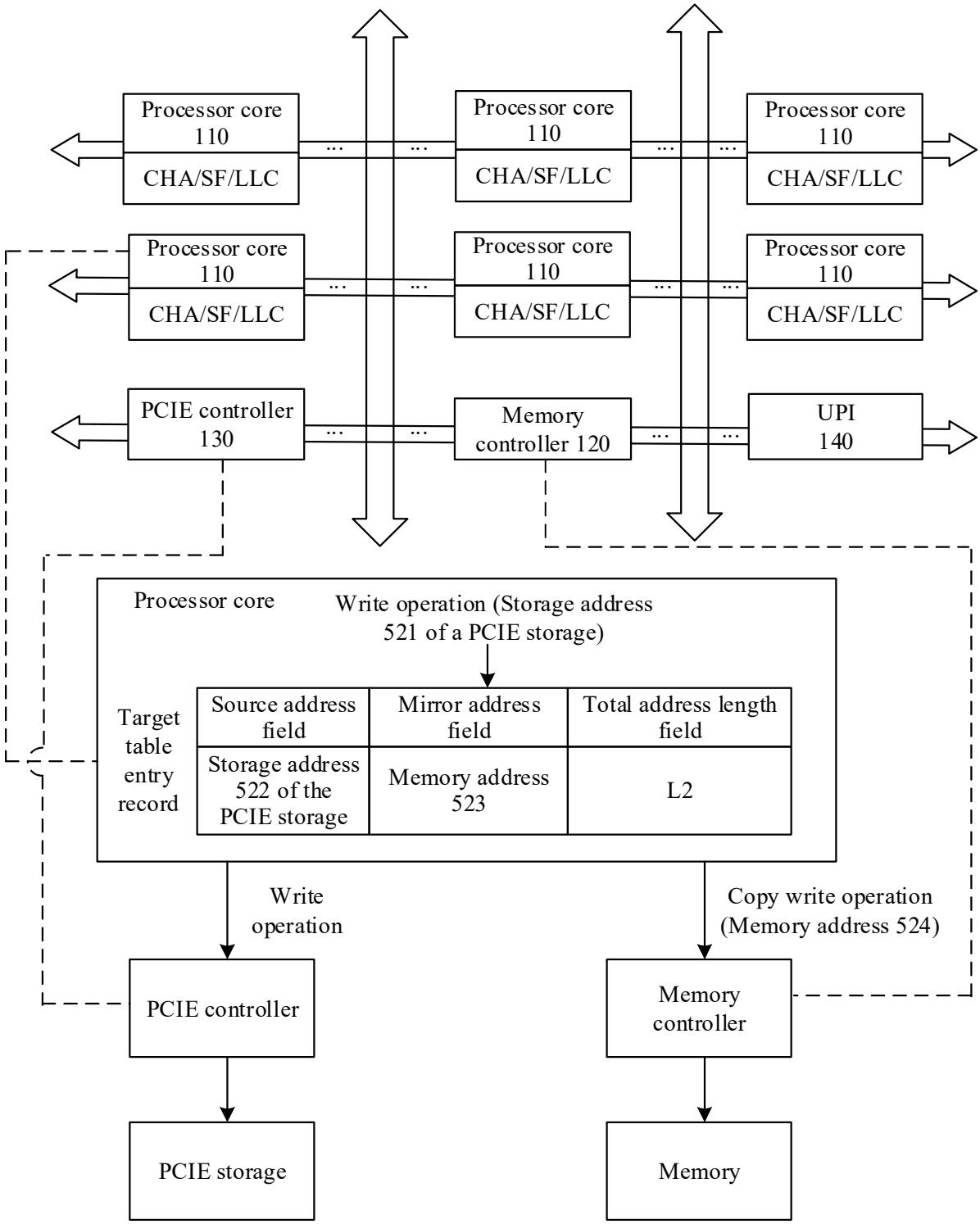

Processor core 110
CHA/SF/LLC
PCIE controller 130
Memory controller 120
UPI 140
Processor core
Write operation (Storage address 521 of a PCIE storage)
Target table entry record
Source address field
Mirror address field
Total address length field
Storage address 522 of the PCIE storage
Memory address 523
L2
Write operation
Copy write operation (Memory address 524)
PCIE controller
Memory controller
PCIE storage
Memory

FIG. 5B

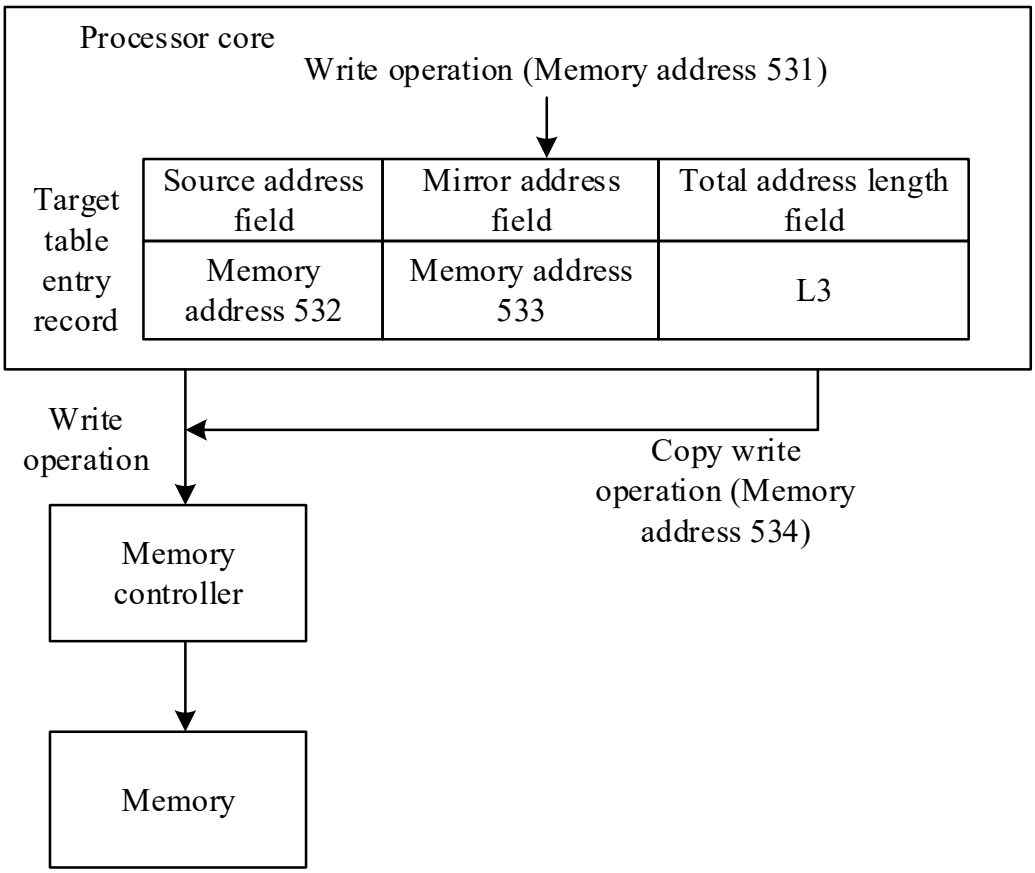

Processor core
Write operation (Memory address 531)
Target table entry record
Source address field
Mirror address field
Total address length field
Memory address 532
Memory address 533
L3
Write operation
Copy write operation (Memory address 534)
Memory controller
Memory

FIG. 5C

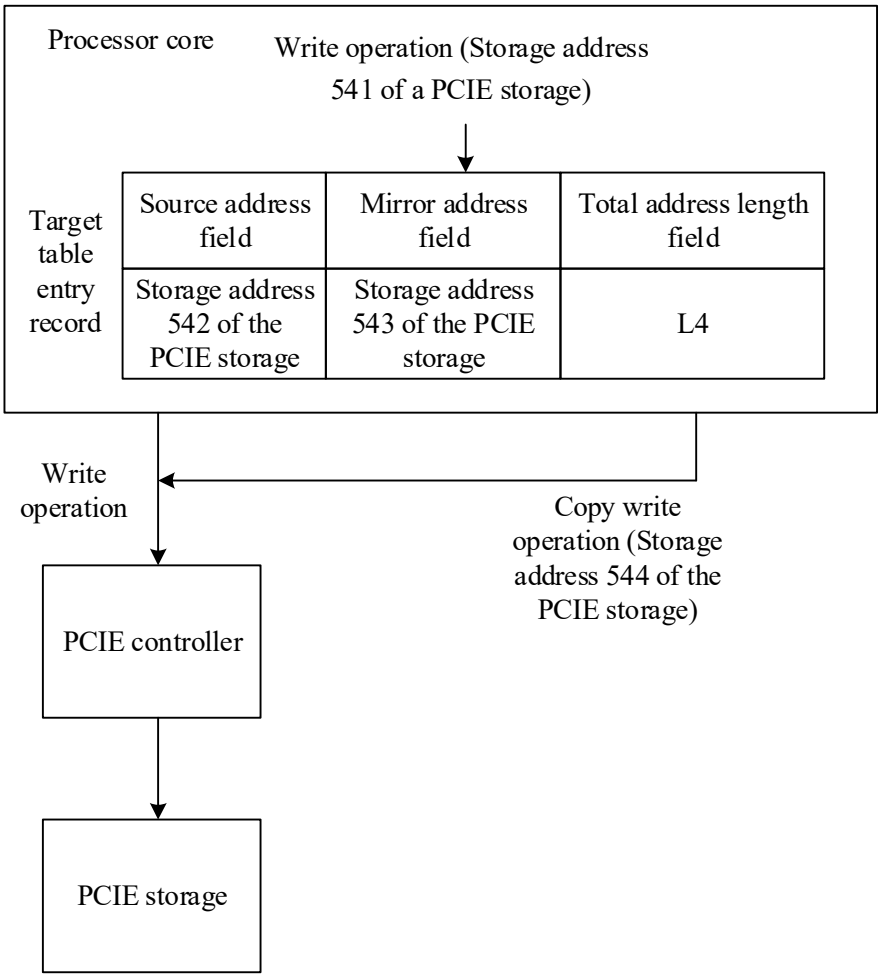

Processor core
Write operation (Storage address 541 of a PCIE storage)
Target table entry record
Source address field
Mirror address field
Total address length field
Storage address 542 of the PCIE storage
Storage address 543 of the PCIE storage
L4
Write operation
Copy write operation (Storage address 544 of the PCIE storage)
PCIE controller
PCIE storage

FIG. 5D

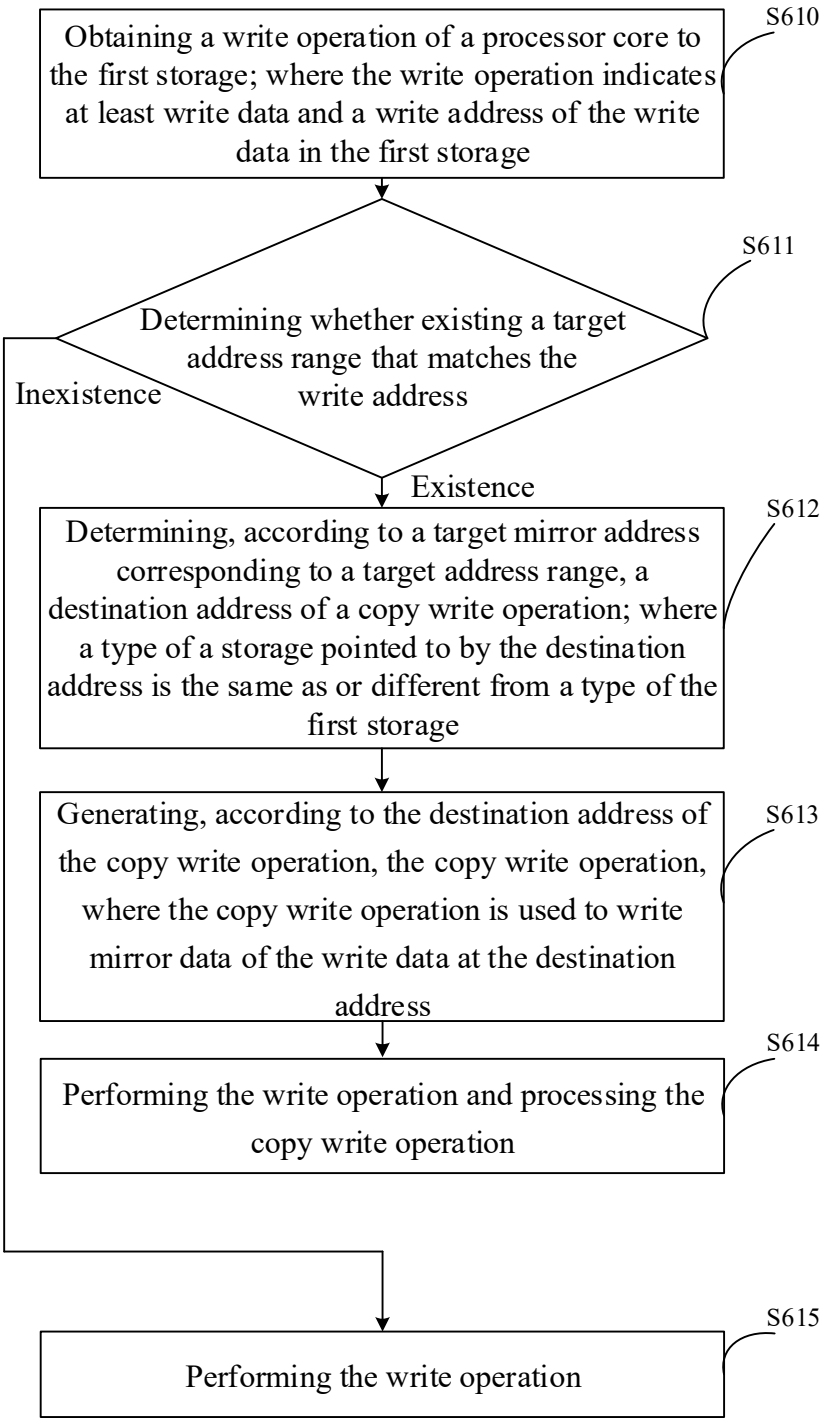

Obtaining a write operation of a processor core to the first storage; where the write operation indicates at least write data and a write address of the write data in the first storage
S610
Determining whether existing a target address range that matches the write address
S611
Inexistence
Existence
Determining, according to a target mirror address corresponding to a target address range, a destination address of a copy write operation; where a type of a storage pointed to by the destination address is the same as or different from a type of the first storage
S612
Generating, according to the destination address of the copy write operation, the copy write operation, where the copy write operation is used to write mirror data of the write data at the destination address
S613
Performing the write operation and processing the copy write operation
S614
Performing the write operation
S615

FIG. 6

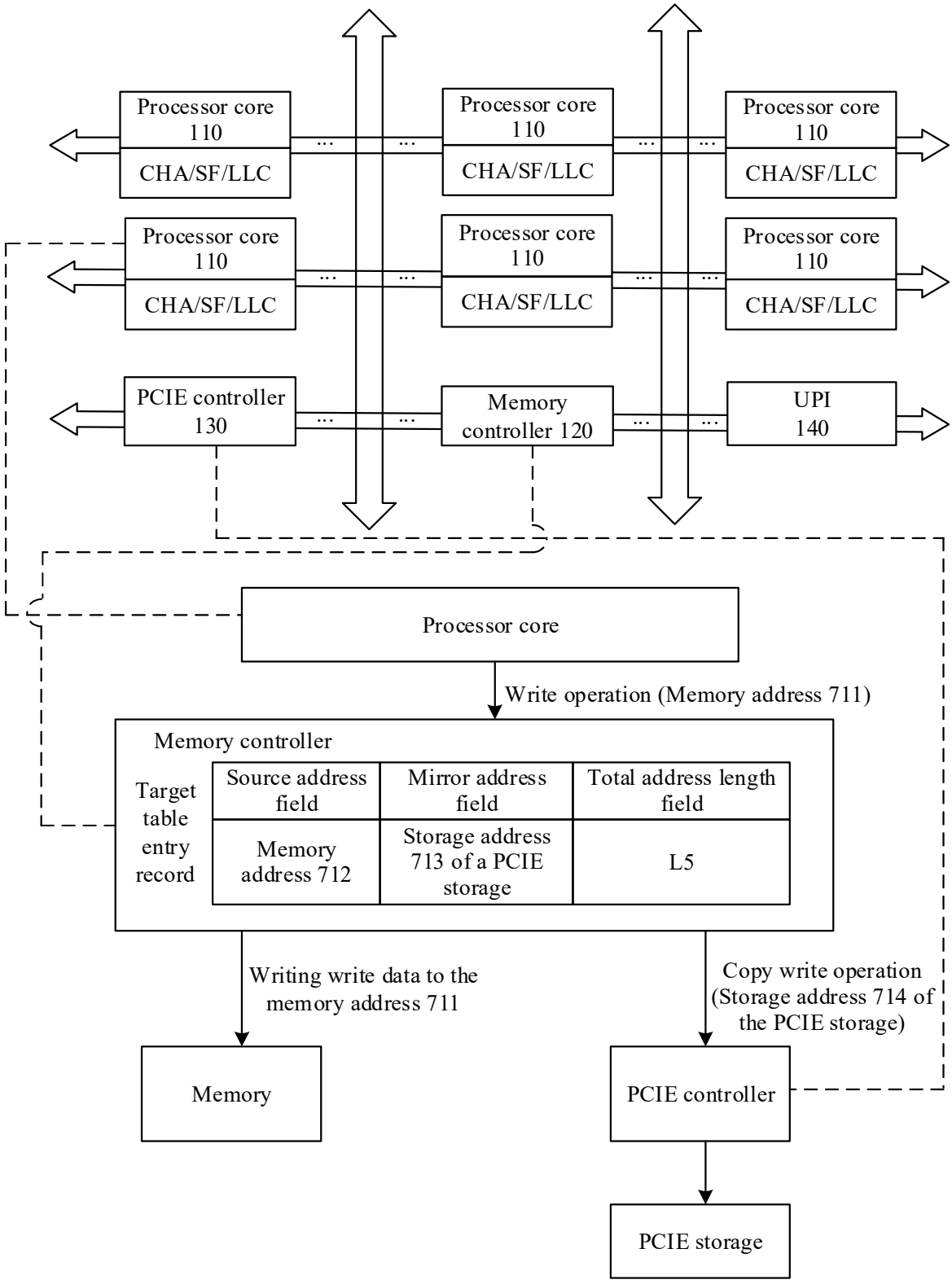

Processor core 110
CHA/SF/LLC
Processor core 110
CHA/SF/LLC
Processor core 110
CHA/SF/LLC
Processor core 110
CHA/SF/LLC
Processor core 110
CHA/SF/LLC
Processor core 110
CHA/SF/LLC
PCIE controller 130
Memory controller 120
UPI 140
Processor core
Write operation (Memory address 711)
Memory controller
Target table entry record
Source address field
Mirror address field
Total address length field
Memory address 712
Storage address 713 of a PCIE storage
L5
Writing write data to the memory address 711
Copy write operation (Storage address 714 of the PCIE storage)
Memory
PCIE controller
PCIE storage

FIG. 7

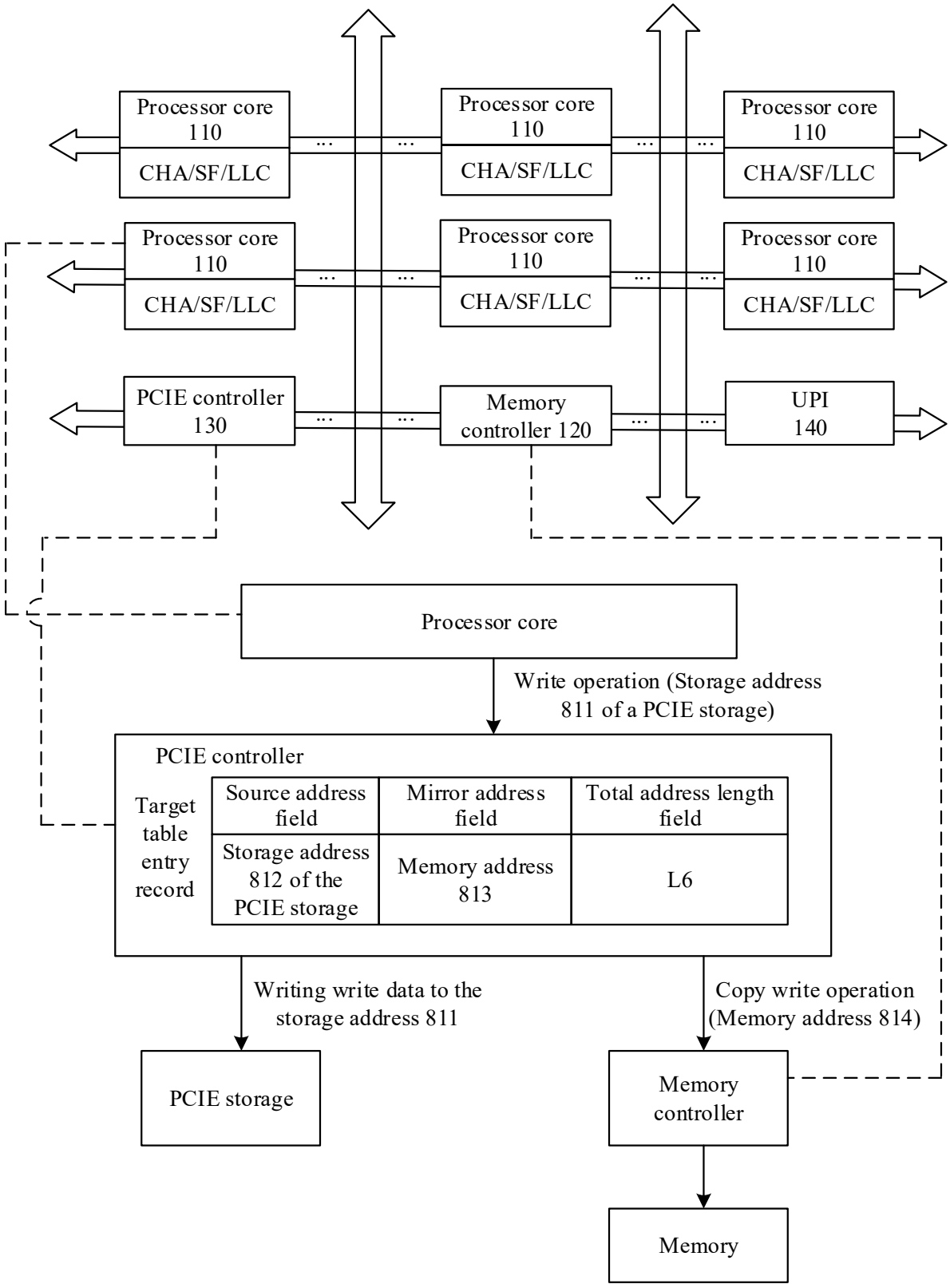

Processor core 110
CHA/SF/LLC
Processor core 110
CHA/SF/LLC
Processor core 110
CHA/SF/LLC
Processor core 110
CHA/SF/LLC
Processor core 110
CHA/SF/LLC
Processor core 110
CHA/SF/LLC
PCIE controller 130
Memory controller 120
UPI 140
Processor core
Write operation (Storage address 811 of a PCIE storage)
PCIE controller
Target table entry record
Source address field
Mirror address field
Total address length field
Storage address 812 of the PCIE storage
Memory address 813
L6
Writing write data to the storage address 811
Copy write operation (Memory address 814)
PCIE storage
Memory controller
Memory

FIG. 8