WHAT IS CLAIMED IS:

1. A finFET transistor, comprising:

a substrate having a fin extending from the substrate;

a gate structure formed on the fin, wherein the gate structure includes:

a first portion and a second portion, wherein the first and second portions each have a first edge and an opposing second edge, and wherein the first edges are substantially collinear and the second edges are substantially collinear; and

an offset portion interposing the first portion and the second portion, the offset portion having a third edge and a fourth edge, wherein the third edge and the fourth edge are non-collinear with the first and second edges of the first and second portions of the gate structure, and wherein the third edge and the fourth edge are offset a first distance in a first direction from the first edges and second edges respectively; and

a contact element connected to the offset portion of the gate structure.

2. The finFET transistor of claim 1, wherein the offset portion directly overlies the fin.

3. The finFET transistor of claim 1, wherein the first portion includes a sidewall, and wherein the first portion sidewall interfaces a lateral sidewall of the fin.

4. The finFET transistor of claim 1, wherein the gate structure includes a metal gate electrode.

5. The finFET transistor of claim 1, wherein the contact element is a conductive feature that lands directly on a top surface of the offset portion.

6. The finFET transistor of claim 1, wherein the gate structure includes a high-k dielectric layer and an overlying metal gate electrode.

7. A semiconductor device, comprising:

a first gate structure formed on a semiconductor substrate, wherein the gate structure has a first side and an opposing second side and includes:

a first portion and a second portion, wherein the first and second portions each have a first edge defining the first side of the gate structure and

an opposing second edge defining the second side of the gate structure; and wherein the first edges are substantially collinear and the second edges are substantially collinear; and

an offset portion contiguous with the first and second portions and interposing the first portion and the second portion, the offset portion having a third edge defining the first side of the gate structure and a fourth edge defining the second side of the gate structure, wherein the third edge is non-collinear with respective on of the first edges of the first and second portions of the gate structure; and

a second gate structure on the semiconductor substrate, wherein the second gate structure has substantially collinear sidewalls extending from a first end to an opposing second end of the second gate structure.

8. The semiconductor device of claim 7, wherein the gate structure includes a metal gate electrode.

9. The semiconductor device of claim 7, further comprising:

a contact element landing on a top surface of the offset portion of the gate structure.

10. The semiconductor device of claim 7, wherein the gate structure interfaces a single, planar surface of the semiconductor substrate.

11. The semiconductor device of claim 7,

wherein the second gate structure on the semiconductor substrate is the next adjacent gate structure to the first gate structure.

12. The semiconductor device of claim 7, wherein the gate structure interfaces a fin of a fin-type field effect transistor (FET).

13. The semiconductor device of claim 12, wherein the offset portion directly overlies the fin.

14. The semiconductor device of claim 12, wherein the third edge of the offset portion is offset from the first edge of the first portion by a distance of less than approximately 10 nanometer.

15. The semiconductor device of claim 12, wherein a width of the offset portion is

substantially equal to the width of the first portion, wherein the width of the offset portion is defined as a distance between the third and fourth edge of the offset portion.

16. A semiconductor device, comprising:

a first gate structure including a gate dielectric layer and a metal gate electrode, wherein the gate structure has a first side and an opposing second side and includes:

a first portion and a second portion, wherein the first and second portions each have a first edge defining the first side and an opposing second edge defining the second side, and wherein the first edges are substantially collinear and the second edges are substantially collinear; and

an offset portion interposing the first portion and the second portion, the offset portion, the offset portion having a third edge defining the first side and a fourth edge defining the second side, wherein the third edge is spaced a first distance from the first edges and the fourth edge is spaced the first distance from the second edges, wherein the first distance is in a direction perpendicular to the first edge; and wherein a width of the offset portion is substantially equal to the width of each of the first portion and the second portion; and

a contact element disposed over the offset portion of the gate structure.

17. The semiconductor device of claim 16, further comprising:

a second gate structure having a contiguous, collinear edge extending the distance of the first portion, second portion and offset portion of the first gate structure.

18. The semiconductor device of claim 16, wherein the offset portion is vertically aligned with a fin element disposed under the gate structure.

19. The semiconductor device of claim 18, wherein the first portion is disposed to a first side of the fin element and the second portion is disposed to a second, opposing side of the fin element.

20. The semiconductor device of claim 16, wherein the first distance is less than approximately 10 nanometers.