

ABSTRACT OF THE DISCLOSURE

A memory device includes a memory cell array, signal lines, a mode selector circuit, a command converter circuit, and an internal processor. The memory cell array
5 includes first and second memory regions. The mode selector circuit is configured to generate a processing mode selection signal for controlling the memory device to enter an internal processing mode based on the address received together with the command. The command converter circuit is configured to convert the received command into an internal processing operation command in response to activation of the processing mode selection
10 signal. The internal processor is configured to perform an internal processing operation on the first memory region in response to the internal processing operation command, in the internal processing mode.

FIG. 1