

What is claimed is:

1. An image processing device comprising:
a multimedia intellectual property (IP) block configured to process image data including a first component and a second component;
5 a memory; and
a frame buffer compressor (FBC) configured to compress the image data to generate compressed data and store the compressed data in the memory,
wherein the frame buffer compressor includes a logic circuit configured to control a compression sequence of the first component and the second component of the image data,
10 wherein the logic circuit:
calculates a total target bit and a chroma component target bit of the chroma component based on a target compression ratio of the image data,
assigns the chroma component target bit to compress the chroma component,
calculates a luma component target bit of the luma component, using a chroma
15 component used bit of the compressed data for the chroma component, and
assigns the luma component target bit to compress the luma component,
and wherein the chroma component used bit is smaller than the chroma component target bit.

20 2. The image processing device of claim 1, wherein after compressing the first component and the second component in accordance with the compression sequence determined by the logic circuit, the frame buffer compressor merges the compressed data of the first component and the compressed data of the second compressed data to generate a single bit stream.

25 3. The image processing device of claim 2, wherein the frame buffer compressor merges the compressed data of the first component and the compressed data of the second component in an arbitrary sequence different from the compression sequence of the first component and the second component to generate the single bit stream.

30 4. The image processing device of claim 2 or claim 3, wherein the frame buffer compressor interleaves and merges the compressed data of the first component and the compressed data of the second component to generate the single bit stream.

5. The image processing device of any one of claims 1 to 4, wherein the image data is image data conforming to a YUV format,

the first component includes a luma component including a Y component in the YUV format, and

the second component includes a chroma component including Cb and Cr components in the YUV format.

6. The image processing device of claim 5, wherein the logic circuit controls the compression sequence so that the frame buffer compressor first compresses the chroma component first and then compresses the luma component.

7. The image processing device of claim 6, wherein, when the image data conforms to the YUV 420 format, the chroma component target bit is set to the $(\text{total target bit} / 3) \times W$, where W is a positive real number ≤ 1 .

8. The image processing device of claim 6 or claim 7, wherein, when the image data conforms to the YUV 422 format, the chroma component target bit is set to the $(\text{total target bit} / 2) \times W$, where W is a positive real number ≤ 1 .

9. The image processing device of any one of claims 6 to 8, wherein the luma component target bit is calculated by subtracting the chroma component used bit from the total target bit.

10. An image processing device comprising:
a multimedia intellectual property (IP) block configured to process image data conforming to a YUV format;

a memory; and

a frame buffer compressor (FBC) configured to compress the image data to generate compressed data and store the compressed data in the memory,

wherein the frame buffer compressor includes a logic circuit configured to control a compression sequence such that compression of a chroma component including Cb and Cr

components of the YUV format of the image data is executed prior to compression of a luma component including Y component of the YUV format of the image data,

wherein the logic circuit:

calculates a total target bit and a chroma component target bit of the chroma component

5 based on a target compression ratio of the image data,

assigns the chroma component target bit to compress the chroma component,

calculates a luma component target bit of the luma component, using a chroma component used bit of the compressed data for the chroma component, and

assigns the luma component target bit to compress the luma component,

10 and wherein the chroma component used bit is smaller than the chroma component target bit.

11. The image processing device of claim 10, wherein the logic circuit determines a quantization parameter (QP) value and an entropy k encoding value so that the chroma component used bit is a value smaller than and closest to the chroma component target bit.

12. The image processing device of claim 10 or claim 11, wherein, when the image data conforms to the YUV 420 format, the chroma component target bit is set to the $(\text{total target bit} / 3) \times W$, where W is a positive real number ≤ 1 .

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13. The image processing device of any one of claims 10 to 12, wherein, when the image data conforms to the YUV 422 format, the chroma component target bit is set to the $(\text{total target bit} / 2) \times W$, where W is a positive real number ≤ 1 .

14. The image processing device of any one of claims 10 to 13, wherein the luma component target bit is calculated by subtracting the chroma component used bit from the total target bit.

15. The image processing device of any one of claims 10 to 14, wherein, when a sum of the luma component used bit of the compressed data of the luma component and the chroma component used bit is less than the total target bit, the logic circuit adds a dummy bit after the compressed data of the luma component.

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16. A method for operating an image processing device, the method comprising:
calculating a total target bit based on a target compression ratio of image data
conforming to a YUV format;

5 calculating a chroma component target bit for compressing a chroma component
including Cb and Cr components of the YUV format;

assigning the chroma component target bit to compress the chroma component;

calculating the luma component target bit of the luma component including a Y
component of the YUV format, using the chroma component used bit of the compressed data
for the chroma component;

10 assigning the luma component target bit to compress the luma component; and

adding a dummy bit after the compressed data of the luma component, when the sum
of the luma component used bit of the compressed data of the luma component and the chroma
component used bit is less than the total target bit,

15 wherein the chroma component used bit is smaller than the chroma component target
bit.