WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate;

first, second, third and fourth bottom contacts in the substrate;

first, second, third and fourth active fins on respective ones of the first, second, third and fourth bottom contacts, each of the second and third active fins extending longitudinally in a first direction, the second and third active fins aligned in the first direction;

first, second and third gate electrodes extending longitudinally in the first direction, the first and second gate electrodes disposed on side surfaces of respective ones of the first and fourth active fins and the third gate electrode disposed on side surfaces of each of the second and third active fins;

a first top contact on the first and second active fins; and

a second top contact on the third and fourth active fins.

2. The semiconductor device of claim 1, wherein the first and second bottom contacts are aligned in a second direction and are spaced apart from each other in the second direction, wherein the third and fourth bottom contacts are aligned in the second direction and are spaced apart from each other in the second direction, wherein the first and second bottom contacts are spaced apart from the third and fourth bottom contacts in the first direction, wherein the second and third bottom contacts overlap in the first direction, and wherein the first and fourth bottom contacts do not overlap in the first direction.

3. The semiconductor device of claim 1 or claim 2, further comprising first, second, third and fourth source/drain regions between the first, second, third and fourth bottom contacts and the first, second, third and fourth active fins, respectively.

4. The semiconductor device of any one of claims 1 to 3, further comprising first, second, third and fourth source/drain regions between the first and second top contacts and the first, second, third and fourth active fins.

5. The semiconductor device of claim 4, wherein the first and second source/drain regions are connected by the first top contact and wherein the third and fourth source/drain regions are connected by the second top contact.

6. The semiconductor device of any one of claims 1 to 5, wherein the first and second active fins have n-type conductivity and wherein the third and fourth active fins have p-type conductivity.

7. The semiconductor device of any one of claims 1 to 6, further comprising a first dummy gate electrode extending longitudinally in the first direction between the first and second gate electrodes.

8. The semiconductor device of claim 7, further comprising a second dummy gate electrode extending longitudinally in the first direction between the third and fourth gate electrodes.

9. A semiconductor device comprising:

first, second, third, fourth and fifth gate electrodes extending longitudinally in a first direction and spaced apart in a second direction;

first and second active fins surrounded by the first gate electrode and spaced apart in the first direction;

a third active fin surrounded by the second gate electrode;

fourth and fifth active fins surrounded by the third gate electrode and spaced apart in the first direction;

a sixth active fin surrounded by the fourth gate electrode;

seventh and eighth active fins surrounded by the fifth gate electrode and spaced apart in the first direction;

a first top contact connecting the third and fourth active fins; and

a second top contact connecting the fifth and sixth active fins.

10. The semiconductor device of claim 9, further comprising first and second power contacts extending longitudinally in the second direction and disposed on respective first and second sides of the first, second, third, fourth and fifth gate electrodes such that the first, second, third, fourth and fifth gate electrodes are located between the first and second power contacts.

11. The semiconductor device of claim 10, further comprising:

a third top contact connecting the first active fin and the first power contact;

a fourth top contact connecting the second active fin and the second power contact;

a fifth top contact connecting the seventh active fin and the first power contact; and

a sixth top contact connecting the eighth active fin and the second power contact.

12. The semiconductor device of claim 11, wherein at least one of the first, second, third, fourth and fifth gate electrodes comprises:

a first sub-gate electrode extending longitudinally in the first direction;

a second sub-gate electrode extending longitudinally in the first direction and is spaced apart from the first sub-gate electrode in the second direction; and

a connecting portion extending longitudinally in the second direction and connects the first and second sub-gate electrodes.

13. The semiconductor device of claim 12, wherein the connecting portion does not overlap the first and second top contacts in the second direction.

14. The semiconductor device of any one of claims 9 to 13, further comprising a first dummy gate electrode extending longitudinally in the first direction between the third and fourth gate electrodes.

15. The semiconductor device of claim 14, wherein the first and second top contacts are on the first dummy gate electrode.

16. The semiconductor device of claim 14 or claim 15, further comprising a third top contact connecting the first and second top contacts and disposed on the first dummy gate electrode, wherein the first, second and third top contacts are integrated in a single member.

17. The semiconductor device of any one of claims 14 to 16, further comprising a second dummy gate electrode extending longitudinally in the first direction between the second and third gate electrodes.

18. The semiconductor device of any one of claims 9 to 17, wherein at least one of the first, second, third, fourth and fifth gate electrodes has a first width in the second direction, wherein other ones of the first, second, third, fourth and fifth gate electrodes have a second width in the second direction, and wherein the first width is greater than *n* times the second width, where *n* is an integer equal to or greater than 2.

19. The semiconductor device of claim 18, wherein, for the group of the first, second, third, fourth, fifth, sixth, seventh and eighth active fins, a number of active fins surrounded by a gate electrode having the first width among the first, second, third, fourth and fifth gate electrodes is *n*.

20. A semiconductor device comprising:

first, second, third and fourth active fins on a substrate, each of the second and third active fins extending longitudinally in a first direction, the second and third active fins aligned in a first direction;

a first gate electrode extending longitudinally in the first direction and on side surfaces of the first active fin;

a second gate electrode extending longitudinally in the first direction and on side surfaces of each of the second and third active fins;

a third gate electrode extending longitudinally in the first direction and on side surfaces of the fourth active fin;

a first top contact on the first and second active fins and electrically connecting the first and second active fins; and

a second top contact on the third and fourth active fins and electrically connecting the third and fourth active fins,

wherein the first gate electrode and the first active fin are components of a first transistor, wherein the second gate electrode and the second active fin are components of a second transistor, wherein the second gate electrode and the third active fin are components of third transistor, wherein the third gate electrode and the fourth active fin are components of a fourth transistor, wherein drain nodes of the first and second transistors are electrically connected by the first top contact, and wherein drain nodes of the third and fourth transistors are electrically connected by the second top contact.