

CIRCUIT FOR SEPARATING CHROMINANCE SIGNALS FROM A
COMPOSITE VIDEO SIGNAL

5 The present invention relates to a circuit for separating chrominance signals from a composite video signal in a colour video processing system.

10 Generally, in the case of NTSC broadcasting systems, technologies for separating the luminance signal Y and the chrominance signal C from a composite video signal have been proposed in various ways.

15 Standard colour television systems transmit the luminance signal and the chrominance signal separately, and provide luminance signals (Y) that are in phase from horizontal scan line to horizontal scan line and chrominance signals that are 180 degrees out of phase on adjacent horizontal scan lines. At the video level, a composite video signal is established that is Y+C for one
20 horizontal scan line and Y-C for the next horizontal scan line. These sum and difference video signals are utilized to separate the luminance video signal from the chrominance video signal.

25 In a motion picture, Y/C separation is usually carried out by using the characteristics between scan lines, and in a still picture, Y/C separation is usually carried out by using a frame memory.

30 The principles of Y/C separation between scan lines which have been realized up to now in a motion picture will be described below with reference to Figures 4 to 7, in which:

Figure 4 is an illustrated block diagram for explaining luminance and chrominance separation between lines;

5 Figures 5 and 7 are sketches showing an arrangement of scanning lines in a display; and

Figure 6 is a block diagram of an adaptive 2H comb filter utilised in the prior art for separating luminance and chrominance signals from a composite video signal.
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The luminance and chrominance signals information of two scan lines of Figure 5 of the accompanying diagrammatic drawings, for example, rely on the contents of the present picture. However between the content of the i-th line and that of the i+1-th line in a motion picture, the information of the luminance and chrominance signals may be similar.
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If the composite video signal, the luminance and the chrominance signals situated at Δt from a reference point of the i-th line are designated as V_i , Y_i and C_i , respectively and the corresponding signals in the i+1-th line are designated as V_{i+1} , Y_{i+1} and C_{i+1} , respectively,
20
the following equations can be made:
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In the i-th line:

$$\begin{aligned} V_i(t + \Delta t) &= Y_i(t + \Delta t) + C_i(t + \Delta t) \\ &= Y_i(t + \Delta t) + E(R - Y)^1 \\ &\quad \cos 2\pi f_{sc}(t + \Delta t) + E(B - Y)^1 \\ &\quad \sin 2\pi f_{sc}(t + \Delta t) \dots \dots \dots (1) \end{aligned}$$

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In the i+1-th line:

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$$\begin{aligned} V_{i+1}(t + \Delta t + 1/F_h) &= Y_{i+1}(t + \Delta t + 1/F_h) \\ &+ E(R - Y)^1 \cos 2\pi f_{sc}(t + \Delta t_d + 1/F_h) \\ &+ Y(B - Y)^1 \sin 2\pi f_{sc}(t + \Delta t_d + 1/f_h) \quad \dots \quad (2) \end{aligned}$$

5 Substituting $f_{sc} = (425/2)F_h$ into equation (2) yields

$$\begin{aligned} &Y_{i+1}(t + \Delta t + 1/F_h) \\ &\quad + E(R - Y)^1 \cos 2\pi f_{sc}(t + \Delta t + 425/2f_{sc}) \\ &\quad + Y(B - Y)^1 \sin 2\pi f_{sc}(t + \Delta t + 425/2f_{sc}) \\ 10 \quad &= Y_i + 1(t + \Delta t + 1/F_h) - E(R - Y)^1 \cos 2\pi f_{sc}(t + \Delta t) \\ &\quad + E(B - Y)^1 \sin 2\pi f_{sc}(t + \Delta t_d) \quad \dots \quad (3) \end{aligned}$$

15 Therefore, from equations (1) and (3) we can obtain the following relationships.

$$\begin{aligned} V_i(t + \Delta t) &= Y_i(t + \Delta t) + C_i(t + \Delta t) \\ V_{i+1}(t + \Delta t) &= Y_{i+1}(t + \Delta t) - C_i(t + \Delta t) \end{aligned}$$

20 Thus, if Y_i and Y_{i+1} are similar and the chrominance information is similar between two adjacent scan lines, Y/C separation can be carried out by adding and subtracting $Y+C$, and $Y-C$ as shown in Figure 4 of the accompanying diagrammatic drawings.

25 Next, referring to Figure 6 of the accompanying diagrammatic drawings, an adaptive 2H comb filtering method which is better than the above-mentioned Y/C separation method will be described below.

30 When the number of scan lines is 3, as shown in Figure 7 of the accompanying diagrammatic drawings, Y/C separation of line (5) separates Y/C separation adaptively by detecting the correlation between upper and lower
35 lines. That is, the difference between line (5) and line

(4), and between line (5) and line (6) in Figure 6 is $\Delta Y_L + \Delta Y_H + 2C$, in each case. Here, ΔY_L is a luminance low pass component, ΔY_H is a luminance high pass component and C is the chrominance signal.

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In the circuit of Figure 6, the video composite signal CV (line 6) is input to a delay circuit D3, which delays the signal by one horizontal scanning period (1H). The delayed output of the delay circuit D3 is fed to another similar delay circuit D4, which outputs a further 1H delayed signal. Thus, at the instant where the video composite signal is at line 6, as shown in Figures 6 and 7, the delay circuit D3 outputs line 5, and the following delay circuit D4 outputs line 4.

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The output of the delay circuit D3 is fed to subtractors 50 and 51, which respectively subtract from it the composite video signal CV in subtractor 50, and the 2H delayed signal from the delay circuit D4 in subtractor 51. The outputs of the subtractors 50 and 51 provide the respective difference signals $\Delta Y_L + \Delta Y_H + 2C$ referred to above.

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If the $\Delta Y_L + \Delta Y_H + 2C$ signals pass through low pass filters LPF₃ and LPF₄, ΔY_L is obtained in each case, so that a correlation based on the value of ΔY_L may be obtained. This means that the smaller is the difference component, the larger is the correlation, and therefore the chrominance signal C is taken by the difference component between the lines with the smaller difference components. Here, the luminance low pass correlation is small and the chrominance signal correlation is not detected, because the detected ΔY_L contains only the low pass luminance component.

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Further, when there exists no correlation, various defects can be caused by carrying out Y/C separation between lines.

5 Preferred embodiments of the present invention aim to provide a circuit for separating from a line the chrominance signal of a video signal, with correlation, by detecting correlation of the chrominance signal as well as the correlation of the luminance signal. Another aim is
10 to provide a separating circuit which output a band pass filtered signal when there is no correlation of the signal between lines.

According to the present invention, there is provided
15 a circuit for separating chrominance signals from a composite video signal in a NTSC colour video signal processing system, the circuit comprising:

a first delay device for 1H delaying a composite
20 video signal;

a first band pass filter for band pass filtering the output of said first delay device;

25 a second delay device for 1H delaying the output of said first delay device;

a first subtractor for subtracting said composite video signal from the output of said first delay device;
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a first adder for adding the output of said first delay device to said composite video signal;

a second adder for adding the outputs of said first and second delay devices;

5 a second subtractor for subtracting the output of said second delay device from that of said first delay device;

10 first and second low pass filters for low pass filtering the outputs of said first and second subtractors respectively and outputting respective luminance difference signal components;

15 second and third band pass filters for filtering at a predetermined band the outputs of said first and second adders respectively, and outputting respective chrominance difference signal components;

20 a correlation detector for detecting correlation between the outputs of said first and second low pass and second and third band pass filters and generating first to fourth correlation control signals;

25 a coefficient generator for logically combining said first to fourth correlation control signals and generating a correlation detecting coefficient;

30 a multiplexer for receiving the output signal of said first band pass filter and the output signals of said first and second subtractors, and outputting one of the received signals selectively in dependence upon the value of said correlation detection coefficient.

35 Preferably, said correlation detector comprises a first comparator for comparing the outputs of said first and second low pass filters;

a second multiplexer for outputting the outputs of said two low pass filters selectively under control of said first comparator;

5 a first comparator for comparing a predetermined first reference value with the output of said second multiplexer;

10 a first OR gate for logically summing the outputs of said first and second comparators, and outputting a first correlation control signal;

15 a first inverter for inverting the output of said first comparator;

a second OR gate for logically summing the output of said first inverter and the output of said second comparator and outputting a second correlation control signal;

20 a third comparator for comparing the output of said second and third band pass filters;

25 a third multiplexer for outputting the output of said second and third band pass filters selectively under control of the output of said third comparator;

30 a fourth comparator for comparing a predetermined second reference value with the output of said third multiplexer;

a third OR gate for logically summing the output of said third and fourth comparators and outputting a third correlation control signal;

a second inverter for inverting the output of said third comparator; and

5 a fourth OR gate for logically summing the output of said second inverter and the output of said fourth comparator and outputting a fourth correlation control signal.

10 The invention extends also to a colour video signal processing system provided with a circuit as above, in accordance with the invention, and to a colour television or video recorder provided with such a signal processing system.

15 For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to Figures 1 to 3 of the accompanying diagrammatic drawings, in which:

20 Figure 1 is a schematic block diagram of one example of a circuit for separating luminance and chrominance signals from a composite video signal in an embodiment of the present invention;

25 Figure 2 is a detailed circuit diagram showing a correlation detector of Figure 1; and

Figure 3 is a detailed circuit diagram showing a coefficient generator of Figure 1.

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In the circuit for separating chrominance signals from a composite video signal, as shown in Figure 1, the composite video signal CV is delayed by a first delay device D1 for a time interval (1H) equal to the time
35 required to complete one horizontal scan line. This

delayed signal is delayed again by a second delay device D2 for another 1H time interval. A first subtractor 10 subtracts the composite video signal CV from the output of the first delay device D1. A first adder 20 adds the output of the first delay device D1 to the composite video signal CV. A second adder 30 adds the first delayed output and the second delayed output. A subtractor 40 subtracts the second delayed output from the first delayed output.

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First and second low pass filters LPF1 and LPF2 are arranged to low pass filter the outputs of the first and second subtractors 10 and 40 and output respective luminance components ΔY_L as A and D. Second and third band pass filters BPF2 and BPF3 are arranged to filter the outputs of the first and second adders 20 and 30 respectively at a predetermined bandwidth, and output respective chrominance components ΔC as B and C. A correlation detector 60 detects correlation between the outputs A, B, C and D of the four filters LPF1, BPF2, BPF3 and LPF2 and outputs four correlation control signals, W, X, Y and Z to a coefficient generator 70. The coefficient generator 70 combines the four correlation control signals W, X, Y and Z logically and generates a correlation coefficient.

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A first band pass filter BPF1 is arranged to band pass filter the output of the first delay device D1 and supplies the band pass filtered signal to a multiplexer MUX1. This multiplexer MUX1 receives the output signals supplied from the first band pass filter BPF1, the first subtractor 10 and the second subtractor 40, and outputs selectively one of the received signals in accordance with the correlation detecting coefficient which it receives from the coefficient generator 70.

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Figure 2 shows the correlation detector 60 of Figure 1 in more detail.

The correlation detector 60 comprises a first
5 comparator COM1 for comparing the output A of the first
low pass filter LPF1 with the output D of the second low
pass filter LPF2, a second multiplexer MUX2 for outputting
the outputs A and D of the two filters LPF1 and LPF2
selectively under the control of the first comparator
10 COM1; a second comparator COM2 for comparing a
predetermined first reference value Ref1 with the output
of the second multiplexer MUX2; a first OR gate G1 for
logically summing the outputs of the first and second
comparators COM1 and COM2, and outputting the first
15 correlation control signal W; a first inverter INV1 for
inverting the output of the first comparator COM1, a
second OR gate G2 for logically summing the output of the
first inverter INV1 and the output of the second
comparator COM2, and outputting the second correlation
20 control signal X.

The correlation detector 60 further comprises a third
comparator COM3 for comparing the output B of the second
band pass filter BPF2 with the output C of the third band
25 pass filter BPF3; a third multiplexer MUX3 for outputting
the output of the two filters BPF2 and BPF3 under the
control of the output of the third comparator COM3; a
fourth comparator COM4 for comparing a predetermined
second reference value Ref2 with the output of the third
30 multiplexer MUX3; a third OR gate G3 for logically summing
the output of the third and fourth comparators COM3 and
COM4, and outputting the third correlation control signal
Y; a second inverter INV2 for inverting the output of the
third comparator COM3; and a fourth OR gate G4 for
35 logically summing the output of the second inverter INV2

and the output of the fourth comparator COM4, and outputting the fourth correlation control signal Z.

Figure 3 shows the coefficient generator 70 of Figure 1 in more detail. This comprises third to sixth inverters INV3 to INV6 for inverting and outputting the first to fourth correlation control signals W,X,Y and Z; a first AND gate G5 for logically combining the first correlation control signal W with the output $\bar{X}$ of the fourth inverter INV4; a second AND gate G6 for logically combining the first correlation control signal W with the third correlation control signal Y; a third AND gate G7 for logically combining the first correlation control signal Y with the output $\bar{Z}$ of the sixth inverter INV6; and a fourth AND gate G8 for logically combining the second correlation control signal X with the fourth correlation control signal Z; a fifth OR gate G9 for logically combining the outputs of the first to third AND gates G5 to G7, and outputting a most significant bit MSB of a detection coefficient of the correlation; and a sixth OR gate G10 for logically combining the output of the fourth AND gate G8 with the outputs $\bar{W}$ and $\bar{Y}$ of the third and fifth inverters and outputting a least significant bit LSB of a detection coefficient of the correlation.

The embodiment of Figures 1 to 3 will now be described below in more detail, based on the aforesaid constitution.

Referring to Figure 1, the difference components between lines 2 and 3, and lines 2 and 1, provide $\Delta Y_L + \Delta Y_H + 2C$ at the first and second subtractors 10 and 40, respectively, and the sum motion components provide $2Y_L + 2Y_H + \Delta C$ at the first and second adders 20 and 30, respectively.

When the difference components are low pass filtered at the first and second low pass filters LPF1 and LPF2, respectively, the respective ΔY_L component is detected in each of the low pass filters LPF1 and LPF2 and, therefore, each detected ΔY_L component is input to the correlation detector 60 with an absolute value. When the sum motion components are band pass filtered at the second and third band pass filters BPF2 and BPF3, respectively, the respective ΔC component is detected in each of the band pass filters BPF2 and BPF3 and, therefore, each of the detected ΔC components is input to the correlation detector 60 with an absolute value in the same manner as ΔY_L . As described above, each of the detected signals A, B, C and D input to the correlation detector 60 generates each control signal for ΔY_L and ΔC correlation through a predetermined processing procedure.

First, referring to Figure 2, the second multiplexer MUX2 in the correlation detector 60 receives the ΔY_L signals A and D through two input terminals and detects the smaller signal among the two input signals. Here, the second multiplexer MUX2 is operated by the control signal of the first comparator COM1, the first comparator COM1 receiving and comparing the ΔY_L signals A and D output from the first low pass filter LPF1 and the second low pass filter LPF2 respectively, and outputting the compared result.

Thus, if the first low pass filtered ΔY_L signal A is larger than the second low pass filtered ΔY_L signal D, "1" is output. Therefore, the smaller signal detected in the second multiplexer MUX2 is input to one terminal of the second comparator COM2 and is compared with the predetermined first reference value Ref1 input to the other terminal of the second comparator COM2. As a

result, if the smaller value detected in the second multiplexer MUX2 is smaller than the first reference value Ref1, the second comparator COM2 outputs "0" and if the former is larger than the latter, the second comparator
5 COM2 outputs "1".

The output of the second comparator COM2 is input to one terminal of each of the first and second OR gates G1 and G2, and the output of the first comparator COM1 is
10 input to the other terminal of the first OR gate G1, and the inverted output of the first comparator COM1 through the first inverter INV1 is input to the other terminal of the second OR gate G2. Therefore, each of the two OR
15 gates G1 and G2 combines logically the input signals, respectively, and as a result, the first and second correlation control signals W and X are output.

The ΔC signals B and C are applied to the two input terminals of the third multiplexer MUX3. The third and
20 fourth correlation control signals Y and Z are generated by the two OR gates G3 and G4 respectively, of which the input terminals are connected to the output terminals of the third comparator COM3, the fourth comparator COM4 and the second inverter INV2, so that the processing is
25 similar to that of the ΔY_i signals which are described above.

The first to fourth correlation control signals (W,X,Y,Z) generated by the procedure described above are
30 input to the coefficient generator 70 and generate the detection coefficient of the correlation.

That is, as shown in Figure 3, the first correlation control signal W and the inverted signal $\bar{X}$ of the second
35 correlation control signal X output from the fourth

inverter INV4 are logically multiplied in the first AND gate G5. The first correlation control signal W and the third correlation control signal Y are logically multiplied in the second AND gate G6. The third correlation control signal Y and the inverted signal $\bar{Z}$ of the fourth correlation control signal Z output from the sixth inverter INV6 are logically multiplied in the third AND gate G7. Then, the outputs of the first to third AND gates G5 to G7 are logically summed in the fifth OR gate G9. The most significant bit MSB of the detection coefficient of the correlation is output from the fifth OR gate G9.

The second correlation control signal X and the fourth correlation control signal Z are logically multiplied by the fourth AND gate G8. The output of the fourth AND gate G8, and the inverted signals $\bar{W}$ and $\bar{Y}$ of the first and third correlation control signals (W, Y) output from the third and fifth inverters INV3 and INV5 are logically summed in the sixth OR gate G10. The least significant bit LSB of the detection coefficient of the correlation is output from the sixth OR gate G10. Therefore, the condition for generating the detection coefficient of the correlation in accordance with the first to fourth correlation control signals W, X, Y, and Z is shown in Table 1.

Table 1

YZ WX	01	10	11
01	01	11	01
10	11	10	10
11	01	10	11

5 Here WX is the control signal of ΔY_L , YZ is the control signal of ΔC , 01 represents combed processing with line 3 in Figure 1, 10 represents combed processing with line 1, and 11 represent that there is no correlation therebetween.

15 Therefore, if the detection coefficient of the correlation is applied to the selecting terminal of the first multiplexer MUX1, the multiplexer MUX1 selects and outputs the output of the first band pass filter BPF1 when there is no correlation. The multiplexer MUX1 selects and
20 outputs the signal output from the first subtractor 10 when the composite video signal is comb processed with line 3 and selects and outputs the signal output from the second subtractor 40 when the composite video signal is comb processed with line 1.

25 As described above, when the chrominance signal is separated from the composite signal, the similarity with the line above and the line below is detected. Then, the chrominance signal is separated from the line bearing the
30 larger similarity, thereby facilitating more accurate filtering and thus improving picture image quality.



CLAIMS

1. A circuit for separating chrominance signals from a composite video signal in a NTSC colour video signal processing system, the circuit comprising:

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a first delay device for 1H delaying a composite video signal;

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a first band pass filter for band pass filtering the output of said first delay device;

a second delay device for 1H delaying the output of said first delay device;

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a first subtractor for subtracting said composite video signal from the output of said first delay device;

a first adder for adding the output of said first delay device to said composite video signal;

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a second adder for adding the outputs of said first and second delay devices;

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a second subtractor for subtracting the output of said second delay device from that of said first delay device;

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first and second low pass filters for low pass filtering the outputs of said first and second subtractors respectively and outputting respective luminance difference signal components;

second and third band pass filters for filtering at a predetermined band the outputs of said first and second



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adders respectively, and outputting respective chrominance difference signal components;

5 a correlation detector for detecting correlation between the outputs of said first and second low pass and second and third band pass filters and generating first to fourth correlation control signals;

10 a coefficient generator for logically combining said first to fourth correlation control signals and generating a correlation detecting coefficient;

15 a multiplexer for receiving the output signal of said first band pass filter and the output signals of said first and second subtractors, and outputting one of the received signals selectively in dependence upon the value of said correlation detection coefficient.

20 2. A circuit according to claim 1, wherein said correlation detector comprises a first comparator for comparing the outputs of said first and second low pass filters;

25 a second multiplexer for outputting the outputs of said two low pass filters selectively under control of said first comparator;

30 a first comparator for comparing a predetermined first reference value with the output of said second multiplexer;

a first OR gate for logically summing the outputs of said first and second comparators, and outputting a first correlation control signal;

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a first inverter for inverting the output of said first comparator;

5 a second OR gate for logically summing the output of said first inverter and the output of said second comparator and outputting a second correlation control signal;

10 a third comparator for comparing the output of said second and third band pass filters;

15 a third multiplexer for outputting the output of said second and third band pass filters selectively under control of the output of said third comparator;

a fourth comparator for comparing a predetermined second reference value with the output of said third multiplexer;

20 a third OR gate for logically summing the output of said third and fourth comparators and outputting a third correlation control signal;

25 a second inverter for inverting the output of said third comparator; and

30 a fourth OR gate for logically summing the output of said second inverter and the output of said fourth comparator and outputting a fourth correlation control signal.

3. A circuit substantially as hereinbefore described with reference to Figures 1 to 3 of the accompanying drawings.



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4. A method substantially as hereinbefore described with reference to Figures 1 to 3 of the accompanying drawings.

5. A colour video signal processing system provided with a circuit according to claim 1, 2 or 3.

6. A colour television or video recorder provided with a signal processing system according to claim 5.

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