WHAT IS CLAIMED IS:

1. An apparatus comprising:

a memory array comprising a plurality of memory cells; and

a memory controller configured to:

receive a single command which specifies a plurality of memory access operations to be performed on the memory array, and

cause the specified plurality of memory access operations to be performed on the memory array, wherein each of the plurality of memory access operations specified in the single command comprises one of a program operation or a read operation.

2. The apparatus of Claim 1,

wherein the memory array comprises phase change memory (PCM) cells, and

wherein the memory controller is further configured to cause the specified plurality of memory access operations by:

causing a plurality of word lines of the memory array to be pre-charged from an initial voltage to a pre-charge voltage;

causing a first memory access pulse to be applied to a first PCM cell connected to one of the plurality of word lines such that a first memory access operation is performed;

causing a second memory access pulse to be applied to a second PCM cell connected to one of the plurality of word lines such that a second memory access operation is performed; and

causing the plurality of word lines to be discharged to the initial voltage.

3. The apparatus of Claim 2, wherein the first PCM cell and the second PCM cell are connected to a same word line of the memory array and are connected to different columns of the memory array.

4. The apparatus of Claim 2, wherein the memory controller is further configured to cause the first memory access pulse to be applied and to cause the second memory access

pulse to be applied without causing the plurality of word lines to be discharged between the first and second memory access pulses.

5. The apparatus of Claim 2, wherein the first memory access pulse comprises one of a SET pulse or a RESET pulse, and wherein the second memory access pulse comprises the same one of the SET pulse or the RESET pulse as the first memory access pulse.

6. The apparatus of Claim 2, wherein the first memory access pulse comprises one of a SET pulse or a RESET pulse, and wherein the second memory access pulse comprises a different one of the SET pulse or the RESET pulse as the first memory access pulse.

7. The apparatus of Claim 5, wherein the memory controller is further configured to:

cause a first program verification pulse to be applied to the first PCM cell after causing the first memory access pulse to be applied to the first PCM cell; and

cause a second program verification pulse to be applied to the second PCM cell after causing the second memory access pulse to be applied to the second PCM cell.

8. The apparatus of Claim 7, wherein causing a memory access pulse and subsequently causing a verification pulse include keeping a word line voltage substantially constant.

9. The apparatus of Claim 5, wherein the memory controller is further configured to:

cause first and second program verification pulses to be applied to the respective first and second PCM cells after causing the first and second memory access pulse to be applied to the first PCM cell.

10. The apparatus of Claim 2, wherein one of the first and second memory access pulses comprises one of a SET pulse or a RESET pulse and another one of the first and second memory access pulses comprises a read pulse.

11. An apparatus comprising:

a managed memory device comprising a plurality of memory devices; and

a memory controller configured to:

receive a single command which specifies a plurality of memory access operations to be performed on the memory devices, and

cause the specified plurality of memory access operations to be performed on the memory devices, wherein each of the plurality of memory access operations specified in the single command comprises one of a write operation or a read operation.

12. The apparatus of Claim 11, wherein the memory controller is integrated with the memory devices in a single package.

13. The apparatus of Claim 11,

wherein each of the memory devices comprises a plurality of pages of flash memory cells, wherein each page of flash memory cells comprise a plurality of flash memory cells connected to a common word line, and

wherein the single command specifies a first memory operation and a second memory operation, wherein the second memory operation comprises a different one of a program operation or a read operation from the first memory operation, and

wherein the memory controller is further configured to cause the specified plurality of memory access operations by:

causing the first memory access operation to be performed on a fraction of a page of flash memory cells, and

causing the second memory access operation to be performed on a fraction of a page of flash memory cells.

14. The apparatus of Claim 13,

wherein the single command further specifies a third memory operation of a type that is the same as one of the first or second memory operations, and

wherein the memory controller is further configured to cause the third memory access operation to be performed on a fraction of a page of flash memory cells,

wherein the memory controller is further configured to cause the third memory access operation and the one of the first and second memory operations that is the same as the third memory access operation to be performed sequentially on the same page.

15. An electronically-implemented method of accessing a memory array comprising a plurality of memory cells, the method comprising:

receiving a single command that specifies a plurality of memory access operations to be performed on the memory array; and

performing the specified plurality of memory access operations on the memory array,

wherein each of the specified plurality of memory access operations of the single command comprises one of a program operation or a read operation

16. The method of Claim 15, wherein the memory array comprises a plurality of phase change memory (PCM) cells, and wherein performing the specified plurality of memory access operations comprises:

pre-charging a plurality of word lines of the memory array from an initial voltage to a pre-charge voltage;

applying a first memory access pulse to a first PCM cell connected to one of the plurality of word lines;

applying a second memory access pulse to a second PCM cell connected to one of the plurality of word lines; and

discharging the plurality of word lines to the initial voltage.

17. The method of Claim 16, wherein the first PCM cell and the second PCM cell are connected to a same word line of the memory array and are connected to different columns of the memory array.

18. The method of Claim 16, wherein the first and second memory access pulses are applied without discharging the remaining ones of the plurality word lines between the first and second memory access pulses.

19. The method of Claim 18, wherein first and second memory access pulses each comprise a same one of a SET pulse or a RESET pulse.

20. The method of Claim 19, wherein performing the specified plurality of memory access operations further comprises:

applying a first program verification pulse to the first PCM cell after applying the first memory access pulse to the first PCM cell; and

applying a second program verification pulse to the second PCM cell after applying the second memory access pulse to the second PCM cell.

21. The method of Claim 15, wherein the memory array comprises a plurality of pages of flash memory cells, wherein each page of flash memory cells comprise a plurality of flash memory cells connected to a common word line, and

wherein the single command specifies a first memory operation and a second memory operation different from the first memory operation,

wherein performing the specified plurality of memory access operations comprises:

performing the first memory access operation on a fraction of a page of flash memory cells, and

performing the second memory access operation on a fraction of a page of flash memory cells.

22. The method of Claim 21,

wherein the single command further specifies a third memory operation of a type that is the same as one of the first or second memory operations, and

wherein performing the specified plurality of memory access operations further comprises performing the third memory access operation on a fraction of the page on which the one of the first and second memory operations same as the third memory operation is performed on.

23. An apparatus comprising:

a memory array;

a memory controller configured to cause a plurality of memory access operations on the memory array in response to a single command from a host,

wherein the single command specifies consecutive operational descriptors specifying each of the plurality of memory access operations to be caused on the memory array,

wherein each of the multiple memory access operations of the single command comprises one of a write operation or a read operation.

24. The apparatus of Claim 23, wherein the memory access operations comprise different ones of write or read operations.

25. The apparatus of Claim 23, wherein the memory controller is further configured to generate a single status corresponding to the multiple memory access operations after causing the plurality of memory access operations.

26. The apparatus of Claim 23, wherein the memory controller is configured to cause the multiple operations in an order that is different from an order in which the consecutive operational descriptors are specified in the single command.

CLAIMS

1. An apparatus comprising:

a memory array comprising a plurality of memory cells; and

a memory controller configured to:

receive a single command which specifies a plurality of memory access operations to be performed on the memory array, wherein each of the plurality of memory access operations specified in the single command comprises one of a program operation or a read operation, and

cause the specified plurality of memory access operations to be performed on the memory array by causing a plurality of word lines of the memory array to be pre-charged from an initial voltage to a pre-charge voltage, causing a first memory access operation to be performed, causing a second memory access operation to performed, and causing the plurality of word lines to be discharged to the initial voltage.

2. An apparatus comprising:

a memory array comprising a plurality of phase change memory (PCM) cells; and

a memory controller configured to:

receive a single command which specifies a plurality of memory access operations to be performed on the memory array, wherein each of the plurality of memory access operations specified in the single command comprises one of a program operation or a read operation; and

the memory controller is further configured to cause the specified plurality of memory access operations by:

causing a plurality of word lines of the memory array to be pre-charged from an initial voltage to a pre-charge voltage;

causing a first memory access pulse to be applied to a first PCM cell connected to one of the plurality of word lines such that a first memory access operation is performed;

causing a second memory access pulse to be applied to a second PCM cell connected to one of the plurality of word lines such that a second memory access operation is performed; and

causing the plurality of word lines to be discharged to the initial voltage.

3. The apparatus of Claim 2, wherein the first PCM cell and the second PCM cell are connected to a same word line of the memory array and are connected to different columns of the memory array.

4. The apparatus of Claim 2, wherein the memory controller is further configured to cause the first memory access pulse to be applied and to cause the second memory access pulse to be applied without causing the plurality of word lines to be discharged between the first and second memory access pulses.

5. The apparatus of Claim 2, wherein the first memory access pulse comprises one of a SET pulse or a RESET pulse, and wherein the second memory access pulse comprises the same one of the SET pulse or the RESET pulse as the first memory access pulse.

6. The apparatus of Claim 2, wherein the first memory access pulse comprises one of a SET pulse or a RESET pulse, and wherein the second memory access pulse comprises a different one of the SET pulse or the RESET pulse as the first memory access pulse.

7. The apparatus of Claim 5, wherein the memory controller is further configured to:

cause a first program verification pulse to be applied to the first PCM cell after causing the first memory access pulse to be applied to the first PCM cell; and

cause a second program verification pulse to be applied to the second PCM cell after causing the second memory access pulse to be applied to the second PCM cell.

8. The apparatus of Claim 7, wherein causing a memory access pulse and subsequently causing a verification pulse include keeping a word line voltage substantially constant.

9. The apparatus of Claim 5, wherein the memory controller is further configured to:

cause first and second program verification pulses to be applied to the respective first and second PCM cells after causing the first and second memory access pulse to be applied to the first PCM cell.

10. The apparatus of Claim 2, wherein one of the first and second memory access pulses comprises one of a SET pulse or a RESET pulse and another one of the first and second memory access pulses comprises a read pulse.

11. An apparatus comprising:

a managed memory device comprising a plurality of flash memory devices; and

a memory controller configured to:

receive a single command which specifies a plurality of memory access operations to be performed on the managed memory device;

combine a first memory access operation and a second memory access operation of the plurality of memory access operations to be performed on a same page of the managed memory device; and

cause the specified plurality of memory access operations and the combined first and second memory access operations to be performed on the managed memory device, wherein each of the plurality of memory access operations specified in the single command comprises one of a write operation or a read operation.

12. The apparatus of Claim 11, wherein the memory controller is integrated with the plurality of flash memory devices in a single package.

13. An apparatus comprising:

a managed memory device comprising a plurality of memory devices; and

a memory controller configured to:

receive a single command which specifies a plurality of memory access operations to be performed on the memory devices, and

cause the specified plurality of memory access operations to be performed on the memory devices, wherein each of the plurality of memory access operations specified in the single command comprises one of a write operation or a read operation,

wherein each of the memory devices comprises a plurality of pages of flash memory cells, wherein each page of flash memory cells comprises a plurality of flash memory cells connected to a common word line,

wherein the single command specifies a first memory operation and a second memory operation, wherein the second memory operation comprises a different one of a program operation or a read operation from the first memory operation, and

wherein the memory controller is further configured to cause the specified plurality of memory access operations by:

causing the first memory access operation to be performed on a fraction of a page of flash memory cells, and

causing the second memory access operation to be performed on a fraction of a page of flash memory cells.

14. The apparatus of Claim 13,

wherein the single command further specifies a third memory operation of a type that is the same as one of the first or second memory operations,

wherein the memory controller is further configured to cause the third memory access operation to be performed on a fraction of a page of flash memory cells, and

wherein the memory controller is further configured to cause the third memory access operation and the one of the first and second memory operations that is the same as the third memory access operation to be performed sequentially on the same page.

15. An electronically-implemented method of accessing a memory array comprising a plurality of memory cells, the method comprising:

receiving a single command that specifies a plurality of memory access operations to be performed on the memory array; and

performing the specified plurality of memory access operations on the memory array,

wherein each of the specified plurality of memory access operations of the single command comprises one of a program operation or a read operation, and

wherein performing the specified plurality of memory access operations comprises:

pre-charging a plurality of word lines of the memory array from an initial voltage to a pre-charge voltage;

applying a first memory access pulse to a memory cell connected to one of the plurality of word lines;

applying a second memory access pulse to a second memory cell connected to one of the plurality of word lines; and

discharging the plurality of word lines to the initial voltage.

16. An electronically implemented method of accessing a memory array comprising a plurality of phase change memory (PCM) cells, the method comprising:

receiving a single command that specifies a plurality of memory access operations to be performed on the memory array; and

performing the specified plurality of memory access operations on the memory wherein each of the specified plurality of memory access operations of the single command comprises one of a program operation or a read operation,

wherein the memory array comprises a plurality of phase change memory (PCM) cells, and

wherein performing the specified plurality of memory access operations comprises:

pre-charging a plurality of word lines of the memory array from an initial voltage to a pre-charge voltage;

applying a first memory access pulse to a first PCM cell connected to one of the plurality of word lines;

applying a second memory access pulse to a second PCM cell connected to one of the plurality of word lines; and

discharging the plurality of word lines to the initial voltage.

17. The method of Claim 16, wherein the first PCM cell and the second PCM cell are connected to a same word line of the memory array and are connected to different columns of the memory array.

18. The method of Claim 16, wherein the first and second memory access pulses are applied without discharging remaining ones of the plurality of word lines between the first and second memory access pulses.

19. The method of Claim 18, wherein first and second memory access pulses each comprise a same one of a SET pulse or a RESET pulse.

20. The method of Claim 19, wherein performing the specified plurality of memory access operations further comprises:

applying a first program verification pulse to the first PCM cell after applying the first memory access pulse to the first PCM cell; and

applying a second program verification pulse to the second PCM cell after applying the second memory access pulse to the second PCM cell.

21. The method of Claim 15,

wherein the memory array comprises a plurality of pages of flash memory cells,

wherein each page of flash memory cells comprises a plurality of flash memory cells connected to a common word line,

wherein the single command specifies a first memory operation and a second memory operation different from the first memory operation, and

wherein performing the specified plurality of memory access operations comprises:

performing the first memory access operation on a fraction of a page of flash memory cells, and

performing the second memory access operation on a fraction of a page of flash memory cells.

22. The method of Claim 21,

wherein the single command further specifies a third memory operation of a type that is the same as one of the first or second memory operations, and

wherein performing the specified plurality of memory access operations further comprises performing the third memory access operation on a fraction of the page on which the

one of the first and second memory operations same as the third memory operation is performed on.

23. An apparatus comprising:

a memory array; and

a memory controller configured to cause a plurality of memory access operations on the memory array in response to a single command from a host,

wherein the single command specifies a list of consecutive operational descriptors specifying information related to each of the plurality of memory access operations to be caused on the memory array, and

wherein each of the multiple memory access operations of the single command comprises one of a write operation or a read operation.

24. The apparatus of Claim 23, wherein the memory access operations comprise different ones of write or read operations.

25. The apparatus of Claim 23, wherein the memory controller is further configured to generate a single status corresponding to the multiple memory access operations after causing the plurality of memory access operations.

26. The apparatus of Claim 23, wherein the memory controller is configured to cause the multiple operations in an order that is different from an order in which the consecutive operational descriptors are specified in the single command.