

SEQUENCING CHIP AND MANUFACTURING MEHTOD

THEREFOR

TECHNICAL FIELD

[0001] The present disclosure relates to the field of biotechnology, and particularly, to a sequencing chip and a manufacturing method therefor.

BACKGROUND

[0002] The microarray sequencing chip is one of the prerequisites for high-throughput sequencing. In the current DNA Nano Ball (DNB) sequencing technology, DNBs are required to be fixed on a sequencing chip for subsequent sequencing biochemical reactions. As an example, for the sequencing chips now in use, nearly 200 million DNB-binding sites are provided on a surface of each chip. In order to stably fix the DNBs to the binding sites, the surface of the sequencing chip is required to subject to an amination treatment. In addition, regions on the chip surface other than binding sites are required to subjected other treatments, in order to reduce non-specific adsorption as much as possible, reduce background optical signal, and improve sequencing quality. Accordingly, one of the basic tasks for achieving high-quality sequencing is to manufacture sequencing chips with microarrays efficiently and with lost cost.

[0003] The existing method for manufacturing sequencing chip mainly includes the following steps. A nano-array patterned photoresist layer is first formed on a silicon wafer through a semiconductor process. The patterned layer may include multiple units with the same structure, and each unit can serve as one sequencing chip. Then the wafer including the patterned layer is subjected to a chemical vapor deposition to form an amination layer in a functional region of the wafer. Through an assembly process, the wafer is divided into individual chips, which are assembled into sequencing chips suitable for sequencing.

[0004] The process of forming the patterned photoresist layer on the silicon wafer includes:

[0043] FIG. 17A is a cross-sectional view of a sequencing chip 3-60A with a DNB array according to an embodiment of the present disclosure, which is formed after DNBs are loaded on the sequencing chip 3-50 that has been subjected to a surface functionalization modification shown in FIG. 16;

5 **[0044]** FIG. 17B is a cross-sectional view of a simpler sequencing chip 3-60B according to an embodiment of the present disclosure, in which a DNB array can be formed on the sequencing chip without performing a surface modification;

[0045] FIG. 17C illustrates another relation between the fluorescence signal of different "well" structures based on a silicon substrate and the second oxide layer according to an
10 embodiment of the present disclosure.

[0046] FIGS. 18-22 are cross-sectional views of respective processes in a preparation of a back-illuminated sequencing chip according to another aspect of the present disclosure, which includes a patterned transition metal oxide layer having arrayed "spot" structures;

[0047] FIG. 18 is a cross-sectional view of a wafer structure 4-10 according to an
15 embodiment of the present disclosure, in which a transition metal oxide layer film having arrayed "spot" structures is formed on a silicon oxide layer of a wafer;

[0048] FIG. 19 is a cross-sectional view of multiple individual chips 4-20 formed after the wafer structure 4-10 with arrayed "spot" structures as shown in FIG. 18 is subjected to a dicing process according to an embodiment of the present disclosure;

20 **[0049]** FIG. 20 is a cross-sectional view of a sequencing chip 4-30 formed by assembling the individual chip 4-20 shown in FIG. 19 according to an embodiment of the present disclosure. During the assembly process, the chip and the frame are assembled with the patterned layer facing downward, and thus an excitation light source/camera illuminates the DNBs and acquires signals through the quartz or glass substrate from the back of the chip;

25 **[0050]** FIG. 21 is a cross-sectional view of a sequencing chip 4-40 according to an embodiment of the present disclosure, which is formed after the sequencing chip shown in FIG. 20 is subjected to a surface functionalization modification;

[0051] FIG. 22A is a cross-sectional view of a sequencing chip 4-50A with a DNB array according to an embodiment of the present disclosure, which is formed after DNBs are loaded
30 on the sequencing chip 4-40 that has been subjected to a surface functionalization modification

and an extremely narrow non-functional spacing is reserved between the chips. This spacing is also referred as to a cutting line where the wafer can be cut by the cutting blade into a plurality of individual chips without damaging the effective structural region of the chips.

[00153] FIG. 2 is a cross-sectional view of multiple individual wafers 1-20 formed after the wafer 1-10 having the patterned transition metal oxide layer is subjected to a dicing process. As illustrated in FIG. 2, the wafer has been cut into individual chips separated through the cutting slot 121. FIG. 2 illustrate the individual chips 11 and 12 formed after the dicing process.

[00154] FIG. 3 is a cross-sectional view of a sequencing chip 1-30 formed by assembling one single chip. One single chip having the patterned surface layer 113 is first placed into a frame structure 131 including a liquid inlet and outlet 133, then a hydrophobically treated cover glass 132 is attached onto the frame 131, and a fluid channel 134 is formed between the cover glass 132 and the chip including the patterned surface 113, thereby allowing liquid to be introduced into or discharged from the fluid channel 134 via the liquid inlet and outlet 133. In this figure, the related components are fixed by using adhesives during assembling the chip into the frame 131 and attaching the cover glass 132 onto the frame 131, and any suitable adhesive can be employed in the present disclosure. In this figure, the structure of the assembled sequencing chip is schematically illustrated, i.e., including the frame for providing the liquid inlet and outlet, and the cover glass for forming the fluid channel together with the frame. However, those skilled in the art should recognize that any frame and cover glass that are made of suitable materials, and any frame and cover glass structure that can provide the liquid inlet and outlet and the fluid channel should be included in the present disclosure.

[00155] FIG. 4 illustrates a sequencing chip 1-40 formed after the sequencing chip 1-30 is subjected a surface functionalization modification. Liquid used for surface modification can be introduced into the fluid channel via the liquid inlet and outlet and contact the transition metal oxide region and the silicon oxide region to functionally modify the surfaces thereof, thereby providing them with a function of adsorbing DNBs (i.e., serving as DNB-binding site, transition metal oxide region, functional region) and a function of repelling DNBs (i.e., serving as DNB non-binding site, silicon oxide region, non-functional region), respectively. The surface modification includes: 1) forming a polyethylene glycol molecular layer 142 on the surface of the silicon oxide layer; and 2) forming multiple amino groups 141 on the transition metal oxide

[00191] As shown in FIG. 23 to FIG. 28, the present embodiment provides cross-sectional views of respective processes of a method for manufacturing a back-illuminated sequencing chip having "well"-structured transition metal oxide on a quartz wafer. The method of Embodiment uses a quartz wafer or any other suitable transparent glass wafer as the substrate, and prepares a patterned transition metal oxide layer with patterned "well" structures on the substrate wafer. The chip is assembled in such a manner that the patterned layer faces downward, and thus the excitation light source/camera excites the DNBs and acquires the fluorescence signal from the back of the chip, i.e., through the quartz wafer substrate.

[00192] FIG. 23 is a cross-sectional view of a wafer structure 5-10, in which a silicon oxide layer and a transition metal oxide layer are formed on a bare wafer. The forming process thereof is similar to that described in Embodiment 2 with reference to FIG. 6.

[00193] FIG. 24 is a cross-sectional view of a wafer 5-20, in which a silicon oxide layer having patterned "well" structures is formed on the transition metal oxide layer of the wafer 5-10 as shown in FIG. 23. The forming process thereof is similar to that described in Embodiment 2 with reference to FIG. 7.

[00194] FIG. 25 is a cross-sectional view of multiple individual chips 5-30 formed after the wafer structure 5-20 of FIG. 24 is subjected to a dicing process. In this figure, the dicing process is similar to that in described in Embodiment 1 with reference to FIG. 2.

[00195] FIG. 26 is a cross-sectional view of a sequencing chip 5-40 formed after one single chip shown in FIG. 25 is subjected to a packaging process. In this process step, the sequencing chip is assembled with and attached to a frame 431 including a liquid inlet and outlet 432 in such a manner that the patterned layer faces downward, and a fluid channel 433 is formed between the frame and the patterned layer on the chip. In this figure, the process of assembling is similar to that described in Embodiment 3 with reference to FIG. 20.

[00196] FIG. 27 is a cross-sectional view of a sequencing chip 5-50 formed after the sequencing chip 5-40 shown in FIG. 26 is subjected to a surface functionalization modification. The process of the functionalization modification is similar to that described in Embodiment 1 with reference to FIG. 4.

[00197] FIG. 28A is a cross-sectional view of a sequencing chip 5-60A with a DNB array formed after DNBs are loaded on the sequencing chip 5-50 shown in FIG. 27, which has been

7-10. Those skilled in the art should recognize that one CMOS wafer may have a plurality of chips, and only two chips 71 and 72 are schematically shown in this figure. As shown in FIG. 35, the CMOS image sensor wafer includes a photosensitive layer 73, an interconnection layer 74, a substrate layer 75, and a dielectric film layer 717 on the photosensitive layer 73. The dielectric film layer is usually formed by stacking a hafnium dioxide film and a tantalum pentoxide film, and a silicon oxide layer 718 is located on the dielectric film layer 717. The photosensitive layer 73 includes a photosensitive part 716 formed in a semiconductor material 715, and the photosensitive part 716 may be a photodiode. The semiconductor material layer 715 can be made of any suitable material, such as silicon, III-V family materials on silicon, graphene on silicon, silicon on insulator, and combinations thereof. Although the photodiode 716 is described in the present disclosure, it should be understood that any suitable photosensitive structures can be applied in the present disclosure. The photodiode 716 can convert a measured light signal into a current signal. The photodiode 716 may include a source and a drain of one metal oxide semiconductor (MOS) transistor, which can transmit the current to other components, such as to another MOS transistor. Other components, such as reset transistors, current source followers, or row selectors configured to convert current values into digital signals, may also be included. A CMOS graphic sensor 7-10 may also include a dielectric layer, and it should be noted that this dielectric layer may include any suitable electrical insulating material. The interconnection layer 74 includes a metal wiring 714 formed in a dielectric layer 713, the metal wiring 714 can be used for internal interconnection of integrated circuit materials and also for electrical connection to the outside. The substrate layer 75 includes a silicon substrate 711 and a CMOS processing circuit layer 712. The CMOS processing circuit layer may include a CMOS circuit required for sequencing operations. For example, the CMOS processing circuit layer 712 may include circuits for image processing, signal processing, control functions for sequencing operations, and external communication. The CMOS processing circuit 712 processes photosensitive signals sensed by the photosensitive layer 73 into electrical signals, and transmits the electrical signals to an external device through interconnection silicon through-holes 720 and pads 719.

[00214] Those skilled in the art should appreciate that the structure of the CMOS image sensor chip described in the present disclosure is merely illustrative, but is not restrictive, and

oxide layer film, and the intensity of fluorescence signal is the highest when the thickness is 10nm to 20 nm.

[00229] Further, when the second silicon oxide layer having the "well" structures is formed thereon, a relation between the thickness of the second silicon oxide layer and the intensity of fluorescence signal is simulated. The simulation results are shown in FIG. 41F. When the thickness of the transition metal oxide layer is fixed, a correlation between the intensity of the optical signal acquired from this structure and the thickness of the second oxide layer is negligible. Taking fluid requirements for DNA sequencing into account, if the thickness of the second oxide layer is too great, the surface structures may be too deep, which may easily lead to "fluid dead zones" and affect the quality of sequencing. The appropriate thickness of the second oxide layer allows DNBs to be tested to fall into the active regions effectively, and the thickness of the second oxide layer can be selected to be 50 nm to 100 nm.

[00230] Embodiment 8: Another packaging method of reusable sequencing chip

[00231] In this embodiment, a new method for packaging a sequencing chip is provided. The sequencing chip used in this packaging method can be reused after subjected to a special processing process, thereby greatly reducing the costs of the sequencing chip.

[00232] A patterned array of transition metal oxide "spot" or "well" structures is first formed on a semiconductor wafer. The structure of such a patterned array can be any one of the structures present on the wafers described in the above Embodiments 1 to 3 with reference to FIG. 1, FIG. 7, and FIG. 13. In the present embodiment, the structure shown in FIG. 1 of Embodiment 1 is taken as an example to describe the manufacturing process of the reusable sequencing chip, and other structures of sequencing chip described in the present disclosure can also be used for manufacturing the reusable sequencing chip with the same packaging process.

[00233] FIG. 42 is a cross-sectional view of a wafer structure 8-10 including a transition metal oxide layer having arrayed "spot" structures, which is the same as that shown in FIG. 1 of Embodiment 1. A silicon oxide layer 812 is formed on a semiconductor wafer substrate 811, the transition metal oxide layer 813 having "spot" structures is formed on the silicon oxide layer 812, and the process and material required in each step are the same as those described in Embodiment 1 with reference to FIG. 1.

[00234] FIG. 43 is a cross-sectional view of a wafer structure 8-20 formed after the wafer

CLAIMS

What is claimed is:

1. A chip matrix, comprising:

a wafer, wherein the wafer has cutting lines that are evenly distributed on the wafer;

a first silicon oxide layer, wherein the first silicon oxide layer is made of silicon oxide and is formed on an upper surface of the wafer; and

a transition metal oxide layer, wherein the transition metal oxide layer is made of a transition metal oxide and is formed on an upper surface of the first silicon oxide layer.

2. The chip matrix according to claim 1, wherein the transition metal oxide layer consists of a plurality of transition metal oxide spots that are unconnected to each other;

the plurality of transition metal oxide spots has a thickness of 10 nm to 20 nm; and the first silicon oxide layer has a thickness of 80 nm to 100 nm, preferably 90 nm;

the plurality of transition metal oxide spots is connected with amino groups; and

optionally, the first silicon oxide layer located among the plurality of transition metal oxide spots that are unconnected to each other is connected with polyethylene glycol.

3. The chip matrix according to claim 1 or 2, further comprising a second silicon oxide layer, wherein

the transition metal oxide layer is of a continuous layer structure, and the second silicon oxide layer is made of silicon oxide and formed on an upper surface of the transition metal oxide layer as a plurality of wells that are connected to each other; or

the transition metal oxide layer consists of a plurality of transition metal oxide spots that are unconnected to each other, and the second silicon oxide layer is formed on the upper surface of the first silicon oxide layer located among the plurality of transition metal oxide spots that are unconnected to each other.

4. The chip matrix according to claim 3, wherein

the wafer is a silicon wafer, the second silicon oxide layer has a thickness ranging from 40 nm to 60 nm, preferably 50 nm, the transition metal oxide layer has a thickness ranging from 5 nm to 15 nm, and the first silicon oxide layer has a thickness ranging from 80 nm to 100 nm, preferably 90 nm; or

the wafer is a quartz wafer, the second silicon oxide layer has a thickness ranging from

100 nm to 200 nm, the transition metal oxide layer has a thickness ranging from 10nm to 20nm, and the first silicon oxide layer has a thickness ranging from 80 nm to 100 nm, preferably 90nm.

5. The chip matrix according to claim 3, wherein,

when the transition metal oxide layer is of a continuous layer structure, amino groups are connected to the transition metal oxide layer at a bottom of each well of the second silicon oxide layer; or when the transition metal oxide layer consists of a plurality of transition metal oxide spots, amino groups are connected to the plurality of transition metal oxide spots; and

optionally, the second silicon oxide layer is connected with polyethylene glycol.

6. The chip matrix according to claim 5, wherein the amino groups are connected to at least a part of transition metal oxide molecules in the transition metal oxide layer through chemical bonds;

optionally, the chemical bonds are formed by the at least part of transition metal oxide molecules and phosphate groups of aminophosphonic acid-based compounds.

7. The chip matrix according to claim 5, wherein the polyethylene glycol is provided by at least one selected from polyethyleneimine-polyethylene glycol and a silane coupling agent containing polyethylene glycol;

when the polyethylene glycol is provided by the polyethyleneimine-polyethylene glycol, and the polyethyleneimine-polyethylene glycol is electrostatically adsorbed on a surface of the first silicon oxide layer or a surface of the second silicon oxide layer; and

when the polyethylene glycol is provided by the silane coupling agent containing polyethylene glycol, and the silane coupling agent containing polyethylene glycol is connected to the first silicon oxide layer or the second silicon oxide layer through a -Si-O-Si- chain.

8. The chip matrix according to any one of claims 1-7, wherein the transition metal oxide comprises at least one of titanium dioxide, zirconium dioxide, tantalum pentoxide, niobium hexaoxide, or hafnium dioxide.

9. A sequencing chip, comprising a chip body, wherein the chip body comprises a number of chip units obtained by cutting the chip matrix according to any one of claims 1 to 8 along the cutting lines of the wafer.

10. The sequencing chip according to claim 9, wherein the sequencing chip is reusable.

11. A method for manufacturing the chip matrix according to any one of claims 1-8, the method comprising: performing surface modification on the wafer,

wherein the surface modification comprises: treating a surface of the wafer with a transition metal oxide to form the transition metal oxide layer, wherein the transition metal oxide layer is formed on an upper surface of the first silicon oxide layer, the first silicon oxide layer is provided on the upper surface of the wafer, and the silicon oxide layer is made of silicon oxide, and the wafer has cutting lines evenly distributed on the wafer.

12. The method according to claim 11, wherein the first silicon oxide layer is formed in advance on the upper surface of the wafer by low-temperature plasma chemical vapor deposition, plasma enhanced chemical vapor deposition, sputtering, or atomic layer deposition.

13. The method according to claim 11, wherein the surface modification of the wafer is performed by thin film deposition, photolithography, or etching to form the transition metal oxide layer in form of a continuous layer or in form of arrayed spots.

14. The method according to claim 13, wherein, for the transition metal oxide layer in form of a continuous layer, the method further comprises forming, with silicon oxide, a second silicon oxide layer in form of continuous wells on an upper surface of the transition metal oxide layer;

optionally, for the transition metal oxide layer in form of arrayed spots, the method further comprises depositing silicon oxide between the spots of the transition metal oxide layer to form a second silicon oxide layer.

15. The method according to any one of claims 11-14, further comprising performing amination treatment on the transition metal oxide,

wherein the amination treatment is performed by reacting transition metal oxide with an aminophosphonic acid-based compound.16. The method according to any one of claims 11-15, further comprising performing a surface modification on the first silicon oxide layer or the second silicon oxide layer to introduce polyethylene glycol on the first silicon oxide layer or the second silicon oxide layer;

wherein the polyethylene glycol is provided by at least one of polyethyleneimine-polyethylene glycol or a silane coupling agent containing polyethylene glycol;

optionally, when the polyethylene glycol is provided by polyethyleneimine-polyethylene glycol, the surface modification is performed by electrostatic adsorption of polyethyleneimine-polyethylene glycol on a surface of the first silicon oxide layer or a surface of the second silicon oxide layer;

optionally, when the polyethylene glycol is provided by the silane coupling agent

containing polyethylene glycol, the surface modification is performed by condensation reaction of the silane coupling agent containing polyethylene glycol with hydroxyl groups of the first silicon oxide layer or the second silicon oxide layer, wherein the hydroxyl groups are provided by Si-OH generated after the first silicon oxide layer or the second silicon oxide layer is ionized and adsorbs hydroxide ions in water.

17. A method for manufacturing a sequencing chip, comprising:

assembling a chip unit, wherein the chip unit is obtained by cutting a chip matrix along cutting lines of a wafer layer of the chip matrix, the chip matrix is as defined in any one of claims 1-8 or obtained by the method according to any one of claims 11-16.

18. The method according to claim 17, wherein said assembling comprises placing the chip unit in a supporting frame including a liquid inlet and outlet, and bonding the chip unit to the supporting frame with a glue or adhesive, a fluid channel being formed between the frame and the chip unit.

19. The method according to claim 18, wherein, when the wafer is a silicon wafer, said assembling comprises: bonding the chip unit to the support frame with an upper surface of the chip unit facing upward, and placing a cover glass on the upper surface of the chip unit to obtain the sequencing chip.

20. The method according to claim 18, wherein, when the wafer is a quartz wafer or a glass wafer, said assembling comprises: bonding the chip unit to the support frame with a lower surface of the chip unit facing upward to obtain the sequencing chip.

21. A sequencing method, comprising performing sequencing using the sequencing chip as defined in claim 9 or manufactured by the method of any one of claims 17-20.