

The invention relates to a method and to a circuit arrangement for transmitting data signals between control devices interconnected via a clock-controlled loop system which is direction-dependently operated, which control devices are formed, in particular, by control devices of a data switching system, in which method and arrangement a transmit authorization signal is transmitted via the loop system from control device to control device, which signal controls these devices in each case to assume a transmit authorization state, the respective control device emitting to the loop system data signals to be transmitted by it, together with a receiver address designating a desired control device, before forwarding the transmit authorization signal, and in which method and arrangement a control device which is designated by the receiver address transmitted together with the data signals accepts these data signals for further processing and emits an acknowledgement signal, to be forwarded via the loop system, which is intended for that control device which is in an acknowledgement receiving state and from which the data signals have been emitted.

A method of the type mentioned above is already known (German Offenlegungsschrift 3,136,586). In this known method, the control device, by which data signals have been emitted, remains in the said acknowledgement receiving state until it receives an acknowledgement signal generated by the control device, selected as receiver, following the acceptance of the data signals. It may also happen that an acknowledgement signal fails to arrive, either due to a faulty operation of the loop system or due to a sporadic falsification of the information items contained in the acknowledgement signal, so that the control device, by which the data signals have previously been emitted, remains in the acknowledgement receiving state. This control device is thus inhibited for the further emission of data signals. To prevent such an occurrence, it is possible to limit the acknowledgement receiving state of the control devices in time (Proceedings of the Sixth International Conference on

Computer Communication, London, GB, 7th - 10th September 1982, pages 496 - 501, North-Holland Publishing Co., Amsterdam, NL; K. YAGYU et al.: "High throughput optical fiber loop network with effective detection mechanism of lost or duplicated token".) Separate monitoring circuits are required for this purpose in the control devices.

It is then the object of the present invention to indicate an approach how in a method and a circuit arrangement of the type initially mentioned an acknowledgement receiving state assumed by a control device can be timed with little control expenditure.

In a method of the type initially mentioned, the above object is achieved in accordance with the invention by the fact that the maximum period during which a control device is in the acknowledgement receiving state after the emission of data signals is determined by the time of the renewed arrival of the transmit authorization signal at the relevant control device, that on arrival of the acknowledgement signal relating to the relevant control device within the said maximum period, a state enabling a renewed emission of data signals is assumed by the relevant control device, and that if the maximum period has elapsed before arrival of the acknowledgement signal relating to the relevant control device, this control device is switched to an error signalling and/or error processing state.

The invention has the advantage that no separate time generator devices are necessary in a control device for timing the acknowledgement receiving state assumed by this control device but that the occurrence of the transmit authorization signal transmitted via the loop system is here evaluated for determining the duration of the existence of an acknowledgement receiving state. A further advantage of the invention is that a control device which is in the acknowledgement receiving state is first switched into an error signalling and/or error processing state when an expected acknowledgement signal fails to arrive within the maximum predetermined period of time. In this manner, it is possible to initiate

measures for error detection within the relevant control device or within the entire loop system within the shortest possible time.

5 For carrying out the method according to the invention in a circuit arrangement comprising control devices interconnected via a clock-controlled loop system which is direction-dependently operated, which control devices in each case emit, as transmitting devices, to the loop system any data signals which may have to be
10 transmitted after reception of a transmit authorization signal, and which control devices in each case accept, as receiving devices, data signals intended for them and transmitted via the loop system, and emit to the loop system an acknowledgement signal corresponding to these
15 data signals for the relevant transmitting device, it is advantageous to construct the circuit arrangement in such a manner that each of the control devices exhibits a transmitting sequence control which switches the associated control device, after emission of data signals,
20 first into the acknowledgement receiving state and, following a renewed arrival of a transmit authorization signal before the arrival of the expected acknowledgement signal, from this into an error signal and/or error processing state, and that in each of the control devices
25 an acknowledgement signal receiver is provided which, following the arrival of an acknowledgement signal, admits an acknowledgement confirmation signal to the associated transmit sequence control, on the basis of which this transmit sequence control switches the associated control device, which is in an acknowledgement
30 receiving state, into a state enabling a renewed emission of data signals. The advantage of this circuit arrangement consists in the fact that in each case separate devices, namely a transmit sequence control and an acknowledgement signal receiver, are provided for monitoring the occurrence of transmit authorization signals and acknowledgement signals in the control devices. Thus, the control expenditure in control devices which are in an
35 acknowledgement receiving state is kept low.

The control expenditure in the individual control devices can in particular be kept low if the transmit sequence control in each case associated with the control devices exhibits a microprocessor arrangement which is provided with a plurality of interrupt control inputs, if a first one of the interrupt control inputs is connected to an arrangement for receiving transmit authorization signals, which, on the occurrence of a transmit authorization signal, emits a corresponding control signal to the relevant interrupt control input, and if a further interrupt control input is connected to the previously mentioned acknowledgement signal receiver for emitting an acknowledgement confirmation signal.

The acknowledgement signal receiver can be implemented with relatively low circuit expenditure if a decoding device and a register, which is connected to the microprocessor arrangement, is provided as acknowledgement signal receiver which, on occurrence of an acknowledgement signal intended for the respective control device, accepts this signal for an evaluation by the microprocessor arrangement and, following this acceptance, emits an acknowledgement confirmation signal at a control output.

In the text which follows, the invention will be explained in greater detail by way of example with reference to drawings, in which:

Figure 1 shows a block diagram of a data switching system formed of a loop system in which the invention is used,

Figure 2 shows a block diagram of the structure of one of the interface circuits, only diagrammatically shown in Figure 1, and the structure of one of the switching units or line termination units,

Figure 3 shows the structure of a transmit buffer arrangement in each case present in the interface circuits,

Figure 4 shows the structure of a device for receiving a transmit authorization signal,

Figure 5 shows the structure of a transmit buffer

control device, and

Figure 6 shows the structure of a receive buffer arrangement in each case present in the interface circuits.

5 Figure 1 shows a data switching system having a plurality of switching units SU0 to SUn. These switching units carry out the switching functions required for transmitting data signals in accordance with the principle of load division. For this purpose, the switching
10 units are jointly connected to a loop system. Such a loop system can consist of a single closed ring conductor arrangement. However, such a loop system can also be constructed, for example, as shown in Figure 1, of two parallel mutually independent ring conductor arrangements
15 RING0 and RING1. When one of the ring conductor arrangements fails, for example, such redundancy makes it possible to transmit data signals on the other ring conductor arrangement in each case.

 The said switching units SU0 to SUn are in each
20 case connected to the two ring conductor arrangements via an interface circuit RA which is separate for each of the ring conductor arrangements and which will be discussed in still greater detail in the text following.

 The said ring conductor arrangements RING0 and
25 RING1 are also connected to a plurality of line termination units TU0 to TUK, in each case again via an interface circuit RA which is separate for each of the ring conductor arrangements. Together with the associated interface circuits, these line termination units are used
30 for the data signal transmission between the switching units and transmission lines connected to subscriber devices, which transmission lines are connected to the line termination units. Each of the line termination units exhibits a plurality of line terminations LTO to
35 LTm for connecting such transmission lines.

 The circuit units formed of the said switching units or the line termination units, respectively, and the associated interface circuits will also be called control devices in the text following. In the case where

the loop system only consists of a single ring conductor arrangement, only a single interface circuit is associated with a control device.

Within the switching system shown in Figure 1, that is to say between the switching units and the line termination units, data signals are transmitted in the form of data signal blocks which in each case exhibit, as data signals, signalling information items in the course of the establishment of a connection, and when a connection is set up, the message signals to be transmitted between the subscriber devices in question. In this arrangement, each data signal block to be transmitted contains, in addition to the actual data signals which are in each case formed of a plurality of bits, for example 8 bits, at least one receiver address designating a control device selected as receiver, start and end identification codes designating the beginning and the end of a data signal block; a transmitter address designating the respective control device as transmitter and a prepared acknowledgement signal. A data signal block structured in this manner can only be emitted to one of the ring conductor arrangements if previously a transmit authorization signal has been received by this control device which signal is transmitted from control device to control device and in each case switches the latter into a transmit state.

Figure 2 shows the structure of a control device in greater detail. As has already been mentioned above, such a control device consists either of a switching unit or of a line termination unit, indicated by the designation SU/TU in Figure 2, and of a number of interface circuits corresponding to the number of ring conductor arrangements. In this connection, Figure 2 shows only one of these interface circuits since all interface circuits connected to the switching units or line termination units have the same internal structure.

The unit (switching unit or line termination unit), a section of which is shown and which is designated by SU/TU in Figure 2, exhibits a microprocessor

arrangement controlling both transmitting and receiving processes. Of this microprocessor arrangement, a microprocessor MP and a memory arrangement MEM comprising read-only memories (program memories) and read/write memories, which are connected to the microprocessor via a bus system, are shown. In this arrangement, the bus system consists of a data bus DB, an address bus AB and a control bus SB. The interface circuit RA is also connected to the microprocessor MP via the data bus and the address bus and via the lines of the control bus designated by WR and SA. Furthermore, two control lines of the interface circuit lead to interrupt inputs INTn-1 and INTn of the microprocessor MP.

The interface circuit RA can be divided into two circuit sections, namely into a transmit section for emitting data signal blocks to the associated ring conductor arrangement and into a receive section for accepting data signal blocks from the associated ring conductor arrangement. In the text which follows, the receive section will first be discussed.

At the interface to the associated ring conductor arrangement, a receive register Reg1 is provided into which signals, transmitted in parallel form via the ring conductor arrangement, are transferred under the control of a clock generator, not shown, which emits clock pulses T. Incidentally, the clock pulse sequence is adapted to the transmission rate in the ring conductor arrangement. The signals just mentioned are in each case a predetermined number of data signals and a transmit authorization signal which is transmitted on a separate line designated by SBE. This transmit authorization signal can be formed by a predetermined state of a binary signal which occurs for a particular period of time.

At the output end, the input register Reg1 is connected with its outputs carrying the data signals to, on the one hand, a receive buffer arrangement EP and, on the other hand, an acknowledgement signal receiver. The latter is formed of an address decoder DEC and an acknowledgement register Reg2. In this arrangement, the

inputs of the two are connected to the outputs of the input register Reg1 just mentioned. The output of the address decoder is connected to a clock input of the acknowledgement register. This acknowledgement register, in turn, exhibits data signal outputs which are connected to the data bus DB already mentioned. In addition, a control line of the acknowledgement register Reg2 leads towards the interrupt input INTn-1 of the microprocessor MP.

As will be explained in still greater detail in the text following, the said receiver buffer arrangement EP is used for accepting data signal blocks intended for the respective control device and for forwarding data signal blocks intended for other control devices connected to the ring conductor arrangement. At the output end, this receiver buffer arrangement is connected, on the one hand, to the data bus DB already mentioned, and, on the other hand, to first inputs of a data selector DW1 and via a line arrangement QS to inputs of a register Reg3.

The transmit section of the interface circuit RA exhibits a transmit buffer arrangement SP which is supplied with signals from the previously mentioned microprocessor arrangement via the data bus DB, the address bus AB and via the lines WR and SA of the control bus SB. Furthermore, an input of the transmit buffer arrangement is connected to the output, carrying the transmit authorization signal, of the input register Reg1 via a line designated by SBE'. Finally, the transmit buffer arrangement SP is supplied with the clock signals T at a further input.

The transmit buffer arrangement SP is connected with data signal outputs to further inputs of the previously mentioned data selector DW1 via a line arrangement SD. Among other things, this data selector is controlled by a control signal occurring on a line designated by SL1 from the transmit buffer arrangement. For this purpose, the data selector is connected with a control input via an OR gate GO to the line SL1.

The last-mentioned inputs of the data selector DW1 are also connected to the data signal outputs of the register Reg3, the input of which is connected to the line arrangement QS. A control output of this register is connected via a line designated by SL2 and the OR gate GO to the control input of the data selector DW1.

At the output end, the data selector DW1 is connected to data signal inputs of an output register Reg4 which is provided at the interface to the associated ring conductor arrangement and which is controlled by the clock pulses T. A further input of this register is connected via a line designated by SBA' to an output of the transmit buffer arrangement SP which carries a transmit authorization signal to be forwarded. The output end of the output register Reg4 is connected to the associated ring conductor arrangement. Incidentally, the line SBA' is also connected to the interrupt input INTn of the microprocessor MP. Finally, the transmit buffer arrangement is also connected to the control bus SB via a line SA'.

With respect to the receive buffer arrangement EP and the acknowledgement register Reg2, it should also be pointed out that, in addition to being connected to the data bus DB, these are also connected to the address bus AB and the control bus SB, in each case for activation from the microprocessor MP. However, the respective connections are not shown in order to simplify Figure 2.

In the text which follows, the interaction of the circuit sections shown in Figure 2 during the transmission of data signals will first be explained before the structure of the receive buffer arrangement EP and of the transmit buffer arrangement SP is discussed in greater detail.

It will first be assumed that data signals are to be transmitted from the control device shown in Figure 2 to another control device. For this purpose, the microprocessor arrangement first assembles the data signals, which in each case consist of a predetermined number of bits, to form at least one data signal block, the actual

data signals being preceded by a start identification code identifying the start of a data signal block and by a receiver address designating the control device selected as receiver. A data signal block assembled in this manner is subsequently transferred word by word into the transmit buffer arrangement SP, controlled by write pulses transmitted via the line WR. In this context, a word is understood to be a predetermined number of bits which is simultaneously transmitted in the form of a parallel character to the transmit buffer arrangement. For example, a word can consist of 16 bits, that is to say of two data signals if each data signal consists of 8 bits.

After the word-by-word transmission of a data signal block, the microprocessor arrangement then emits a transmit request signal to the transmit buffer arrangement SP via the line SA. However, this signal initially remains unconsidered in the transmit buffer arrangement until a transmit authorization signal occurs which reaches the transmit buffer arrangement via the input register Reg1 and the line SBE'. After the occurrence of a transmit authorization signal, however, the data signal block which is now stored in the transmit buffer arrangement is emitted word by word to the associated ring conductor arrangement via the output register Reg4. During this process, an end identification code indicating the end of a data block and a transmitter address designating the control device transmitting the data signal block is still attached to the data signal block and an acknowledgement signal prepared for the receiver is appended. Subsequently, the transmit buffer arrangement SP then forwards the previously received transmit authorization signal via the line SBA' to the output register Reg4 which emits this transmit authorization signal to the ring conductor arrangement.

After the emission of the transmit authorization signal, which is indicated to the microprocessor MP by means of a signal on line SA', the control device concerned first goes into an acknowledgement receiving state

in which only receiving processes can be handled and in which the interrupt input INTn of the microprocessor is enabled.

5 In the normal case, the acknowledgement receiving state is maintained up to the arrival of an acknowledgement signal which is emitted by the control device considered as receiver following the reception of the data signal block just transmitted. The acknowledgement signal here is the prepared acknowledgement signal already mentioned which is transmitted in the data signal block and which is modified in the control device considered as receiver. Due to this modification, the transmitter is supplied with information concerning the reception of the data signal block transmitted. For 10 example, the error-free transmission of a data signal block can be indicated by an acknowledgement signal modified in a particular manner. 15

A modified acknowledgement signal has attached to it the address of the transmitter of the data signal block just received and the end identification code associated with the data signal block. In this connection, the address and the end identification code are taken from the received data signal block. 20

The occurrence of an acknowledgement signal is now monitored with the aid of the acknowledgement signal receiver already mentioned. For this purpose, the associated address decoder DEC continuously compares the signals occurring at the output of the input register Reg1 (Figure 2) with a signal consisting of the address allocated to the control device concerned and of the specified end identification code. If during this process the address decoder determines a match, it outputs a control signal at its output. When this control signal occurs, the acknowledgement signal transmitted following 25 the address and the end identification code is transferred into the acknowledgement register Reg2. 30 35

Following the acceptance of the acknowledgement signal, the acknowledgement register emits an acknowledgement confirmation signal via its control output to

the microprocessor MP. In consequence, the latter accepts for subsequent evaluation the acknowledgement signal just stored in the acknowledgement register. During this evaluation, the microprocessor then switches the associated control device from the acknowledgement receiving state to a state in which a renewed emission of a data signal block is possible. In this connection, it depends on the evaluation of the acknowledgement signal whether any further data signal block present for transmission is transmitted or whether measures for error processing such as, for example, measures for the renewed transmission of the data signal block previously emitted, are initiated when a transmission error has been detected. Incidentally, the interrupt input INTn is inhibited in this state.

In addition, the arrival of the transmit authorization signal is continuously monitored in the control devices, namely in the associated transmit buffer arrangement SP. Following the occurrence of the transmit authorization signal, the latter arrangement emits a control signal to the interrupt input INTn of the microprocessor MP. If the acknowledgement signal expected by a control device currently in an acknowledgement receiving state has not arrived in this control device before the emission of this control signal, the microprocessor MP switches the associated control device into an error signalling and/or error processing state. In this state, measures for error processing are initiated, if necessary, in addition to an error message. These measures have the consequence that, for example, all devices of the switching system included in the transmission of the data signal block which has not been acknowledged, that is to say the two control devices in question and the ring conductor arrangement used for the transmission, are checked step by step. If, for example, this check shows that the ring conductor arrangement concerned or the interface circuits RA connected to it are not operating without errors, the error processing may consist of changing over to the ring conductor arrangement hitherto

not used for transmitting data signal blocks. If, in contrast, central parts of the control devices involved in the transmission are not operating without errors, the error processing can amount to the respective control device being excluded from any further data signal transmission.

In the text which follows, the control processes occurring in a control device when a data signal block is received will be explained. As has already been mentioned above, the receive buffer arrangement EP is provided for accepting data signal blocks. When a start identification code designating the start of a data signal block occurs, this arrangement compares the receiver address transmitted at the beginning of the data signal block with an address allocated to the relevant control device. When the addresses compared with one another match, the signals belonging to the data signal block are transferred into the memory arrangement until an end identification code occurs which indicates the end of the data signal block. They will initially remain in this arrangement until they are transferred by the microprocessor arrangement of the unit SU/TU (Figure 2). In this connection, the transfer can occur, for example, following a control signal emitted by the receive buffer arrangement when the end identification code occurs. For this purpose, the control signal can be supplied to the microprocessor at a further interrupt input, for example the input INT1.

Before a data signal block is transferred, a check with regard to its error-free transmission is still carried out in the receive buffer arrangement EP, for example in the form of a parity check. During this process, the receive buffer arrangement modifies the acknowledgement signal transmitted in the data signal block and prepared by the transmitter of the data signal block in accordance with the result of the check and then transfers this modified acknowledgement signal together with the address designating the transmitter of the data signal block just received and the end identification

code to the register Reg3. In this process, end identification code and address are taken from the received data signal block. The register Reg3 then forwards the transferred signal via the data selector DW1 and the output register Reg4 to the ring conductor arrangement. For this purpose, the data selector DW1 is appropriately controlled via the line SL2 from the register Reg3.

If, in contrast, the receive buffer arrangement EP determines a non-correspondence of the addresses compared with one another when a start identification code of a data signal block occurs, the receive buffer arrangement forwards the data signal block unchanged to the data selector DW1. The data signal block then passes back to the ring conductor arrangement via this data selector and the output register Reg4 following it, and thus to the next control device in the ring conductor arrangement.

In the text which follows, the structure of the transmit buffer arrangement SP and of the receive buffer arrangement EP will also be discussed. Figure 3 shows a block diagram of the transmit buffer arrangement. It exhibits, among other things, a transit store FIFO1, the data signal inputs of which are connected to the data bus DB. This transit store, which is also called first-in-first-out store, is used for aforementioned word-by-word acceptance of a data signal block provided by the microprocessor arrangement of the SU/TU unit and for forwarding it to the ring conductor arrangement following the occurrence of a transmit authorization signal. The read and write processes required for this are controlled from a buffer control device PS shown in Figure 5 which is connected to the transit store via the lines WR1, RD and FE. In this arrangement, the WR1 and RD lines are used for transmitting write pulses and read pulses, respectively. The transit store emits a control signal indicating its empty state via the line FE.

The data signal outputs of the transit store FIFO1 are connected to the data signal inputs of a register Reg5. This register, the output of which is

connected to the line arrangement designated by SD in Figure 2 is connected with a clock input via the line RD previously mentioned and with an input, used for enabling its data signal outputs, via the line EN1 to the buffer control device PS.

In addition, the transmit buffer arrangement SP exhibits two further registers Reg6 and Reg7. The data signal outputs of these registers are in each case connected to the previously mentioned line SD. For enabling these data signal outputs, each register again exhibits a control input which can be controlled via a line EN2 or EN3, respectively, from the buffer control device PS. In this connection, the register Reg6 is used for providing the transmit address and end identification code to be transmitted in a data signal block. These information items are supplied to the input of this register via the data bus DB. The transmitter address and end identification code are transferred with the aid of a write pulse which is emitted by the buffer control device via the line WR2. The prepared acknowledgement signal previously mentioned is stored in the register Reg7.

For controlling write processes in the transit store FIF01, the buffer control device PS is connected to the address bus AB and the line WR via which address signals and write pulses, respectively, are transmitted.

For controlling read processes in the transit store and in the registers Reg5, Reg6 and Reg7, in contrast, the buffer control device is connected, on the one hand, for transferring clock pulses, to the line T already shown in Figure 2 and, on the other hand, to a line RF. Via this line, the buffer control device PS is supplied from a device, shown in greater detail in Figure 4, for receiving a transmit authorization signal SBS, with an enable signal for reading out a data signal block stored in the transit store FIF01. This device SBS is connected to the lines SBE', SL1 and SBA' shown in Figure 2. In addition, it is connected via a line SA' to the output of a flip flop stage FF1 which is supplied at its

clock input with the previously mentioned transmit request signal via the line SA from the microprocessor MP. Finally, a reset input of this flip flop stage is connected to the buffer control device PS via the line RS. Incidentally, the line SA' is also connected to the control bus SB.

The following control processes occur in the transmit buffer arrangement SP shown in Figure 3. For the word-by-word transfer of a data signal block into the transit store FIF01, write pulses are emitted from the microprocessor MP in conjunction with address signals designating the transit store to the buffer control device PS. The latter forwards the write pulses to the transit store. The data signal block transferred word by word with the aid of these write pulses initially remains stored in the transit store. After this transfer of the data signal block, the microprocessor finally also emits via the line SA a transmit request signal which switches the flip flop stage FF1 into the active state.

Due to this active state of the flip flop stage FF1, the presence of a data signal block to be transmitted is indicated to the device for receiving a transmit authorization signal SBS. If then this device subsequently receives a transmit authorization signal, it emits a corresponding signal via the line RF to the buffer control device PS which thereupon applies read pulses occurring in the clock pattern of the clock pulses T to the transit store FIF01 and the register Reg5. In addition, the buffer control device also outputs an enable signal for the data signal outputs of the register Reg5. By this means, the data signal block now stored in the transit store FIF01 is read out word by word and forwarded to the ring conductor arrangement via the register Reg5 and the data selector DW1. For this purpose, the data selector is appropriately controlled by the device SBS.

The reading-out mentioned above now occurs until, following the reading-out of the last data signal belonging to the data signal block, a signal indicating the

empty state of the transit store FIFO1 is emitted by the latter via the line FE to the buffer control device PS. This signal has the effect that the data signal outputs of the register Reg5 are inhibited from the buffer control device and thereupon first the data signal outputs of the register Reg6 and subsequently the data signal outputs of the register Reg7 are enabled for one clock pulse T in each case. By this means, the transmitter address including the end identification code and the prepared acknowledgement signal are still appended to the data signal block just transmitted, as already mentioned above. After the emission of the acknowledgement signal, the flip flop stage FF1 is reset into its inactive state from the buffer control device PS. This resetting has the effect that the transmit authorization signal received by the device SBS is forwarded via the line SBA' to the ring conductor arrangement and a control signal indicating this forwarding is emitted to the microprocessor MP via the line SA'.

Figure 4 shows the structure of the device for receiving a transmit authorization signal SBS. This device exhibits a so-called RS flip flop FF2, the set input S of which is connected to an output of an AND gate G1 negating an output signal. This AND gate is connected with one input to the line SBE' carrying the transmit authorization signal and with a further input to the line SA', the latter also being connected to the reset input of the flip flop FF2. Both lines are also connected to inputs of an AND gate G2, in which arrangement the input connected to the line SA' negates the input signal supplied to it. At the output end, this AND gate is connected to an input of an OR gate G3. A further input of this OR gate is connected to the output of a monostable flip flop MV which, in turn, is connected with its input to the output of the previously mentioned RS flip flop FF2. At this output, the lines SL1 and RF (Figure 3) are also connected.

The arrangement shown in Figure 4 always immediately forwards a transmit authorization signal, occurring

on the line SBE' via the AND gate G2 and the OR gate G3 to the output register Reg4 shown in Figure 2, whenever the flip flop FF1 is in its inactive state, that is to say when no transmit request signal has been previously emitted by the microprocessor. If, in contrast, the flip flop FF1 is in its active state, the transmission path specified above is inhibited for the transmit authorization signal. When a transmit authorization signal arrives, the flip flop FF2 is switched to its active state in which the abovementioned enable signal occurs on line RF for reading out a data signal block stored in the transit store FIFO1. In addition, a control signal is emitted to the data selector DW1 (Figure 2) via line SL1 in this state.

Resetting the flip flop FF1 into its inactive state after the transmission of a data signal block has the effect that the flip flop FF2 is also switched to its inactive state. During this transition, the monostable flip flop MV following the flip flop FF2 emits an output signal of predetermined duration which is forwarded as transmit authorization signal via the OR gate G2.

Figure 5 shows the structure of the buffer control device PS. According to this, the buffer control device exhibits a decoder DEC2, the input of which is connected to the address bus AB and the line WR. Depending on the address signals present on the address bus, the decoder forwards the write pulses transmitted on the line WR either to the line WR1 or to the line WR2.

The buffer control device PS also exhibits an AND gate G4 which emits clock pulses T as read pulses to the line RD when the abovementioned enable signal is present on the line RF. The output of this AND gate is also connected to clock inputs of two series-connected flip flops FF3 and FF4. The non-negating output of the flip flop FF3 in this arrangement is directly connected to the data signal input of the flip flop FF4. The data signal input of the flip flop FF3 is connected to the output of an AND gate G6. At the input, this AND gate is connected, on the one hand, to the line FE shown in Figure 3 and, on

the other hand, to the output, which negates the output signal, of the flip flop FF3. This output is also connected to the line EN2. The flip flop FF4 is connected with its output not negating the output signal to the line RS and with its output negating the output signal to the line EN3. The abovementioned line FE is finally also connected to an inverter G5, the output of which is connected to the line EN1.

When a signal indicating the empty state of the transit store FIFO1 occurs, the circuit arrangement just explained and consisting of the AND gate G6, the two flip flops FF3 and FF4 and the inverter G5 first emits an inhibit signal for inhibiting the data signal outputs of the register Reg5 and subsequently in each case an enable signal for the data signal outputs of the registers Reg6 and Reg7. In addition, a signal effecting the resetting of the flip flop FF1 is also provided by the flip flop FF4.

Figure 6 shows the structure of the receive buffer arrangement EP previously mentioned. This arrangement exhibits a comparator arrangement Vg1 which is connected to the data signal outputs of the input register Reg1 (Figure 2) for the abovementioned address comparison and which emits a set signal to a flip flop FF5 when the address compared matches. The output of this flip flop is connected to an input of an AND gate G7. This AND gate is supplied at a further input with the clock pulses T as write pulses. The output of this AND gate G7 is connected to a write pulse input of a store FIFO2. This store is, for example, a transit store which is connected with its data signal outputs to the data bus DB. Into this transit store, the data signal block is transferred word by word with the aid of the clock pulses T transferred via the AND gate G7 when an abovementioned set signal is present. In this connection, data signal words are transferred until the flip flop FF5 is reset to its inactive state by the occurrence of the end identification code indicating the end of the data signal block. For the purpose of this resetting, the flip flop FF5 is connected to the line EK

carrying the end identification code at the input of the transit store. This line is also connected to a further flip flop FF6 which emits at its output the previously mentioned control signal indicating the availability of a data signal block to the microprocessor MP following the occurrence of the end identification code. The reading-out of a data signal block out of the transit store FIFO2 will not be discussed in greater detail here. This reading-out is effected in a familiar manner by supplying corresponding control signals via lines of the control bus SB. In this connection, the reading-out is terminated with the occurrence of a signal indicating the empty state of the transit store. This signal is supplied to the microprocessor MP from the transit store FIFO2, for example in the form of a control signal via the control bus SB or as interrupt signal at an interrupt input.

The input of the transit store FIFO2 is connected to a device SB for checking received data signal blocks. This device checks received data signal blocks with respect to their error-free transmission, for example in the form of a parity check. During this process, it modifies the acknowledgement signal, prepared by the transmitter and contained in a received data signal block, in accordance with the result of the check and subsequently emits this modified acknowledgement signal together with the address designating the transmitter of the data signal block just received and with the end identification code to the register Reg3.

Finally, the transit store FIFO2 is also preceded by a data selector DW2. This data selector is controlled from the abovementioned comparator arrangement Vg1. It only forwards data signal words belonging to a data signal block to the transit store when the comparator arrangement has found a match of the addresses compared with one another. Otherwise, the entire received data signal block is forwarded to the associated ring conductor arrangement via the data selector DW1 shown in Figure 2 and the output register Reg4.

In the text above, Figures 2 and 6 were used for explaining that in each case two separate address decoders, namely the address decoder DEC and the comparator arrangement Vgl, are provided for the reception of acknowledgement signals and data signal blocks in the control devices. Instead of these two address decoders, however, it is also possible to use a single address decoder which is supplied, in addition to the lines carrying the addresses, also with lines carrying the start identification code and end identification code for detecting acknowledgement signals and data signal blocks.

List of reference designations

	AB	Address bus
	DB	Data bus
	DEC, DEC2	Address decoder
5	DW1, DW2	Data selector
	EN1, EN2, EN3	Line
	EK	Line
	EP	Receive buffer arrangement
	FE	Line
10	FF1, ..., FF6	Flip flop
	FIFO1, FIFO2	Transit store
	GO, G3	OR gate
	G1, G2, G4, G6, G7	AND gate
	G5	Inverter
15	INTn-1, INTn	Interrupt input of the microprocessor MP
	LTO, LTm	Line termination
	MEM	Memory arrangement
	MP	Microprocessor
20	MV	Monostable flip flop
	PS	Buffer control device
	QS	Line arrangement
	RA	Interface circuit
	RD	Line
25	Reg1	Input register
	Reg2	Acknowledgement register
	Reg3, Reg5, Reg6, Reg7	Register
	Reg4	Output register
	RF	Line
30	RING0, RING1	Ring conductor arrangement
	RS	Line
	S	Set input of flip flop FF2
	SA, SA'	Line of control bus SB
	SB	Control bus
35	SBA'	Line
	SBE'	Line
	SBS	Device for receiving a transmit authorization signal
	SD	Line arrangement

	SL1, SL2	Line
	SP	Transmit buffer arrangement
	SUo, ..., SUn	Switching unit
	T	Clock
5	TUo, ..., TUn	Line termination unit
	Vgl	Comparator arrangement
	WR	Line of control bus SB
	WR1, ..., WR2	Line

Patent claims.

1. Method for transmitting data signals between control devices (SUO, RA;... SUn, RA; TUO, RA; TUK, RA) interconnected via a clock-controlled loop system (RING0, RING1) which is direction-dependently operated, which control devices are formed, in particular, by control devices of a data switching system, in which method a transmit authorization signal is transmitted via the loop system from control device to control device, which signal controls these devices in each case to assume a transmit authorization state, the respective control device emitting to the loop system data signals to be transmitted by it, together with a receiver address designating a desired control device, before forwarding the transmit authorization signal, and in which method a control device which is designated by the receiver address transmitted together with the data signals accepts these data signals for further processing and emits an acknowledgement signal, to be forwarded via the loop system, which is intended for that control device which is in an acknowledgement receiving state and from which the data signals have been emitted, characterized in that the maximum period during which a control device is in the acknowledgement receiving state after the emission of data signals is determined by the time of the renewed arrival of a transmit authorization signal at the relevant control device, that on arrival of the acknowledgement signal relating to the relevant control device within the said maximum period, a state enabling a renewed emission of data signals is assumed by the relevant control device, and that if the maximum period has elapsed before arrival of the acknowledgement signal relating to the relevant control device, this control device is switched to an error signalling and/or error processing state.

2. Circuit arrangement for carrying out the method according to Claim 1, comprising control devices (SUO, RA;...TUK, RA) interconnected via a clock-controlled loop



system (RING0, RING1) which is direction-dependently operated, which control devices in each case emit, as transmitting devices, to the loop system any data signals which may have to be transmitted after reception of a transmit authorization signal, and which control devices in each case accept, as receiving devices, data signals intended for them and transmitted via the loop system, and emit to the loop system an acknowledgement signal corresponding to these data signals for the relevant transmitting device, characterized in that each of the control devices (SUO, RA;...TUK, RA) exhibits a transmitting sequence control (MP, SP) which switches the associated control device, after emission of data signals, first into the acknowledgement receiving state and, following a renewed arrival of a transmit authorization signal before the arrival of the expected acknowledgement signal, from this into an error signal and/or error processing state, and that in each of the control devices an acknowledgement signal receiver (DEC, Reg 2) is provided which, following the arrival of an acknowledgement signal, emits an acknowledgement confirmation signal to the associated transmit sequence control, on the basis of which this transmit sequence control switches the associated control device, which is in an acknowledgement receiving state, into a state enabling a renewed emission of data signals.

3. Circuit arrangement according to Claim 2, characterized in that the transmit sequence control exhibits a microprocessor arrangement (MP, MEM) which is provided with a plurality of interrupt control inputs (INT1 to INTn), that a first one of the interrupt control inputs (INTn) is connected to an arrangement (SBS) for receiving transmit authorization signals, which, on the occurrence of a transmit authorization signal, emits a corresponding control signal to the relevant interrupt control input, and that a further interrupt control input (INTn - 1) is connected to the previously mentioned acknowledgement signal receiver (DEC, Reg2) for emitting an acknowledgement confirmation signal.



4. Circuit arrangement according to Claim 2 or 3, characterized in that a decoding device (DEC) and a register (Reg2), which is connected to the microprocessor arrangement (MP, MEM), is provided as acknowledgement signal receiver which, on occurrence of an acknowledgement signal intended for the respective control device, accepts this signal for an evaluation by the microprocessor arrangement and, following this acceptance, emits an acknowledgement confirmation signal at a control output.

