INTERPOLATION AND SCANNING LINE CONVERTING CIRCUIT

The present invention relates to a method of interpolating a digital image signal, to a circuit for interpolating a digital image signal, and to a scanning line converter circuit for a digital image signal.

With the development of digital signal treatment techniques, and the memory-related semiconductor industries, a digital television has been developed which is equipped with an improved resolution by using 3-dimensional signal treatment methods incorporating horizontal, vertical and time axis sampling.

However, as it was inevitable to use high-priced field memory or frame memory means to get the time axis treatment, scanning line conversion techniques employing 2-dimensional signals which have not been treated with the time axis have been used.

That is to say, when a digitally converted image signal has been input, delayed by 1H (1 horizontal line), added to the input image signal, and the resultant multiplied by 1/2, it produces a linearly interpolated interpolation signal that is vertically situated in between the horizontal lines. A scanning line conversion technique has been employed which is made possible by linear interpolation outputting converted scanning lines by way of progressively scanning the said "vertically-linear-interpolated" interpolation signal and input image signal.

Here, the term "progressive scan" means that interlaced-scan image data scans continuously, namely means "non-interlacing".

If the scanning period of 1 horizontal line at

interlaced scan is 63.5μ/sec, the input image signal is produced during 63.5μ/sec, and during the next 63.5μ/sec the linearly interpolated image signal is output.

However, although downfall of horizontally directed resolution is not experienced, the vertically directed resolution drops down.

In other words, if the vertically directed resolution of the existing interlaced scan method is 525/2 LPH (lines per height), the passband following the linear interpolation downgrades to 525/4 LPH.

As evidenced above, one of the disadvantages in the linear interpolation method is the reduction in the vertical resolution.

To remedy this drawback, the slant correlation interpolation can be suggested.

The slant correlation interpolation method involves obtaining the pixel value of the interpolation line using the mean value of pixels with high correlations after detecting the correlation of pixel in the diagonal directions of the right/left and up/down directions, based on the pixels of interpolation lines.

This slant correlation interpolation method can improve resolution slightly in the area of the slope line. However, this method basically cannot prevent a reduction in the vertical direction resolution.

It is an object of the present invention to reduce the drawbacks outlined above.

According to a first aspect of the present invention

there is provided a method of interpolating a digital image signal comprising the steps of forming from said image signal first and second component parts, said first component part being a highpass component and said second component part being a lowpass component, generating a highpass interpolation signal by inserting "0" in said highpass component, generating a lowpass interpolation signal by interpolating said lowpass component, and applying said highpass interpolation signal and said low pass interpolation signal to adding means, the output of said adding means providing an interpolation signal for said digital image signal.

The invention also relates to a circuit for interpolating a digital image signal comprising means for dividing said image signal into first and second component parts, said first component part being a highpass component and said second component part being a lowpass component, an "0" insertion interpolation part arranged to insert "0" in said highpass component to generate a highpass interpolation signal, a further interpolation part arranged to interpolate said lowpass component to generate a lowpass interpolation signal, and first adding means arranged to receive and add said highpass interpolation signal and said lowpass interpolation signal to output an interpolation signal for said digital image signal.

According to a further aspect of the invention there is provided a scanning line converter circuit for a digital image signal comprising an interpolating circuit as defined above, and flxther comprising double speed converter means to which is applied the input image signal and said interpolation signal.

An embodiment of the invention has the advantage of providing an interpolation and scanning line converting

circuit which utilises the original incoming image signal and a 2-dimensional interpolation of image signal that scans the interpolation signal progressively after generating the interpolation signal by way of "0" insertion interpolation at the vertical direction highpass component.

An embodiment of the invention has the advantage of improving the resolution of the slant (slope) line whilst removing the visual disturbance phenomena caused by the structure of scanning line in the interlaced scan method.

An embodiment of the present invention is able to interpolate linearly or do slant correlation interpolation in the vertical direction lowpass component of the incoming image signal and thereby prevent the decline of the vertical resolution.

In an embodiment of an interpolation circuit of the invention said filtering means comprises a vertical bandpass filter arranged to pass as said first component part a vertical direction highpass component of the image signal, said subtracting means being arranged to subtract said vertical direction highpass component from the image signal to produce as said second component part a vertical direction lowpass component, and wherein said further interpolation part comprises a linear interpolation part arranged to generate said lowpass interpolation signal by linear interpolation between the horizontal lines and the vertical direction lowpass component.

In an alternative embodiment, said filtering means comprises a vertical bandpass filter arranged to pass the vertical direction highpass component from the image signal and a horizonal band blanking filter arranged to pass as

said first component part a first interpolation band signal produced by filtering through vertical band blanking the vertical direction highpass component, said subtracting means being arranged to subtract said first interpolation band signal from the image signal to produce as said second component part a second interpolation band signal, and wherein said further interpolation part comprises a slant correlation interpolation part arranged to generate said lowpass interpolation signal by interpolating through slant correlation the second interpolation band signal.

Preferably, the circuit further comprises a matching delay part arranged to delay and match the image signal as much as the amount of group delay of the vertical bandpass filter, the subtracting means being arranged to produce said second component part by subtracting from said delayed image signal.

Preferably, said "0" insertion interpolation part is arranged to generate said highpass interpolation signal by way of "0" insertion interpolation which makes "0" the level of image signal of interpolation line being generated in between 1H delay line and the current incoming lines.

In an embodiment, said circuit further comprises second adding means arranged to restore the original input image signal from said highpass component and the lowpass component output by said first adding means.

A scanning line converter circuit as defined above may be made to output through progressive scanning the original incoming image signal restored from the adder and the interpolation signal at a double speed converter by being equipped with said "0" insertion interpolation part arranged to generate a highpass interpolation signal by

inserting "0" into the vertical direction highpass component from the vertical bandpass filter;

and a further adder which generates interpolation signal by adding lowpass interpolation signal created from the linear interpolation part and the said highpass interpolation signal.

Utilising an interpolation circuit as defined above, the scanning line converter circuit may comprise second adding means to restore the original incoming image signal by adding a first interpolation band signal output from the horizontal band blanking filter of the interpolation circuit and a second interpolation band signal output from the adder of the interpolation circuit; and a double speed converter that outputs through progressive scanning the lowpass interpolation signal coming out of the original input image signal restored from the second adder and the slant correlation interpolation part of the interpolation circuit.

Embodiments of the present invention will hereinafter be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows a general view of a scanning line converting circuit which is not in accordance with the present invention,

Figure 2 is an illustrative view explaining the linear interpolation in Figure 1,

Figure 3 is a frequency characteristic diagram of the interpolation of Figure 1,

Figure 4 shows an exemplary view illustrating slant correlation interpolation,

Figure 5 shows an embodiment of an interpolation circuit of the present invention,

Figure 6 is an illustrative view showing "0" insertion interpolation in Figure 5,

Figure 7 shows a scanning line converting circuit that employs the interpolation circuit of Figure 5,

Figure 8 shows a further embodiment of an interpolation circuit of the present invention,

Figure 9 shows a frequency characteristic diagram of a horizontal band blanking filter as used in the circuit of Figure 8,

Figure 10 is a domain drawing of an interpolation of the circuit of Figure 8, and

Figure 11 shows a scanning line converting circuit employing an interpolation circuit as shown in Figure 8.

Referring to Figure 1, if a digitally converted image signal is input as indicated, the signal R is delayed by 1H at a 1H (1 horizontal line) delay circuit 41 of a linear interpolation part 40. This 1H delayed image signal is added to the input image signal at an adder 42, multiplied

by 1/2 at a multiplier 43 and generates a vertically, linearly, interpolated interpolation signal among the horizontal lines.

The said vertically, linearly, interpolated interpolation signal I and the input image signal R are progressively scanned at a double speed converter 80 and output to converted scanning lines.

The linear interpolation according to Figure 2, is added by the image signal a of 1H delayed line n, and the image signal b of the current input n+2, and then multiplied by 1/2.

Referring to the linear interpolation according to Figure 3, wherein the vertical direction resolution is given as 525/2 LPH (line per height), it will be seen that the passband after the linear interpolation drops to 525/4 LPH.

In the slant correlation interpolation method illustrated in Figure 4, the pixels of the 1H delayed line n are X11, X12, and X13, and the pixels of the current input line n+2 are X31, X32, and X33. Fixing the pixel X22 of the interpolation line n+1 as a base, is a method of obtaining the pixel value of the interpolation line as a mean value of high correlated pixels whereas the correlation of pixel is detected at the diagonal directions in the left and in the right X1, X33, X13, X31, plus at the up and down directions X12, X32.

In other words,

where $|X11-X33| = \epsilon 1$
$|X12-X32| = \epsilon 2$
$|X13-X31| = \epsilon 3$

the method of obtaining the pixel value Y22 of the interpolation line n+1 by averaging as below according to the correlations in the pixels can be determined.

Namely,

where $\epsilon_1 < \epsilon_2, \epsilon_3$, which yields Y22 = (X11+X33)/2....(1)
where $\epsilon_2 < \epsilon_1, \epsilon_3$, which yields Y22 = (X12+X32)/2....(2)
where $\epsilon_3 < \epsilon_1, \epsilon_2$, which yields Y22 = (X13+X31)/2....(3).

Then, the pixel value Y22 of the interpolation line n+1 can be obtained.

Figure 5 is an exemplary view of an interpolation circuit in the present invention. This circuit comprises a vertical bandpass filter 20 which extracts a vertical direction highpass component from the incoming image signal; a matching delay part 10 which delays and matches the incoming image signal as much as the amount of group delay of the vertical bandpass filter 20, and a subtractor 30 which extracts a vertical direction lowpass component by subtracting a vertical direction highpass component extracted from the delayed incoming image signal. The interpolation circuit also comprises a linear interpolation part 40 which is arranged to generate a lowpass interpolation signal by linear interpolation in the horizontal lines as against the extracted vertical direction lowpass component. An "0" insertion interpolation part 50 is arranged to generate an highpass interpolation signal by inserting "0" into the vertical direction highpass component of the vertical bandpass filter 20. A first adder 60 generates an interpolation signal by adding the lowpass interpolation signal and the highpass interpolation signal.

The operation of the interpolation circuit of Figure 5

will now be explained.

Referring to Figure 5, if a digitally converted image signal is input to an image signal input terminal 101, the input image signal at the vertical bandpass filter 20 that goes through a vertical bandpass is to extract a vertical direction highpass component. Simultaneously the said input image signal in passing the matching delay part 10 is delayed as much as the amount of the group delay time of the said vertical bandpass filter. And then, at the subtractor 30 the vertical direction lowpass component is extracted after subtracting the vertical direction highpass component extracted from the said delayed input image signal.

The said extracted vertical direction highpass component becomes a highpass interpolation signal IH being "0" insert interpolated at "0" insertion interpolation part 50, whilst the said vertical direction lowpass component becomes lowpass interpolation IL being linearly interpolated vertically to the horizontal lines at the linear interpolation part 40.

Inasmuch as the said highpass interpolation signal IH and the lowpass interpolation signal IL are added by way of a first adder 60, the interpolation signal I is obtained.

Here, the "0" insertion interpolation, as indicated in Figure 6 denotes that the image signal of interpolation line n+1 that comes in between IH delay line n and the current input line n+2 is levelled to "0".

Figure 7 shows a circuit of a scanning line converting circuit that employs the interpolation circuit of Figure 5. The scanning line converting circuit comprises the vertical

bandpass filter 20 which extracts the vertical direction highpass component at the input image signal. The matching delay part 10 delays the input image signal by the same amount as that imported by the vertical bandpass filter 20. The subtractor 30 forms the vertical direction lowpass component by subtracting the vertical direction highpass component from the delayed input image signal. The linear interpolation part 40 generates the lowpass interpolation signal which is linearly interpolated among the horizontal lines, as opposed to the extracted vertical direction lowpass component. A second adder 70 restores the original input image signal by adding the vertical direction highpass component, which is output by the vertical bandpass filter 20, and the vertical direction lowpass component, which is output by the adder 30. A double speed converter outputs and scans progressively the original input image signal restored from the said second adder 70 and the lowpass interpolation signal output from the linear interpolation part 40.

The vertical bandpass filter 20 shown in Figure 7 comprises a 1H delay circuit 21 arranged to delay by 1 horizontal line the incoming image signal input to image signal input terminal 101. The filter 20 also comprises a 1H delay circuit 23 arranged to delay, also by 1 horizontal line, the image signal which has already been delayed by 1 horizontal line. First and second multipliers 22, 24 multiply by 1/2 respectively the image signal and a further image signal which has been delayed by 2 horizontal lines at the first and second delay circuits 21, 23. A third adder 25 outputs the vertical direction highpass component by adding the image signal delayed by 1 horizontal line at the said first delay circuit 21, and the outputs of the first and second multipliers 22 and 24.

The linear interpolation part 40, as described above,

delays the incoming image signal by 1H at a third 1H delay circuit 41. After adding the input image signal to the image signal delay by 1H at a fourth adder 42, the signal is multiplied by 1/2 at a third multiplier 43. The part 40 generates a lowpass interpolation signal IL by linear interpolation of the vertical direction lowpass component which is the output of the adder 30.

Referring again to Figure 7, a detailed description of the operation of the scanning line converting circuit will now be given.

A digitally converted image signal input to the image signal input terminal 101, is multiplied by -1/2 at the first multiplier 22, and is simultaneously input to the third adder 25, and then, input to the said third adder after being delayed by 1 horizontal line at 1H delay circuit 21.

The image signal delayed by 1 horizontal line at the second 1H delay circuit 23 is also delayed by 1 horizontal line, is multiplied by -1/2 at the second multiplier, and is then input into the third adder 25. The input image signal matches the vertical direction highpass component extracted from the adder 25 inasmuch as it is delayed at the matching delay part 10 by as much as the amount of the group delay of the vertical bandpass filter 20. The vertical direction lowpass component is extracted by subtracting the vertical direction highpass component from the image signal which is delay matched at the subtractor 30. A lowpass interpolation signal IL is output at the linear interpolation part 40 by being linearly interpolated as against the vertical direction lowpass component. Highpass interpolation signal IH is output at the "0" insertion interpolation part 50 by being "0" insert interpolated as opposed to the extracted vertical direction

highpass component.

The interpolation signal at the first adder 60 is generated by adding the lowpass interpolation signal IL output from the linear interpolation part 40 and the highpass interpolation signal IH output from the "0" insertion interpolation part 50. The original input image signal R at the second adder 70 is restored by adding the vertical direction highpass component extracted from the vertical bandpass filter 20 and the vertical direction lowpass component extracted from the adder 30. A double speed converter 80 receives the restored original image signal R and the interpolation signal I and outputs progressive scans. Thus, a scanning line converting circuit utilising an interpolation circuit of the invention can improve the vertical resolution by the use of the highpass interpolation signal and the signal in the next field, whilst still keeping high frequency characteristics intact according to men's visual characteristics. It also eliminates visual disturbance phenomena of the scanning line structure incurred by the linearly interpolated lowpass interpolation signal IL. Meanwhile, referring further to Figure 7, the same operation as described above can be obtained when an "0" insertion interpolation part 50 and the first adder 60 are removed, and the lowpass interpolation signal output from the linear interpolation part 40 is applied to the double speed scanning converter 80 as an interpolation signal I.

As the progressive scan at the double speed scanning converter 80 scans progressively the original image signal R and the interpolation signal I, the insertion of "0" into the vertical direction highpass component can have the identical result or effect with scanning the lowpass interpolation signal IL of the linear interpolation part 40 to the interpolation line in the form of interpolation

signal I.

Figure 8 shows an alternative embodiment of an interpolation circuit in which a vertical bandpass filter extracts a vertical direction highpass component from the input image signal, and a matching delay part 10 delays the input image signal as much as the amount of the delay provided by the vertical bandpass filter 20. A vertical band blanking filter 90 is arranged to extract a first interpolation band signal by "horizontal-band blanking/filtering" the extracted vertical direction highpass component. The subtractor 30 extracts a second interpolation band signal by subtracting the first interpolation band signal from the delayed input image signal. A slant correlation interpolation part 100 generates a lowpass interpolation signal by interpolating in the form of slant correlation the second extracted interpolation band signal. The "0" insertion interpolation part 50 produces a highpass interpolation signal by inserting "0" into the first extracted interpolation signal. The first adder 60 outputs the interpolation signal by adding the lowpass and the highpass interpolation signals.

Figure 9 is a frequency characteristic diagram of a horizontal band blanking filter 90 of Figure 8.

Figure 10 is an interpolation domain drawing of Figure 8, wherein the oblique lined domain K1, K2, is an "0" insertion interpolation domain, and the balance is the slant correlation interpolation domain.

The embodiment illustrated in Figure 8 is explained below in detail with reference to the frequency characteristic drawing in Figure 9 and the interpolation domain diagram of Figure 10.

Once the digitally converted image signal is input to the image signal input terminal 101 of the circuit of Figure 8, the input image signal is filtered through the vertical bandpass at the vertical bandpass filter 20 which extracts the vertical direction highpass component. Simultaneously the input image signal is delayed at the matching delay part 10 by the same amount as the delay introduced by the vertical bandpass filter 20. And, at the vertical band blanking filter 90, and "0" insertion interpolation domain which are the areas K1, K2, shown in oblique lines in Figure 10, only extracts the first interpolation band signal. Here, the frequency characteristic of the said horizontal band blanking filter 90 is shown in Figure 9 whilst the reference P denotes the passband and S shows the stop band.

At the adder 30, the slant correlation interpolation domain which excludes the "0" insertion interpolation area, in other words, the portion that rules out oblique lined areas K1, K2, extracts the second interpolation band signal.

The extracted first interpolation band signal being interpolated by the "0" insertion becomes a highpass interpolation signal IH at the "0" insertion interpolation part 50, whilst the second interpolation band signal being interpolated by the slant correlation becomes a lowpass interpolation signal IL at the slant correlation interpolation part 100.

The first interpolation band signal experiencing a slant correlation interpolation in the highpass component which is separated from the vertical bandpass filter 20 becomes a signal being excluded of a band signal that enhances resolution.

The second interpolation band signal which is interpolated through slant correlation becomes a vertical direction lowpass component to improve resolution of the slant area, and a vertical direction highpass signal excepted from the first interpolation band signals K1, K2.

Therefore, resolution improvement at the slant part along with the prevention of resolution drop in the "0" insertion interpolation domain can be achieved.

Figure 11 is a drawing of a scanning line converting circuit that employs an interpolation circuit as shown in Figure 8 and which comprises the vertical bandpass filter 20 which extracts the vertical direction highpass component from the incoming image signal. The matching delay part 10 is provided to match the delay at the vertical bandpass filter 20. The horizontal band blanking filter 90 is arranged to extract the first interpolation band signal by blank filtering the vertical highpass component at a horizontal band. The subtractor 30 extracts the second interpolation band signal by subtracting the first interpolation band signal extracted from the delayed input image signal. The slant correlation interpolation part 100 generates the lowpass interpolation signal by interpolating, through slant correlation, the second interpolation band signal. The second adder 70 restores the original input image signal by adding the first interpolation band signal (which is the output of the horizontal band blanking filter 90) and the second interpolation bandpass signal (which is the output of the subtractor 30). Finally, the double speed converter 80 outputs through progressive scanning a lowpass interpolation signal that is coming out of the slant correlation interpolation part 100 and the original input image signal restored from the adder 70.

The vertical bandpass filter 20 in Figure 11 comprises the 1H first delay circuit 21 that delays by 1 horizontal line the input image signal coming from the image signal input terminal 101. The second 1H delay circuit 23 which delays again by 1 horizontal line the image signal which is already delayed by 1 horizontal line. The first and second multipliers 22, 24 which multiply by -1/2 respectively the image signals which are delayed by 2 horizontal lines at the input signal and by the 1H delay circuits 1, 2, 21 and 23. The third adder 25 arranged to output a vertical direction highpass component by adding an image signal delayed by 1 horizontal line at the above 1H delay circuits 1 and 21 to the output of the first and second multipliers 22, 24.

The horizontal band blanking filter 90 comprises a delay circuit 91 which delays by 4 pixels the vertical direction highpass component output from the third adder 25 of the vertical bandpass filter 20. A fourth adder 92 which adds the currently incoming vertical direction highpass component from the third adder 25 of the vertical bandpass filter 20 and the vertical direction highpass component delayed by 4 pixels at the delay circuit 91. A third multiplier 93 which averages the vertical direction highpass component value by multiplying by 1/2 the vertical direction highpass component value which was added to the fourth adder 92.

A detailed explanation of the scanning line converting circuit shown in Figure 11 will now be given.

Once the digitally converted image signal is input to the input terminal 101, the vertical bandpass filter 20 filters the incoming image signal by way of the vertical bandpass filter and extracts a vertical direction highpass component. The matching delay part 10 matches and delays

the incoming image signal as much as the amount of the delay of the vertical bandpass filter 20. The horizontal band blanking filter 90 extracts a first interpolation band signal by blank filtering through the horizontal band the vertical direction highpass component extracted from the vertical bandpass filter 20. The adder 30 extracts a second interpolation band signal by subtracting the first interpolation band signal (which is extracted out of the horizontal band blanking filter 20) from the input image signal which is delayed at the matching delay part 10.

The slant correlation interpolation part 100 generates a lowpass interpolation signal IL by interpolating through a slant correlation the extracted second interpolation band signal. An "0" insertion interpolation part 50 generates a highpass interpolation signal IH by inserting "0" into the first extracted interpolation band signal. The first adder 60 generates the interpolation signal I by adding a lowpass interpolation signal I generated from the slant correlation interpolation part 100 and a highpass interpolation signal I made out of "0" insertion interpolation part 50. The second adder 70 restores the original input image signal R by adding the first and second interpolation band signals. The double speed converter 80 outputs progressive scanning by inputting the restored original image signal R and the interpolation signal I.

Now, the horizontal band blanking filter 90 delays by 4 pixels the vertical direction highpass component separated from the vertical direction bandpass filter 20. It outputs the first interpolation band signal, the same as the "0" insertion interpolation domain (K1, K2) shown by oblique lines in Figure 10, after adding in the form of the fourth adder 92 the delayed vertical direction highpass component and the current incoming vertical direction highpass component, and by multiplying the third multiplier

93 by 1/2.

As mentioned above, the advantage of the present invention is that, as an original incoming image signal, progressive scanning interpolation and scanning line conversion circuits, and without using field and frame memory means, it can prevent drop of vertical direction resolution and visual hindrance phenomena incurred by scanning line structure of the erstwhile interlaced scan method.

It will be appreciated that variations in and modifications to the invention as described and illustrated may be made within the scope of the appended claims.



CLAIMS

1. A method of interpolating a digital image signal comprising the steps of forming from said image signal first and second component parts, said first component part being a highpass component and said second component part being a lowpass component, generating a highpass interpolation signal by inserting "0" in said highpass component, generating a lowpass interpolation signal by interpolating said lowpass component, and applying said highpass interpolation signal and said low pass interpolation signal to adding means, the output of said adding means providing an interpolation signal for said digital image signal.

2. A method as claimed in Claim 1, wherein said interpolation signal output from said adding means is combined with said digital image signal.

3. A method as claimed in Claim 1 or 2, wherein said first and second component parts of said image signal are formed by applying said image signal to filtering means such that said filtering means outputs said highpass component in the form of the image signal from which filtered components have been removed, and applying said image signal and said highpass component to subtracting means to produce said lowpass component in the form substantially of said filtered components.

4. A circuit for interpolating a digital image signal comprising means for dividing said image signal into first and second component parts, said first component part being a highpass component and said second component part being a lowpass component, an "0" insertion interpolation part arranged to insert "0" in said highpass component to generate a highpass interpolation signal, a further interpolation part arranged to interpolate said lowpass component to generate a lowpass interpolation signal, and

first adding means arranged to receive and add said highpass interpolation signal and said lowpass interpolation signal to output an interpolation signal for said digital image signal.

5. A circuit as claimed in Claim 4, further comprising converter means arranged to receive the output of said first adding means, and also being arranged to receive said digital image signal.

6. A circuit as claimed in Claim 4 or Claim 5, wherein said means for dividing said image signal comprises filtering means arranged to filter said image signal and output said highpass component in the form of the image signal from which filtered components have been removed, and subtracting means for subtracting said highpass component from said image signal to produce said lowpass component.

7. A circuit as claimed in Claim 6, wherein said filtering means comprises a vertical bandpass filter arranged to pass as said first component part a vertical direction highpass component of the image signal, said subtracting means being arranged to subtract said vertical direction highpass component from the image signal to produce as said second component part a vertical direction lowpass component, and wherein said further interpolation part comprises a linear interpolation part arranged to generate said lowpass interpolation signal by linear interpolation between the horizontal lines and the vertical direction lowpass component.

8. A circuit as claimed in Claim 6, wherein said filtering means comprises a vertical bandpass filter arranged to pass the vertical direction highpass component from the image signal and a horizonal band blanking filter arranged to pass as said first component part a first

interpolation band signal produced by filtering through vertical band blanking the vertical direction highpass component, said subtracting means being arranged to subtract said first interpolation band signal from the image signal to produce as said second component part a second interpolation band signal, and wherein said further interpolation part comprises a slant correlation interpolation part arranged to generate said lowpass interpolation signal by interpolating through slant correlation the second interpolation band signal.

9. A circuit as claimed in Claim 7 or Claim 8, further comprising a matching delay part arranged to delay and match the image signal as much as the amount of group delay of the vertical bandpass filter, the subtracting means being arranged to produce said second component part by subtracting from said delayed image signal.

10. A circuit as claimed in any of Claims 4 to 9, wherein said "0" insertion interpolation part is arranged to generate said highpass interpolation signal by way of "0" insertion interpolation which makes "0" the level of image signal of interpolation line being generated in between 1H delay line and the current incoming lines.

11. A circuit as claimed in any of Claims 4 to 10, further comprising second adding means arranged to restore the original input image signal from said highpass component and the lowpass component output by said first adding means.

12. A scanning line converter circuit for a digital image signal comprising an interpolating circuit as claimed in any of Claims 4 to 11, and further comprising double speed converter means to which is applied the input image signal and said interpolation signal.

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13. A circuit as claimed in Claim 12, wherein said highpass component is generated by a vertical bandpass filter comprising a first 1H delayer arranged to delay the incoming image signal by 1 horizontal line, a second 1H delayer arranged to delay by 1 horizontal line the image signal which has already been delayed by 1 horizontal line, first and second multipliers arranged to multiply by -1/2 respectively the image signal delayed by 1 horizontal line and the image signal delayed by 2 horizontal lines, and third adding means arranged to add the image signal delayed by 1 horizontal line and the outputs of said first and second multipliers to form said highpass component.

14. A circuit as claimed in Claim 13, wherein said highpass component is also generated by a horizontal band blanking filter comprising a further delayer arranged to delay by 4 pixels the highpass component output from said third adding means of the vertical bandpass filter, fourth adding means arranged to add the current highpass component output from said third adding means and the highpass component delayed by 4 pixels, and a third multiplier arranged to average the highpass component value added from the fourth adding means.

15. A method of interpolating a digital image signal substantially as hereinbefore described with reference to Figures 5 to 11 of the accompanying drawings.

16. A circuit for interpolating a digital image signal substantially as hereinbefore described with reference to Figures 5 to 11 of the accompanying drawings.

17. A scanning line converter circuit for a digital image signal substantially as hereinbefore described with reference to Figures 5 to 11 of the accompanying drawings.

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