

WAFER-LEVEL PACKAGE WITH ENHANCED PERFORMANCERelated Applications

5 **[0001]** This application claims the benefit of provisional patent application serial number 62/374,447, filed August 12, 2016, the disclosure of which is hereby incorporated herein by reference in its entirety.

Field of the Disclosure

10 **[0002]** The present disclosure relates to a wafer-level package and a process for making the same, and more particularly to a wafer-level package with enhanced electrical and rigidity performance, and a packaging process to enhance electrical and rigidity performance of a wafer-level package.

Background

15 **[0003]** The wide utilization of cellular and wireless devices drives the rapid development of radio frequency (RF) technologies. The substrates on which RF devices are fabricated play an important role in achieving high level performance in the RF technologies. Fabrications of the RF devices on conventional silicon substrates may benefit from low cost of silicon materials, a large scale capacity
20 of wafer production, well-established semiconductor design tools, and well-established semiconductor manufacturing techniques.

[0004] Despite the benefits of using conventional silicon substrates for RF device fabrication, it is well known in the industry that the conventional silicon substrates may have two undesirable properties for the RF devices: harmonic
25 distortion and low resistivity values. Harmonic distortion is a critical impediment to achieve high level linearity in the RF devices built over silicon substrates. In addition, the low resistivity encountered in the silicon substrates may degrade quality factors (Q) at high frequencies of microelectromechanical systems (MEMS) or other passive components.

30 **[0005]** Wafer-level fan-out (WLFO) packaging technology and embedded wafer-level ball grid array (EWLB) technology currently attract substantial

attention in portable RF applications. WLFO and EWL B technologies are designed to provide high density input/output ports (I/O) as well as low profile package height without increasing the size of the component semiconductor chips. The I/O pad size on the chip remains small keeping die size to a minimum. This capability allows for densely packaging the RF devices within a single wafer.

[0006] To reduce deleterious harmonic distortion of the RF devices, and to utilize advantages of WLFO/EWL B packaging technologies, it is therefore an object of the present disclosure to provide an improved package design with enhanced performance. Further, there is also a need to enhance the performance of the RF devices without increasing the package size.

Summary

[0007] The present disclosure relates to a wafer-level package with enhanced electrical and rigidity performance, and a packaging process for making the same. The disclosed wafer-level package includes a first thinned die, a second intact die, a multilayer redistribution structure, a first mold compound, and a second mold compound. The first thinned die includes a first device layer, which is formed from glass materials and has a number of first die contacts at a bottom surface of the first device layer. The second intact die includes a second device layer and an intact silicon substrate over the second device layer, wherein the second device layer comprises a plurality of second die contacts at a bottom surface of the second device layer. The multilayer redistribution structure includes a number of package contacts on a bottom surface of the multilayer redistribution structure and redistribution interconnects that connect the package contacts to certain ones of the first die contacts and certain ones of the second die contacts. Connections between the redistribution interconnects and the first die contacts, and between the redistribution interconnects and the second die contacts are solder-free. In addition, the first mold compound resides over the multilayer redistribution structure and around the first thinned die, and extends beyond a top surface of the first thinned die to define an opening within the first mold compound and over the first thinned die. The top surface of the first thinned die is exposed at a bottom of the opening. Additionally, the top surface of the first thinned die is at the bottom of the

opening. The second mold compound fills the opening and is in contact with the top surface of the first thinned die.

[0008] In one embodiment of the wafer-level package, the glass materials are at least one of a group consisting of Silicon Dioxide (SiO_2), Aluminum Oxide (Al_2O_3), Lithium superoxide (LiO_2), Barium oxide (BaO), Potassium oxide (K_2O),

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Sodium Oxide (Na_2O), Boron Oxide (B_2O_3), Magnesium Oxide (MgO), Strontium Oxide (SrO), and Calcium Oxide (CaO).

[0009] In one embodiment of the wafer-level package, the first thinned die provides a microelectromechanical systems (MEMS) component.

5 **[0010]** According to another embodiment, the wafer-level package further includes a second intact die residing over the multilayer redistribution structure. Herein, the second intact die has a second device layer and an intact silicon substrate over the second device layer, and the first mold compound encapsulates the second intact die.

10 **[0011]** In one embodiment of the wafer-level package, the first thinned die provides a MEMS component and the second intact die provides a complementary metal-oxide-semiconductor (CMOS) controller that controls the MEMS component.

[0012] In one embodiment of the wafer-level package, the second device
15 layer is formed from a combination of dielectric and metal layers.

[0013] In one embodiment of the wafer-level package, the second mold compound has an electrical resistivity greater than $1\text{E}6\text{ Ohm-cm}$.

[0014] In one embodiment of the wafer-level package, the first mold compound is formed from a same material as the second mold compound.

20 **[0015]** In one embodiment of the wafer-level package, the first mold compound and the second mold compound are formed from different materials.

[0016] In one embodiment of the wafer-level package, the top surface of the first thinned die exposed at the bottom of the opening is a top surface of the first device layer.

25 **[0017]** In one embodiment of the wafer-level package, the second mold compound is formed from thermoplastics or thermoset materials with a thermal conductivity greater than $2\text{ W/m}\cdot\text{K}$. Herein, the first device layer has a thickness between $70\text{ }\mu\text{m}$ and $1000\text{ }\mu\text{m}$.

[0018] In one embodiment of the wafer-level package, the second mold
30 compound is formed from organic epoxy resin. Herein, the first device layer has a thickness between $5\text{ }\mu\text{m}$ and $1000\text{ }\mu\text{m}$.

[0019] In one embodiment of the wafer-level package, the multilayer redistribution structure is glass-free.

[0020] According to an exemplary process, a mold wafer having a first die and a first mold compound is provided. The first die includes a first device layer and a first silicon substrate over the first device layer. The first device layer is formed from glass materials and includes a number of first die contacts at a bottom surface of the first device layer. A top surface of the first die is a top surface of the first silicon substrate and a bottom surface of the first die is the bottom surface of the first device layer. The first mold compound encapsulates sides and top of the first die such that the bottom surface of the first device layer is exposed. Next, a multilayer redistribution structure is formed underneath the mold wafer. The multilayer redistribution structure includes a number of package contacts on a bottom surface of the multilayer redistribution structure and redistribution interconnects that connect the package contacts to certain ones of the first die contacts. Connections between the redistribution interconnects and the first die contacts are solder-free. The first mold compound is then thinned down to expose the top surface of the first silicon substrate. The first silicon substrate of the first die is removed substantially to provide a first thinned die and form an opening within the first mold compound and over the first thinned die. A top surface of the first thinned die is exposed at a bottom of the opening. The first thinned die has a top surface exposed at a bottom of the opening. Lastly, a second mold compound is applied to substantially fill the opening and directly contact the top surface of the first thinned die.

[0021] Those skilled in the art will appreciate the scope of the present disclosure and realize additional aspects thereof after reading the following detailed description of the preferred embodiments in association with the accompanying drawing figures.

Brief Description of the Drawing Figures

[0022] The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the disclosure, and together with the description serve to explain the principles of the disclosure.

[0023] Figure 1 shows an exemplary wafer-level package according to one embodiment of the present disclosure.

[0024] Figures 2-13 provide exemplary steps that illustrate a process to fabricate the exemplary wafer-level package shown in Figure 1.

5 **[0025]** It will be understood that for clarity of illustration, Figures 1 -13 may not be drawn to scale.

Detailed Description

10 **[0026]** The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the embodiments and illustrate the best mode of practicing the embodiments. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that
15 these concepts and applications fall within the scope of the disclosure and the accompanying claims.

[0027] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from
20 another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0028] It will be understood that when an element such as a layer, region, or
25 substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. Likewise, it will be understood that when an
30 element such as a layer, region, or substrate is referred to as being "over" or extending "over" another element, it can be directly over or extend directly over

the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly over" or extending "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or

5 "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

[0029] Relative terms such as "below" or "above" or "upper" or "lower" or
10 "horizontal" or "vertical" may be used herein to describe a relationship of one element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.

15 **[0030]** The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes," and/or
20 "including" when used herein specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0031] Unless otherwise defined, all terms (including technical and scientific
25 terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense
30 unless expressly so defined herein.

[0032] The present disclosure relates to a wafer-level package with enhanced electrical and rigidity performance, and a packaging process for making the same. Figure 1 shows an exemplary wafer-level package 10 according to one embodiment of the present disclosure. For the purpose of this illustration, the exemplary wafer-level package 10 includes a thinned glass-based die 12, a thinned microelectromechanical systems (MEMS) die 14, a complementary metal-oxide-semiconductor (CMOS) controller die 16, a multilayer redistribution structure 18, a first mold compound 20, and a second mold compound 22. In different applications, the wafer-level package 10 may include fewer or more thinned glass-based /MEMS dies. For instance, in some applications, the wafer-level package 10 may only include thinned MEMS dies and CMOS controller dies; and in some applications, the wafer-level package 10 may only include thinned glass-based dies.

[0033] In detail, the thinned glass-based die 12 includes a first device layer 24, which is formed from glass materials, such as Silicon Dioxide (SiO_2), Aluminum Oxide (Al_2O_3), Lithium superoxide (LiO_2), Barium oxide (BaO), Potassium oxide (K_2O), Sodium Oxide (Na_2O), Boron Oxide (B_2O_3), Magnesium Oxide (MgO), Strontium Oxide (SrO), and Calcium Oxide (CaO). The glass materials used in the first device layer 24 may be alkali free. The first device layer 24 includes a number of first die contacts 26 and at least one electronic component (not shown) coupled to the first die contacts 26. Herein, the first die contacts 26 are at a bottom surface of the first device layer 24, while the at least one electronic component (not shown) is not exposed at a top surface of the first device layer 24. Since the first device layer 24 is formed from glass materials, which typically have low thermal tolerance, the at least one electronic component (not shown) in the first device layer 24 is a low heat-generation component, such as a low-power filter, a low-power capacitor, and etc. The first device layer 24 may have a thickness between 5 μm and 1000 μm , which may ensure at least 100 psi molding pressure, or between 70 μm and 1000 μm , which may ensure at least 750 psi molding pressure (more details are described in the following fabrication

process). From size, cost, and rigidity aspects, the first device layer 24 may have a thickness between 70 μm and 200 μm .

[0034] The thinned MEMS die 14 includes a second device layer 28, which is also formed from glass materials, such as Silicon Dioxide (SiO_2), Aluminum Oxide (Al_2O_3), Lithium superoxide (LiO_2), Barium oxide (BaO), Potassium oxide (K_2O), Sodium Oxide (Na_2O), Boron Oxide (B_2O_3), Magnesium Oxide (MgO), Strontium Oxide (SrO), and Calcium Oxide (CaO). The glass materials used in the first device layer 24 may be alkali free. The second device layer 28 includes a number of second die contacts 30 and a MEMS component (not shown) coupled to the second die contacts 30. Herein, the second die contacts 30 are at a bottom surface of the second device layer 28, while the MEMS component is not exposed at a top surface of the second device layer 28. The MEMS component is typically a switch and has low heat-generation. The second device layer 28 may have a thickness between 5 μm and 1000 μm , which may ensure at least 100 psi molding pressure, or between 70 μm and 1000 μm , which may ensure at least 750 psi molding pressure (more details are described in the following fabrication process). From size, cost, and rigidity aspects, the second device layer 28 may have a thickness between 70 μm and 200 μm .

[0035] Notice that the thinned glass-based die 12 and the thinned MEMS die 14 are both thinned dies, which have a device layer and essentially no silicon substrate over the device layer. Herein, essentially no silicon substrate over the device layer refers to at most 2 μm silicon substrate over the device layer. In desired cases, each thinned die does not include any silicon substrate over the device layer such that a top surface of each thinned die is a top surface of the device layer. For other cases, the top surface of one thinned die may be a top surface of the thin silicon substrate.

[0036] The CMOS controller die 16 includes a third device layer 32 and a silicon substrate 34 over the third device layer 32. The third device layer 32 may include a CMOS controller (not shown) that controls the MEMS component (not shown) within the thinned MEMS die 14, and a number of third die contacts 36 that are coupled to the CMOS controller and at a bottom surface of the third

device layer 32. The third device layer 32 has a thickness between 0.1 μm and 50 μm , and may be formed from a combination of dielectric and metal layers (such as silicon oxide, silicon nitride, aluminum, titanium, copper, or the like). The CMOS controller die 16 is an intact die, which includes the intact silicon substrate 34 with a thickness between 25 μm and 250 μm or between 10 μm and 750 μm .

[0037] Herein, the multilayer redistribution structure 18 includes a first dielectric pattern 38 at the top, a number of redistribution interconnects 40, a second dielectric pattern 42, and a number of package contacts 44. In one embodiment, the thinned glass-based die 12, the thinned MEMS die 14, and the CMOS controller die 16 reside directly over the multilayer redistribution structure 18. As such, the first device layer 24 of the thinned glass-based die 12, the second device layer 28 of the thinned MEMS die 14, and the third device layer 32 of the CMOS controller die 16 are in contact with the first dielectric pattern 38. In addition, the first die contacts 26 at the bottom surface of the first device layer 24, the second die contacts 30 at the bottom surface of the second device layer 28, and the third die contacts 36 at the bottom surface of the third device layer 32 are exposed through the first dielectric pattern 38.

[0038] For the purpose of this illustration, the redistribution interconnects 40 include five first redistribution interconnects 40(1) and one second redistribution interconnect 40(2). In different applications, the redistribution interconnects 40 may include fewer or more first redistribution interconnects 40(1)/second redistribution interconnects 40(2). Each first redistribution interconnect 40(1) connects one package contact 44 to a corresponding one of the first, second, and third die contacts 26, 30, and 36. The second redistribution interconnect 40(2) is used to connect one second die contact 30 to a corresponding third die contact 36, such that the CMOS controller (not shown) within the CMOS controller die 16 electrically connects the MEMS component (not shown) within the thinned MEMS die 14. Herein, each redistribution interconnect 40 is electrically coupled to at least one of the first, second, and third die contacts 26, 30, and 36 through the first dielectric pattern 38 and extends underneath the first

dielectric pattern 38. The connections between the redistribution interconnects 40 and the first, second, and third die contacts 26, 30, and 36 are solder-free.

[0039] The second dielectric pattern 42 is formed underneath the first dielectric pattern 38. The second dielectric pattern 42 partially encapsulates each first redistribution interconnect 40(1). As such, a portion of each first redistribution interconnect 40(1) is exposed through the second dielectric pattern 42. Further, the second dielectric pattern 42 fully encapsulates the second redistribution interconnect 40(2). As such, no portion of the second redistribution interconnect 40(2) is exposed through the second dielectric pattern 42. In different applications, there may be extra redistribution interconnects (not shown) electrically coupled to the redistribution interconnects 40 through the second dielectric pattern 42, and an extra dielectric pattern (not shown) formed underneath the second dielectric pattern 42 to partially encapsulate each of the extra redistribution interconnects.

[0040] In this embodiment, each package contact 44 is on a bottom surface of the multilayer redistribution structure 18 and electrically coupled to a corresponding first redistribution interconnect 40(1) through the second dielectric pattern 42. Consequently, the first redistribution interconnects 40(1) connect the package contacts 40 to certain ones of the first, second, and third die contacts 26, 30, and 36. Herein, the package contacts 44 are separate from each other and extend underneath the second dielectric pattern 42, such that an air gap 46 is formed surrounding each package contact 44. The air gap 46 may extend underneath the thinned glass-based die 12 and/ or underneath the thinned MEMS die 14.

[0041] Further, the multilayer redistribution structure 18 may be free of glass fiber or glass-free. Herein, the glass fiber refers to individual glass strands twisted to become a larger grouping. These glass strands may then be woven into a fabric. The first dielectric pattern 38 and the second dielectric pattern 42 may be formed of Benzocyclobutene (BCB) or polyimide. The redistribution interconnects 40 may be formed of copper or other suitable metals. The package contacts 44 may be formed of at least one of copper, gold, nickel, and palladium.

The multilayer redistribution structure 18 has a thickness between 2 μm and 300 μm .

[0042] The first mold compound 20 resides over a top surface of the multilayer redistribution structure 18, resides around the thinned glass-based die 12 and the thinned MEMS die 14, and encapsulates the CMOS controller die 16. Further, the first mold compound 20 extends beyond a top surface of the thinned glass-based die 12 to define a first opening 48 within the first mold compound 20 and over the thinned glass-based die 12, and extends beyond a top surface of the thinned MEMS die 14 to define a second opening 50 within the first mold compound 20 and over the thinned MEMS die 14. Herein, the top surface of the thinned glass-based die 12 is exposed at a bottom of the first opening 48, and the top surface of the thinned MEMS die 14 is exposed at a bottom of the second opening 50.

[0043] The second mold compound 22 substantially fills the first and second openings 48 and 50, and is in contact with the top surface of the thinned glass-based die 12 and the top surface of the thinned MEMS die 14. The second mold compound 22 may have an electrical resistivity greater than 1E6 Ohm-cm. The high electrical resistivity of the second mold compound 22 may improve the quality factor (Q) at high frequencies of the MEMS component (not shown) of the thinned MEMS die 14.

[0044] The second mold compound 22 may be formed of thermoplastics or thermoset materials with a thermal conductivity greater than 2 W/m·K, such as PPS (poly phenyl sulfide), overmold epoxies doped with boron nitride or alumina thermal additives, or the like. The second mold compound 22 may also be formed from an organic epoxy resin system with a thermal conductivity less than 2 W/m·K. The second mold compound 22 may be formed of a same or different material as the first mold compound 20. However, unlike the second mold compound 22, the first mold compound 20 does not have electrical resistivity requirements. Herein, a portion of the second mold compound 22 may reside over a top surface of the first mold compound 20. Notice that the second mold compound 22 is separate from the CMOS controller die 16 by the first mold

compound 20. A top surface of the CMOS controller die 16 is in contact with the first mold compound 20.

[0045] Figures 2-13 provide exemplary steps to fabricate the exemplary wafer-level package 10 shown in Figure 1. Although the exemplary steps are illustrated in a series, the exemplary steps are not necessarily order dependent. Some steps may be done in a different order than that presented. Further, processes within the scope of this disclosure may include fewer or more steps than those illustrated in Figures 2-13.

[0046] Initially, an adhesive layer 52 is applied on a top surface of a carrier 54 as illustrated in Figure 2. Then, a glass-based die 12D, a MEMS die 14D, and the CMOS controller die 16 are attached to the adhesive layer 52 as illustrated in Figure 3. In different applications, there might be fewer or more dies attached to the adhesive layer 52. For instance, in some applications, there may be only the glass-based die 12D attached to the adhesive layer 52; and in some applications, there may be only the MEMS die 14D and the CMOS controller die 16 attached to the adhesive layer 52.

[0047] The glass-based die 12D includes the first device layer 24 and a first silicon substrate 56 over the first device layer 24. As such, the bottom surface of the first device layer 24 is a bottom surface of the glass-based die 12D, and the backside of the first silicon substrate 56 is a top surface of the glass-based die 12D. The first silicon substrate 56 has a thickness between 5 μm and 750 μm . The glass-based die 12D has a thickness between 75 μm and 250 μm , or between 10 μm and 1750 μm .

[0048] The MEMS die 14D includes the second device layer 28 and a second silicon substrate 58 over the second device layer 28. As such, the bottom surface of the second device layer 28 is a bottom surface of the MEMS die 14D, and the backside of the second silicon substrate 58 is a top surface of the MEMS die 14D. The second silicon substrate 58 has a thickness between 5 μm and 750 μm . The MEMS die 14D has a thickness between 75 μm and 250 μm , or between 10 μm and 1750 μm . In this embodiment, the CMOS controller die 16 may be shorter than the glass-based die 12D and the MEMS die 14D. In different applications,

the CMOS controller die 18 may be the same height as the glass-based die 12D and the MEMS die 14D, or the CMOS controller die 18 may be taller than the glass-based die 12D and the MEMS die 14D.

[0049] Next, the first mold compound 20 is applied over the adhesive layer 52 to encapsulate the glass-based die 12D, the MEMS die 14D, and the CMOS controller die 16 as illustrated in Figure 4. The first mold compound 20 may be applied by various procedures, such as sheet molding, overmolding, compression molding, transfer molding, dam fill encapsulation, or screen print encapsulation. In a typical compression molding, a molding pressure used for applying the first mold compound 20 is between 100 psi and 1000 psi. Since the glass-based die 12D, the MEMS die 14D, and the CMOS controller die 16 are relatively thick and the bottom surfaces of the glass-based die 12D, the MEMS die 14D, and the CMOS controller die 16 are essentially flat, there may be no vertical deformations occurring to the glass-based die 12D, the MEMS die 14D, or the CMOS controller die 16 during this molding step.

[0050] The first mold compound 20 may be an organic epoxy resin system or the like, which can be used as an etchant barrier to protect the glass-based die 12D, the MEMS die 14D, and the CMOS controller die 16 against etching chemistries such as potassium hydroxide (KOH), sodium hydroxide (NaOH), and acetylcholine (ACH). A curing process (not shown) is then used to harden the first mold compound 20. The curing temperature is between 100 °C and 320 °C depending on which material is used as the first mold compound 20. The adhesive layer 52 and the carrier 54 are then removed to expose the bottom surface of the first device layer 24, the bottom surface of the second device layer 28, and the bottom surface of the third device layer 32 as shown in Figure 5. Removal of the adhesive layer 52 and the carrier 54 may be provided by heating the adhesive layer 52.

[0051] With reference to Figures 6 through 9, the multilayer redistribution structure 18 is formed according to one embodiment of the present disclosure. The first dielectric pattern 38 is firstly formed underneath the glass-based die 12D, the MEMS die 14D, and the CMOS controller die 16, as illustrated in Figure

6. As such, the first, second, and third die contacts 26, 30, and 36 are exposed through the first dielectric pattern 38.

[0052] Next, the redistribution interconnects 40 are formed as illustrated in Figure 7. Herein, the redistribution interconnects 40 includes five first
5 redistribution interconnects 40(1) and one second redistribution interconnect 40(2). In different applications, the redistribution interconnects 40 may include fewer or more first redistribution interconnects 40(1)/second redistribution interconnects 40(2). The first redistribution interconnects 40(1) are electrically
10 coupled to the first, second, and third die contacts 26, 30, and 36 through the first dielectric pattern 38 and extend underneath the first dielectric pattern 38. The second redistribution interconnect 40(2) is used to connect one second die contact 30 to a corresponding third die contact 36, such that the CMOS controller (not shown) within the CMOS controller die 16 electrically connects the MEMS component (not shown) within the thinned MEMS die 14. The second
15 redistribution interconnect 40(2) may also extend underneath the first dielectric pattern 38. The connections between the redistribution interconnects 40 and the first, second, and third die contacts 26, 30, and 36 are solder-free.

[0053] The second dielectric pattern 42 is formed underneath the first dielectric pattern 38 to partially encapsulate each first redistribution interconnect
20 40(1) as illustrated in Figure 8. As such, a portion of each first redistribution interconnect 40(1) is exposed through the second dielectric pattern 42. Further, the second dielectric pattern 42 fully encapsulates the second redistribution interconnect 40(2). As such, no portion of the second redistribution interconnect 40(2) is exposed through the second dielectric pattern 42. Lastly, the package
25 contacts 44 and the air gap 46 are formed as illustrated in Figure 9. Each package contact 44 is coupled to an exposed portion of a corresponding first redistribution interconnect 40(1) through the second dielectric pattern 42. Consequently, the first redistribution interconnects 40(1) connect the package contacts 44 to certain ones of the first, second, and third die contacts 26, 30, and
30 36. In addition, the package contacts 44 are separate from each other and

extend underneath the second dielectric pattern 42, such that the air gap 46 is simultaneously formed surrounding each package contact 44.

[0054] After the multilayer redistribution structure 18 is formed, the first mold compound 20 is thinned down to expose the first silicon substrate 56 of the glass-based die 12D and the second silicon substrate 58 of the MEMS die 14D as shown in Figure 10. The thinning procedure may be done with a mechanical grinding process. Since the CMOS controller die 16 has a lower height than both the MEMS die 14D and the glass-based die 12D, the silicon substrate 34 of the CMOS controller die 16 is not exposed and still encapsulated by the first mold compound 20.

[0055] Next, the first silicon substrate 56 and the second silicon substrate 58 are removed substantially to provide a precursor package 60, as illustrated in Figure 11. The removal of the first silicon substrate 56 from the glass-based die 12D provides the thinned glass-based die 12 and forms the first opening 48 within the first mold compound 20 and over the thinned glass-based die 12. The removal of the second silicon substrate 58 from the MEMS die 14D provides the thinned MEMS die 14 and forms the second opening 50 within the first mold compound 20 and over the thinned MEMS die 14. Herein, removing substantially a silicon substrate refers to removing at least 95% of the entire silicon substrate and leaving at most 2 μm silicon substrate. In desired cases, the first and second silicon substrates 56 and 58 are removed completely, such that the first device layer 24 of the thinned glass-based die 12 is exposed at the bottom of the first opening 48 and the second device layer 28 of the thinned MEMS die 14 is exposed at the bottom of the second opening 50.

[0056] Removing substantially the first and second silicon substrates 56 and 58 may be provided by an etching process with a wet/dry etchant chemistry, which may be TMAH, KOH, ACH, NaOH, or the like. Both the first device layer 24 and the second device layer 28 are formed from glass materials, which are resistant to these wet/dry etching chemistries, such that the electronic components (not shown) within the first device layer 24 and the MEMS component (not shown) within the second device layer 28 will not be damaged by

these wet/dry etching chemistries. The first mold compound 20 encapsulates and protects the CMOS controller die 16 from the wet/dry etchant chemistries. In some applications, a protection layer (not shown) may be placed at the bottom surface of the multilayer redistribution structure 18 to protect the package contacts 44 from the etchant chemistry. The protection layer is applied before the etching process and removed after the etching process. Further, if the silicon substrate 34 of the CMOS controller die 16 is not encapsulated by the first mold compound 20 (in some applications, if the CMOS controller die 16 has a same height as or is taller than glass-based die 12 and the MEMS die 14, the silicon substrate 34 of the CMOS controller die 16 will be exposed during the thinning process), there may be an extra protection layer (not shown) placed over the silicon substrate 34 to protect the CMOS controller die 16 from the wet/dry etchant chemistry. The extra protection layer is applied before the etching process and removed after the etching process.

15 **[0057]** The second mold compound 22 is then applied to substantially fill the first and second openings 48 and 50, as illustrated in Figure 12. Herein, substantially filling an opening refers to filling at least 75% of the entire opening. The second mold compound 22 directly resides over the top surface of the thinned glass-based die 12 and the top surface of the thinned MEMS die 14. If

20 there is no first silicon substrate 56 left in the first opening 48 and no second silicon substrate 58 left in the second opening 50, the second mold compound 22 directly resides over the first device layer 24 and the second device layer 28. In addition, the second mold compound 22 may further reside over the first mold compound 20. In some applications, the precursor package 60 may be attached

25 to a rigid carrier (not shown) before applying the second mold compound 22 to substantially fill the first and second openings 48 and 50. The rigid carrier (not shown) may help assist with mechanical support of the precursor package 60 and help prevent further deformation of the thinned glass-based die 12 and the thinned MEMS die 14.

30 **[0058]** The second mold compound 22 may be applied by various procedures, such as sheet molding, overmolding, compression molding, transfer molding,

dam fill encapsulation, and screen print encapsulation. During the molding process of the second mold compound 22, liquefaction and molding pressure are not uniform across the entire precursor package 60. A first combination of the thinned glass-based die 12 and a first portion of the multilayer redistribution structure 18 directly underneath the thinned glass-based die 12, and a second combination of the thinned MEMS die 14 and a second portion of the multilayer redistribution structure 18 directly underneath the thinned MEMS die 14 may suffer more molding pressure than the other portions of the precursor package 60.

10 **[0059]** In one embodiment, the second mold compound 22 is formed of thermoplastics or thermoset materials with a thermal conductivity greater than 2 W/m·K. A typical molding pressure (compression molding) used for applying the second mold compound 20 is between 250 psi and 1000 psi. Herein, the first device layer 24 of the thinned glass-based die 12 may have a thickness between
15 70 μm and 1000 μm to endure at least 750 psi molding pressure. As such, even if a first portion of the air gap 46 is vertically below the thinned glass-based die 12, and there is no extra mechanical support within the first portion of the air gap 46, vertical deformations of the thinned glass-based die 12 may not occur or may be within an acceptable level. Similarly, the second device layer 28 of the thinned
20 MEMS die 14 has a thickness between 70 μm and 1000 μm to endure at least 750 psi molding pressure. As such, even if a second portion of the air gap 46 is vertically below the thinned MEMS die 14, and there is no extra mechanical support within the second portion of the air gap 46, vertical deformations of the thinned MEMS die 14 may not occur or may be within an acceptable level.

25 **[0060]** Since both the thinned glass-based die 12 and the thinned MEMS die 14 are low heat-generation dies, the second mold compound 22 directly residing over the thinned glass-based die 12 and the thinned MEMS die 14 is not required to have a high thermal conductivity. In another embodiment, the second mold compound 22 may be formed from an organic epoxy resin system with a thermal
30 conductivity less than 2 W/m·K. A typical molding pressure (overmolding) used for applying the second mold compound 20 is between 100 psi and 1000 psi.

Herein, the first device layer 24 of the thinned glass-based die 12 may have a thickness between 5 μm and 1000 μm , which endures at least 100 psi molding pressure. As such, even if the first portion of the air gap 46 is vertically below the thinned glass-based die 12, and there is no extra mechanical support within the first portion of the air gap 46, the vertical deformations of the thinned glass-based die 12 may not occur or may be within an acceptable level. Similarly, the second device layer 28 of the thinned MEMS die 14 may have a thickness between 5 μm and 1000 μm , which endures at least 100 psi molding pressure. As such, even if the second portion of the air gap 46 is vertically below the thinned MEMS die 14, and there is no extra mechanical support within the second portion of the air gap 46, the vertical deformations of the thinned MEMS die 14 may not occur or may be within an acceptable level.

[0061] Notice that, the silicon substrate 34 of the CMOS controller die 16 remains in the precursor package 60 and is encapsulated by the first mold compound 20. As such, the third device layer 36 of the CMOS controller die 16 is not required to be formed from glass materials or have a relatively thick thickness to avoid vertical deformation. The third device layer 36 may be formed from a combination of dielectric and metal layers (such as silicon oxide, silicon nitride, aluminum, titanium, copper, or the like) and has a thickness between 0.1 μm and 50 μm .

[0062] A curing process (not shown) is followed to harden the second mold compound 22. The curing temperature is between 100 $^{\circ}\text{C}$ and 320 $^{\circ}\text{C}$ depending on which material is used as the second mold compound 22. Lastly, a top surface of the second mold compound 22 is then planarized to form the wafer-level package 10, as illustrated in Figure 13. If the second mold compound 22 does not cover a top surface of the first mold compound 20, the top surface of the second mold compound 22 and /or the first mold compound 20 are planarized to be coplanar (not shown). A mechanical grinding process may be used for planarization. The wafer-level package 10 may be marked, diced, and singulated into individual components (not shown).

[0063] Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

Claims

What is claimed is:

1. An apparatus comprising:

- 5 a first thinned die comprising a first device layer, which is formed from glass materials and comprises a plurality of first die contacts at a bottom surface of the first device layer;
- a second intact die comprising a second device layer and an intact silicon substrate over the second device layer, wherein the second device layer comprises a plurality of second die contacts at a bottom surface of the second device layer;
- 10 a multilayer redistribution structure comprising a plurality of package contacts on a bottom surface of the multilayer redistribution structure and redistribution interconnects that connect the plurality of package contacts to certain ones of the plurality of first die contacts and certain ones of the plurality of second die contacts, wherein connections between the redistribution interconnects and the plurality of first die contacts, and between the redistribution interconnects and the plurality
- 15 of second die contacts are solder-free;
- a first mold compound residing over the multilayer redistribution structure wherein:
 - the first mold compound surrounds the first thinned die, and extends beyond a top surface of the first thinned die to define an opening within the first mold compound and over the first thinned die, wherein the top surface of the first thinned die is at a bottom of
 - 20 the opening; and
 - the first mold compound encapsulates the second intact die; and
 - a second mold compound filling the opening and in contact with the top surface of the first thinned die.
- 25 2. The apparatus of claim 1 wherein the glass materials are at least one of a group consisting of Silicon Dioxide (SiO_2), Aluminum Oxide (Al_2O_3), Lithium superoxide (LiO_2), Barium oxide (BaO), Potassium oxide (K_2O), Sodium Oxide (Na_2O), Boron Oxide (B_2O_3), Magnesium Oxide (MgO), Strontium Oxide (SrO), and Calcium Oxide (CaO).
- 30 3. The apparatus of claim 1 wherein the first device layer has a thickness between 5 μm and 1000 μm .
4. The apparatus of claim 1 wherein the first device layer has a thickness between 70 μm and 200 μm .

5. The apparatus of claim 1 wherein the first thinned die provides a microelectromechanical systems (MEMS) component.
- 5 6. The apparatus of claim 1 wherein the first thinned die provides a MEMS component and the second intact die provides a complementary metal-oxide-semiconductor (CMOS) controller that controls the MEMS component.
7. The apparatus of claim 1 wherein the second device layer is formed from a combination of
10 dielectric and metal layers.
8. The apparatus of claim 1 wherein the second mold compound has an electrical resistivity greater than 1E6 Ohm-cm.
- 15 9. The apparatus of claim 1 wherein the first mold compound is formed from a same material as the second mold compound.
10. The apparatus of claim 1 wherein the first mold compound and the second mold compound are formed from different materials.
- 20 11. The apparatus of claim 1 wherein the top surface of the first thinned die exposed at the bottom of the opening is a top surface of the first device layer.
12. The apparatus of claim 1 wherein the second mold compound is formed from thermoplastics or
25 thermoset materials with a thermal conductivity greater than 2 W/m·K.
13. The apparatus of claim 12 wherein the first device layer has a thickness between 70 μm and 1000 μm .
- 30 14. The apparatus of claim 1 wherein the second mold compound is formed from organic epoxy resin.
15. The apparatus of claim 14 wherein the first device layer has a thickness between 5 μm and 1000 μm .

16. The apparatus of claim 1, wherein the multilayer redistribution structure is glass-free.

17. A method comprising:

- 5 providing a mold wafer having a first die and a first mold compound, wherein:
 - the first die comprises a first device layer and a first silicon substrate over the first device layer, wherein the first device layer is formed from glass materials and comprises a plurality of first die contacts at a bottom surface of the first device layer;
 - a top surface of the first die is a top surface of the first silicon substrate and a
 - 10 bottom surface of the first die is the bottom surface of the first device layer; and
 - the first mold compound encapsulates sides and the top surface of the first die, wherein the bottom surface of the first device layer is exposed;
 - forming a multilayer redistribution structure underneath the mold wafer, wherein:
 - the multilayer redistribution structure comprises a plurality of package contacts on a
 - 15 bottom surface of the multilayer redistribution structure and redistribution interconnects that connect the plurality of package contacts to certain ones of the plurality of first die contacts; and
 - connections between the redistribution interconnects and the plurality of first die contacts are solder-free;
 - 20 thinning down the first mold compound to expose the top surface of the first silicon substrate;
 - removing substantially the first silicon substrate of the first die to provide a first thinned die and form an opening within the first mold compound and over the first thinned die, wherein the first thinned die has a top surface exposed at a bottom of the opening; and
 - 25 applying a second mold compound to substantially fill the opening and directly contact the top surface of the first thinned die.

18. The method of claim 17 wherein the first die provides a MEMS component.

30 19. The method of claim 17 wherein:

- the second mold compound is formed from thermoplastics or thermoset materials with a thermal conductivity greater than 2 W/m·K;
- the second mold compound is applied between 250 psi and 1000 psi; and
- the first device layer has a thickness between 70 μm and 1000 μm .

20. The method of claim 17, wherein:

the second mold compound is formed from organic epoxy resin;

the second mold compound is applied between 100 psi and 1000 psi; and

5 the first device layer has a thickness between 5 μm and 1000 μm .

21. The method of claim 17, wherein the mold wafer further comprises a second intact die, wherein:

the second intact die has a second device layer and a second silicon substrate over the

second device layer, wherein the second device layer comprises a plurality of second die contacts at

10 a bottom surface of the second device layer; and

the first mold compound encapsulates sides and a top surface of the second intact die,

wherein the bottom surface of the second device layer is exposed.

22. The method of claim 21, wherein forming the multilayer redistribution structure underneath the

15 mold wafer further comprises connecting the plurality of package contacts to certain ones of the

plurality of second die contacts by the redistribution interconnects.

23. The method of claim 22, wherein the second intact die is shorter than the first die, such that

after thinning down the first mold compound to expose the top surface of the first silicon substrate,

20 the second silicon substrate is not exposed and is still encapsulated by the first mold compound.