(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
15 July 2004 (15.07.2004)

PCT

(10) International Publication Number
WO 2004/059727 A1

(51) International Patent Classification[7]: H01L 21/84

(21) International Application Number:
PCT/US2002/040869

(22) International Filing Date:
19 December 2002 (19.12.2002)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, NY 10504 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **FRIED, David, M.** [US/US]; 201 Maple Avenue, B2, Ithaca, NY 14850 (US). **NOWAK, Edward, J.** [US/US]; 8 Windridge Road, Essex Junction, VT 05452 (US). **RAINEY, BethAnn** [US/US]; 2 Olde Orchard Park, Apartment 219, South Burlington, VT 05403 (US).

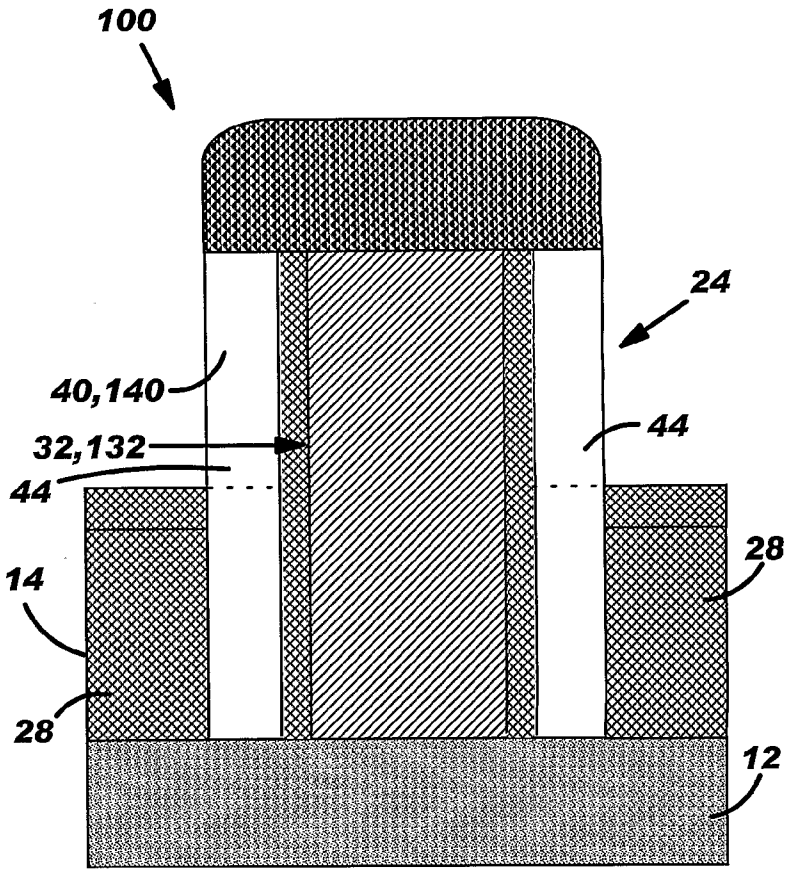
(74) Agent: **PEPPER, Margaret, A.**; International Business Machines Corporation, Dept. 18G, Building 300/482, 2070 Route 52, Hopewell Junction, NY 12533 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),

[Continued on next page]

(54) Title: METHODS OF FORMING STRUCTURE AND SPACER AND RELATED FINFET



(57) Abstract: Methods for forming a spacer (44) for a first structure (24, 124), such as a gate structure of a FinFET, and at most a portion of a second structure (14), such as a fin, without detrimentally altering the second structure. The methods generate a first structure (24) having a top portion (30, 130) that overhangs an electrically conductive lower portion (32, 132) and a spacer (44) under the overhang (40, 140). The overhang (40, 140) may be removed after spacer processing. Relative to a FinFET, the overhang protects parts of the fin (14) such as regions adjacent and under the gate structure (24, 124) , and allows for exposing sidewalls of the fin (14) to other processing such as selective silicon growth and implantation. As a result, the methods allow sizing of the fin (14) and construction of the gate structure (24, 124) and spacer without detrimentally altering (e.g., eroding by forming a spacer thereon) the fin (14) during spacer processing. A FinFET (100) including a gate structure (24, 124) and spacer (44) is also disclosed.

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European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— *of inventorship (Rule 4.17(iv)) for US only*

Published:

— *with international search report*

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