

OPTICAL TRANSCEIVER

[0001] This application claims the priority of the Chinese patent application filed with the China Patent Office on November 27, 2023, with application number 202311589919.4 and invention name “Optical Transceiver”, the entire contents of which are incorporated by reference into this application.

TECHNICAL FIELD

[0002] The present application belongs to the field of lasers, and specifically relates to an optical transceiver.

BACKGROUND ART

[0003] In the airtight transistor outline (TO) coaxial package, the transistor cap and the transistor base are usually welded on the same plane. Since the large surface of the transistor base needs to be connected to the pins, the side of the transistor base is required to dissipate heat. However, the side area of the transistor base is small and the distance from the packaged chip is also far, so that a good heat dissipation effect cannot be achieved.

SUMMARY OF THE INVENTION

[0004] Purpose of the invention: The embodiment of the present application provides an optical transceiver to solve the above-mentioned problems.

[0005] Technical solution: An optical transceiver described in an embodiment of the present application includes:

[0006] a transistor base, the transistor base comprising a first base portion and a second base portion intersecting and interconnected, as well as a first side portion and a second side portion spaced apart from each other in a first direction, and the first side portion and the second side portion being both connected to the first base portion and the second base portion and defining an accommodating

cavity having a first opening;

[0007] a transistor cap, connected to the transistor base and covering the first opening;

[0008] a photoelectric chip, arranged in the accommodating cavity, the photoelectric chip being arranged on the first base portion; and

[0009] an electrical connector, passing through the second base portion and extending into the accommodating cavity, one end of the electrical connector passing through the accommodating cavity and being electrically connected to the photoelectric chip, and the other end of the electrical connector being located outside the accommodating cavity.

[0010] In some embodiments, the transistor base has a first welding end surface surrounding the first opening, the transistor cap has a second welding end surface, the first welding end surface and the second welding end surface are located in the same plane, and the transistor base and the transistor cap are sealed and connected via the first welding end surface and the second welding end surface.

[0011] In some embodiments, the first base portion has a first welding sub-surface facing the transistor cap, the second base portion has a second welding sub-surface facing the transistor cap, the first side portion has a third welding sub-surface facing the transistor cap, the second side portion has a fourth welding sub-surface facing the transistor cap, and the first welding sub-surface, the second welding sub-surface, the third welding sub-surface and the fourth welding sub-surface are located in the same plane and are sequentially connected to form the first welding end surface.

[0012] In some embodiments, the transistor cap comprises a first cap portion, and a second cap portion connected to each other, and a third side portion and a

fourth side portion arranged at intervals in the first direction; the third side portion and the fourth side portion are both connected to the first cap portion and the second cap portion and enclose an optical path cavity having a second opening; the optical path cavity is connected to the accommodating cavity; and the second welding end surface surrounds the second opening; and

[0013] the first cap portion has a fifth welding sub-surface facing the first base portion, the second cap portion has a sixth welding sub-surface facing the second base portion, the third side portion has a seventh welding sub-surface facing the first side portion, the fourth side portion has an eighth welding sub-surface facing the second side portion, and the fifth welding sub-surface, the sixth welding sub-surface, the seventh welding sub-surface and the eighth welding sub-surface are located in the same plane and are sequentially connected to form the second welding end surface.

[0014] In some embodiments, the first cap portion is provided with a first combining portion extending along a side away from the second cap portion; the first combining portion has a first combining surface facing the first welding sub-surface and a first extrusion surface away from the first welding sub-surface; the first combining surface and the fifth welding sub-surface are located in the same plane and connected to each other, and the first extrusion surface is parallel to the first welding sub-surface; and

[0015] the second cap portion is provided with a second combining portion extending along a side away from the first cap portion; the second combining portion has a second combining surface facing the second welding sub-surface and a second extrusion surface away from the second welding sub-surface, the second combining surface and the sixth welding sub-surface are located in the

same plane and are connected to each other, and the second extrusion surface is parallel to the second welding sub-surface.

[0016] In some embodiments, the first base portion has a corresponding first surface and a second surface in the second direction, the second base portion has a corresponding third surface and a fourth surface in the third direction, and the second surface is connected to the third surface; and

[0017] the first cap portion is opposite to the third surface in the third direction, the second cap portion is opposite to the second surface in the second direction and the first direction, the second direction and the third direction intersect each other.

[0018] In some embodiments, the transistor cap is provided with an optical port, the optical port faces the optoelectronic chip, the optical port is sealed with a first optical window, and the optoelectronic chip is configured to emit or receive laser light toward the first optical window.

[0019] In some embodiments, the transistor cap is provided with an observation port, and the observation port is sealed with a second optical window.

[0020] In some embodiments, the optical transceiver further comprises:

[0021] a lens, wherein the lens is arranged on a side of the first optical window facing away from the optoelectronic chip, and the lens is configured to couple laser light emitted or received by the optoelectronic chip.

[0022] In some embodiments, the optical transceiver further comprises:

[0023] a monitoring chip, wherein the monitoring chip is arranged in the accommodating cavity, the monitoring chip is connected to the second base portion, and the monitoring chip is electrically connected to the optoelectronic chip and the electrical connector respectively.

[0024] Beneficial effect: The optical transceiver of the embodiment of the present application includes a transistor base, the transistor base includes a first base portion and a second base portion that intersect and are connected to each other, and a first side portion and a second side portion that are spaced apart in a first direction, the first side portion and the second side portion are both connected to the first base portion and the second base portion and surround an accommodating cavity with a first opening; a transistor cap, wherein the transistor cap is connected to the transistor base and covers the first opening; an optoelectronic chip, wherein the optoelectronic chip is arranged in the accommodating cavity and is at least connected to the first base portion; an electrical connector, wherein the electrical connector is connected to the second base portion, one end of the electrical connector is passed through the accommodating cavity and electrically connected to the optoelectronic chip, that is, the optoelectronic chip is arranged on the first base portion to be spaced apart from the electrical connector on the second base portion, so that the optoelectronic chip has a larger heat dissipation area and improves the heat dissipation performance. In addition, the first side portion and the second side portion can also be used to contact the optoelectronic chip and serve as the heat dissipation surface of the optoelectronic chip, which is beneficial to further improve the heat dissipation effect.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] In order to more clearly illustrate the technical solutions in the embodiments of the present application, the drawings required for use in the description of the embodiments will be briefly introduced below. Obviously, the drawings described below are only some embodiments of the present application.

For those skilled in the art, other drawings can be obtained based on these drawings without creative work.

[0026] FIG. 1 is a schematic diagram of the structure of an optical transceiver according to Embodiment 1 of the present application;

[0027] FIG. 2 is a schematic diagram of the internal cross-sectional structure of the optical transceiver in Embodiment 1 of the present application;

[0028] FIG. 3 is a schematic diagram of the structure of a transistor base, an optoelectronic chip, an electrical connector and a monitoring chip in Embodiment 1 of the present application;

[0029] FIG. 4 is a schematic diagram of the structure of the transistor base in Embodiment 1 of the present application;

[0030] FIG. 5 is a schematic diagram of the structure of the transistor cap in Embodiment 1 of the present application;

[0031] FIG. 6 is a schematic diagram of the structure of an optical transceiver with a coupling lens according to Embodiment 1 of the present application;

[0032] FIG. 7 is a schematic diagram of the structure of an optical transceiver with a coupling lens according to Embodiment 2 of the present application; and

[0033] Description of reference numerals: 1, optical transceiver; 10, transistor base; 100, first base portion; 1000, first surface; 1001, second surface; 1002, extension portion; 1003, support portion; 101, second base portion; 1010, third surface; 1011, fourth surface; 102, first side portion; 103, second side portion; 104, accommodating cavity; 105, first opening; 106, first welding end surface; 1060, first welding sub-surface; 1061, second welding sub-surface; 1062, third welding sub-surface; 1063, fourth welding sub-surface; 20, transistor cap; 200, first cap portion; 2000, first combining portion; 2001, first combining surface;

2002, first extrusion surface; 201, second cap portion; 2010, second combining portion; 2011, second combination surface; 2012, second extrusion surface; 202, third side portion; 203, fourth side portion; 204, optical path cavity; 205, second opening; 206, second welding end surface; 2060, fifth welding sub-surface; 2061, sixth welding sub-surface; 2062, seventh welding sub-surface; 2063, eighth welding sub-surface; 207, welding protrusion; 208, optical port; 209, observation port; 30, optoelectronic chip; 300, laser; 301, pad; 40, electrical connector; 400, insulating portion; 401, connecting portion; 50, first optical window; 60, second optical window; 70, lens; 80, monitoring chip; 90, positioning groove; X, first direction; Y, second direction; Z, third direction.

DETAILED DESCRIPTION

[0034] The technical solutions in the embodiments of the present application will be described clearly and completely below in conjunction with the drawings in the embodiments of the present application. Obviously, the described embodiments are only part of the embodiments of the present application, rather than all of the embodiments. Based on the embodiments in the present application, all other embodiments obtained by those skilled in the art without creative work are within the scope of protection of the present application.

[0035] In the description of the present application, it should be understood that the terms "length", "width", "thickness", "up", "down", "front", "back", "left", "right", "top", "bottom", "inside", "outside" and the like indicate positions or positional relationships based on the positions or positional relationships shown in the accompanying drawings, and are only for the convenience of describing the present application and simplifying the description, rather than indicating or implying that the device or element referred to must have a specific

orientation, be constructed and operated in a specific orientation, and therefore cannot be understood as a limitation on the present application. In addition, the terms "first" and "second" are used for descriptive purposes only, and cannot be understood as indicating or implying relative importance or implicitly indicating the number of technical features indicated. Thus, the features defined as "first" and "second" may explicitly or implicitly include one or more features. In the description of the present application, "multiple" means two or more, and at least one means one, two or more, unless otherwise clearly and specifically defined.

[0036] It should also be noted that in the description of this application, "vertical" means completely vertical at 90° or almost completely vertical, for example, an angle within the range of 80° to 100° is considered vertical. Similarly, "parallel" means completely parallel or almost completely parallel, for example, an angle within 10° of completely parallel is considered parallel.

[0037] The applicant noted that with the rise of demand for 1550nm LiDAR and the application of silicon photonics in optical modules, high-power lasers are used to achieve better heat dissipation in a low-cost manner, which will positively help the output power of the light source of 1550nm LiDAR and silicon photonics modules. The traditional airtight transistor outline (TO) is a coaxial package, with the metal cap and the header welded on the same plane. The larger bottom surface of the header is mostly used for pin lead-out and flexible board welding, which cannot achieve good heat dissipation effect. The heat can only be dissipated by the side of the header, but the side area is small and far away from the chip, so the heat dissipation performance is poor.

[0038] In view of this, an embodiment of the present application discloses an optical transceiver, which can solve at least one of the above-mentioned defects.

[0039] Embodiment 1:

[0040] Referring to FIGS. 1 to 5, the optical transceiver 1 has a first direction X, and includes a transistor base 10, a transistor cap 20, an optoelectronic chip 30, and an electrical connector 40. The transistor base 10 includes a first base portion 100, a second base portion 101, and a first side portion 102 and a second side portion 103 that are intersecting and connected to each other in the first direction X. The first side portion 102 and the second side portion 103 are connected to the first base portion 100 and the second base portion 101 and enclose an accommodating cavity 104 having a first opening 105. The transistor cap 20 is connected to the transistor base 10 and covers the first opening 105. The optoelectronic chip 30 is disposed in the accommodating cavity 104, and the optoelectronic chip 30 is at least connected to the first base portion 100. The electrical connector 40 is connected to the second base portion 101, one end of the electrical connector 40 is passed through the accommodating cavity 104 and electrically connected to the optoelectronic chip 30, and the other end is located outside the accommodating cavity 104.

[0041] The optoelectronic chip 30 is arranged on the first base portion 100 to be spaced from the electrical connector 40 on the second base portion 101, so that the optoelectronic chip 30 has a larger heat dissipation area and improves the heat dissipation performance. In addition, the first side portion 102 and the second side portion 103 can also be used to contact the optoelectronic chip 30 and serve as the heat dissipation surface of the optoelectronic chip 30, which is beneficial to further improve the heat dissipation effect.

[0042] It should be noted that, in the present embodiment, the intersection of the first base portion 100 and the second base portion 101 means that there is an

angle between the first base portion 100 and the second base portion 101 that is not 0° or 180° , so that the electrical connector 40 and the optoelectronic chip 30 are spaced from each other in structure, and the electrical connector 40 is prevented from occupying the heat dissipation surface of the optoelectronic chip 30. On this basis, after the first side portion 102 and the second side portion 103 are connected to the transistor cap 20, the first side portion 102 and the second side portion 103 are not occupied by the electrical connector 40, that is, the optoelectronic chip 30 can also conduct heat to contact the first side portion 102 and/or the second side portion 103, so as to further expand the contact heat dissipation surface, thereby improving the overall heat dissipation effect.

[0043] Further, referring to FIGS. 1 to 5, in some embodiments, the transistor base 10 has a first welding end surface 106 surrounding the first opening 105, and the transistor cap 20 has a second welding end surface 206. The first welding end surface 106 and the second welding end surface 206 are parallel to each other and connected to each other. In the present embodiment, the transistor base 10 and the transistor cap 20 are wedge-shaped structures, and the two can be sealed and combined through the first welding end surface 106 and the second welding end surface 206.

[0044] In addition, the present embodiment takes the arrangement of the optoelectronic chip 30 in the accommodating cavity 104 as an example. It can be understood that the optoelectronic chip 30 can include a laser 300 and a detector (not shown in the figure) integrated in the accommodating cavity 104 to complete the reception and transmission of optical signals. In other embodiments, if this product is only an optical transmitter, then the optoelectronic chip 30 can be set

as a laser 300; if this product is only an optical receiver, then the optoelectronic chip 30 can be set as a detector.

[0045] Specifically, referring to FIG. 2, FIG. 3 and FIG. 4, the optical transceiver 1 further has a second direction Y and a third direction Z, and the first direction X, the second direction Y and the third direction Z intersect each other. The first base portion 100 has a corresponding first surface 1000 and a second surface 1001 in the second direction Y, and the second base portion 101 has a corresponding third surface 1010 and a fourth surface 1011 in the third direction Z, and the second surface 1001 is connected to the third surface 1010; the first base portion 100 has a first welding sub-surface 1060 facing the transistor cap 20, the second base portion 101 has a second welding sub-surface 1061 facing the transistor cap 20, the first side portion 102 has a third welding sub-surface 1062 facing the transistor cap 20, and the second side portion 103 has a fourth welding sub-surface 1063 facing the transistor cap 20, and the first welding sub-surface 1060, the second welding sub-surface 1061, the third welding sub-surface 1062 and the fourth welding sub-surface 1063 are sequentially connected to form a first welding end surface 106.

[0046] Referring to FIGS. 2 and 5, in some embodiments, the transistor cap 20 includes a first cap portion 200, a second cap portion 201, and a third side portion 202 and a fourth side portion 203 that are connected to each other in the first direction X. The third side portion 202 and the fourth side portion 203 are connected to the first cap portion 200 and the second cap portion 201 and surround an optical path cavity 204. The optical path cavity 204 is connected to the accommodating cavity 104. The second welding end surface 206 surrounds the second opening 205. The first cap portion 200 is opposite to the third surface

1010 in the third direction Z, and the second cap portion 201 is opposite to the second surface 1001 in the second direction Y.

[0047] Specifically, the first cap portion 200 has a fifth welding sub-surface 2060 facing the first base portion 100, the second cap portion 201 has a sixth welding sub-surface 2061 facing the second base portion 101, the third side portion 202 has a seventh welding sub-surface 2062 facing the first side portion 102, and the fourth side portion 203 has an eighth welding sub-surface 2063 facing the second side portion 103. The fifth welding sub-surface 2060, the sixth welding sub-surface 2061, the seventh welding sub-surface 2062 and the eighth welding sub-surface 2063 are sequentially connected to form an integral second welding end surface 206.

[0048] It should be noted that, referring to FIG. 5, in order to increase the contact surface between the first cap portion 200, the third side portion 202 and the fourth side portion 203 and the transistor base 10, the first cap portion 200, the third side portion 202 and the fourth side portion 203 extend the first combining portion 2000 on the plane where the second welding end surface 206 is located. The first combining portion 2000 has a first combining surface 2001 facing the first welding sub-surface 1060 and a first extrusion surface 2002 away from the first welding sub-surface 1060. The first combining surface 2001 and the fifth welding sub-surface 2060 are located in the same plane and connected to each other. The first extrusion surface 2002 is parallel to the first welding sub-surface 1060. The fifth welding sub-surface 2060 actually includes the side surface of the first combining portion 2000 facing the transistor base 10.

[0049] Similarly, the second cap portion 201, the third side portion 202 and the fourth side portion 203 extend the second combining portion 2010 on the plane

where the second welding surface is located. The second combining portion 2010 has a second combining surface 2011 facing the second welding sub-surface 1061 and a second extrusion surface 2012 away from the second welding sub-surface 1061. The second combining surface 2011 and the sixth welding sub-surface 2061 are located in the same plane and are connected. The second extrusion surface 2012 is parallel to the second welding sub-surface 1061. The above-mentioned sixth welding sub-surface 2061 actually includes the side of the second combining portion 2010 facing the transistor base 10.

[0050] It should be noted that the integral transistor base 10 can be made of a metal material with high thermal conductivity by machining or stamping. Specifically, metal materials such as copper, aluminum, silver, tungsten, etc. can be flexibly used according to actual needs, and the first base portion 100, the second base portion 101, the first side portion 102 and the second side portion 103 of the transistor base 10 can actually be integrally formed, and in this case, the first welding end surface 106 is formed when the transistor base 10 is formed.

[0051] Similarly, the integral transistor cap 20 can also be processed by metal material craftsmanship or stamping. Specifically, metal materials such as copper and aluminum can be flexibly used according to actual needs. The first cap portion 200, the second cap portion 201, the third side portion 202, the fourth side portion 203, the first combining portion 2000 and the second combining portion 2010 of the transistor cap 20 can actually be formed as one piece. In addition, the second welding end surface 206 is formed when the transistor cap 20 is formed; the transistor cap 20 is usually also subjected to surface treatment, such as tin plating, nickel plating, etc., to improve its corrosion resistance and connection performance.

[0052] In the present embodiment, the first side portion 102, the second side portion 103, the third side portion 202 and the fourth side portion 203 are arranged to form a first welding end surface 106 and a second welding end surface 206 that are parallel to each other. While being compatible with traditional resistance welding transistor base 10 and transistor cap 20 equipment, a higher airtightness yield and reliability can be obtained. Compared with only arranging the first base portion 100, the second base portion 101, the first cap portion 200 and the second cap portion 201, the need for multiple welding surfaces at the same time during welding is avoided, the resistance welding process requirements are reduced, and the welding reliability and production efficiency are improved.

[0053] In order to facilitate the connection between the transistor base 10 and the transistor cap 20 by resistance welding, the first extrusion surface 2002 and the second extrusion surface 2012 are used for abutment by the resistance welding equipment, which is conducive to making the first combining surface 2001, the second combining surface 2011 and the overall second welding end surface 206 stably abut against the first welding end surface 106.

[0054] In addition, referring to FIG. 5, in some embodiments, the transistor cap 20 encloses an optical path cavity 204 having a second opening 205, and the second welding end surface 206 is provided with a welding protrusion 207 toward the first welding end surface 106, and the welding protrusion 207 surrounds the second opening 205. In the present embodiment, the transistor cap 20 and the transistor base 10 are welded by a resistance welding process to ensure the airtightness of the accommodating cavity 104 and the optical path cavity 204,

and the welding protrusion 207 improves the sealing effect when the two are connected by resistance welding.

[0055] Exemplarily, referring to FIG. 2 and FIG. 3, a support portion 1003 is formed on the second surface 1001 of the transistor base 10, and the optoelectronic chip 30 includes a laser 300 (Laser Diode, LD for short) and a pad 301 (Laser Diode Submount, LD SM for short), wherein the pad 301 is fixed on the support portion 1003, and the laser 300 is fixed on the pad 301. Specifically, the laser 300 can be connected to the pad 301 by gold soldering, and the pad 301 can be fixed to the support portion 1003 by silver glue or gold soldering.

[0056] The pad 301 can provide mechanical support and protection for the laser 300, preventing the laser 300 from being affected by external shock or vibration, thereby extending the life and stability of the laser 300. In addition, the pad 301 can dissipate heat for the laser 300 in time to maintain its stable operating temperature. In addition, the pad 301 has precise size and geometric shape, which can provide accurate optical positioning to accurately arrange the laser 300, thereby ensuring the precise alignment between the laser diode and other optical elements to obtain high-quality laser output.

[0057] In some embodiments, referring to FIG. 1, FIG. 2 and FIG. 3, the electrical connector 40 is configured as a pin that penetrates the second base portion 101, and an insulating portion 400 is provided between the outer side of the pin and the second base portion 101. The insulating portion 400 may be a glass insulator, and is fixed to the transistor base 10 by high-temperature sintering. In the present embodiment, the electrical connector 40 is electrically connected to the pad 301 through the connecting portion 401, thereby electrically connecting the laser 300. The connecting portion 401 may be a gold-tin solder

sheet, solder paste, etc. In addition, the electrical connector 40 may also be directly connected to the pad 301 by gold wire bonding. In other embodiments, the electrical connector 40 may also be a multilayer ceramic substrate, which will not be described in detail here.

[0058] In addition, in some embodiments, referring to FIG. 3, the optical transceiver 1 further includes a monitoring chip 80 (Monitor Photodiode, MPD for short), which is disposed in the accommodating cavity 104 and connected to the third surface 1010. The monitoring chip 80 can be fixed to the third surface 1010 by using silver glue, and the monitoring chip 80 can be electrically connected to the optoelectronic chip 30 and the electrical connector 40 by welding only, respectively. The monitoring chip 80 can monitor the backlight intensity output by the laser 300, that is, by being installed on the back side of the laser 300, converting the optical signal into an electrical signal to monitor the backlight intensity of the laser 300 in real time, thereby providing a feedback signal for controlling and adjusting the output power and stability of the laser 300.

[0059] In addition, in order to further improve the heat dissipation effect of the laser 300, in other embodiments, a semiconductor cooler (Thermoelectric Cooler, TEC for short) can be added to the support portion 1003 for connecting the laser 300 and the pad 301, and components such as thermistors can be provided to detect the temperature of the laser 300 in real time to improve the stability of use.

[0060] In some embodiments, referring to FIG. 1, FIG. 2 and FIG. 5, the first cap portion 200 is provided with an optical port 208, the optical port 208 faces the laser 300, and the optical port 208 is sealed with a first optical window 50.

The laser 300 can emit laser light toward the first optical window 50, so that the laser light can be smoothly guided out of the optical path cavity 204.

[0061] In addition, the second cap portion 201 is provided with an observation port 209, which faces the laser 300 and is sealed with a second optical window 60. The observation port 209 and the second optical window 60 can be used to observe the components in the accommodating cavity 104 such as the laser 300, facilitate high-precision mounting with external components, and improve the coupling efficiency with external optical components.

[0062] It should be noted that the first optical window 50 and the second optical window 60 can be made of glass optical window material having a thermal expansion coefficient intersecting with the transistor cap 20, and can be sealed and bonded to the transistor cap 20 by gold soldering or glass solder high-temperature sintering.

[0063] In some embodiments, referring to FIG. 2 and FIG. 6, the optical transceiver 1 further includes a lens 70, which is disposed on a side of the first optical window 50 away from the laser 300. The lens 70 is configured to couple the laser emitted or received by the optoelectronic chip 30. For example, the vertical and horizontal divergence angles of the laser emitted by the laser 300 can be adjusted by the lens 70, so as to couple and match with external optical components.

[0064] It should be noted that the angle between the first base portion 100 and the second base portion 101 is limited to be between 60° and 135°. Within this angle range, the first base portion 100 carries the optoelectronic chip 30 and the second base portion 101 carries the electrical connector 40 without interfering with each other, and the first base portion 100 can have enough space for the

optoelectronic chip 30 to dissipate heat. When the angle between the first base portion 100 and the second base portion 101 is less than 60° , the space between the second surface 1001 and the third surface 1010 is narrow, which is not conducive to installing the optoelectronic chip 30; when the angle is greater than 135° , the electrical connector 40 that passes through the second base portion 101 may affect the installation of the first base portion 100 and the entire optical transceiver 1. Therefore, it is preferred that the angle between the first base portion 100 and the second base portion 101 is between 60° and 135° .

[0065] In the present embodiment, the first direction X, the second direction Y and the third direction Z are perpendicular to each other, that is, the first base portion 100 and the second base portion 101 are perpendicular to each other, and the first cap portion 200 and the second cap portion 201 are also perpendicular to each other, so that the optoelectronic chip 30 and the electrical connector 40 are independent of each other, and the internal space layout of the optical transceiver 1 is more reasonable, with better heat dissipation effect and sufficient installation space.

[0066] In addition, referring to FIG. 2, the interconnected ends of the first base portion 100 and the second base portion 101 are provided with a positioning groove 90 penetrating the first surface 1000 and the fourth surface 1011, and the positioning groove 90 is intended to correspond to the coaxial packaging equipment to quickly position and install the transistor base 10.

[0067] In addition, in the present embodiment, a single-channel laser 300 is taken as an example. In other embodiments, multiple lasers 300 and multiple optical signal channels can also be set. In addition, in other embodiments, an optical receiver can be set or the laser 300 and the optical receiver can be

arranged in one piece in the accommodating cavity 104, which will not be repeated here.

[0068] Embodiment 2:

[0069] Referring to FIG. 7, the difference between the present embodiment and Embodiment 1 is that: illustratively, one end of the first base portion 100 away from the second base portion 101 is connected to an extension portion 1002 in the third direction Z, and correspondingly, a smaller lens 70 than that in Embodiment 1 can be used and directly coupled to the extension portion 1002 to adapt to different process methods.

[0070] In addition, in other embodiments, the lens 70 may also be directly built into the transistor cap 20, which will not be described in detail herein.

[0071] The optical transceiver provided in the embodiment of the present application is introduced in detail above, and the principles and implementation methods of the present application are explained by applying specific examples. The description of the above embodiments is only used to help understand the technical solution and its core idea of the present application; ordinary technicians in this field should understand that: they can still modify the technical solutions recorded in the aforementioned embodiments, or replace some of the technical features therein with equivalents; and these modifications or replacements do not make the essence of the corresponding technical solution deviate from the scope of the technical solution of the embodiments of the present application.

CLAIMS

- [Claim 1] An optical transceiver (1), comprising:
- a transistor base (10), the transistor base (10) comprising a first base portion (100) and a second base portion (101) intersecting and interconnected, and a first side portion (102) and a second side portion (103) spaced apart from each other in a first direction (X), the first side portion (102) and the second side portion (103) being both connected to the first base portion (100) and the second base portion (101) and defining an accommodating cavity (104) having a first opening (105);
- a transistor cap (20), connected to the transistor base (10) and covering the first opening (105);
- a photoelectric chip (30), arranged in the accommodating cavity (104), the photoelectric chip (30) being arranged on the first base portion (100); and
- an electrical connector (40), passing through the second base portion (101) and extending into the accommodating cavity (104), one end of the electrical connector (40) passing through the accommodating cavity (104) and being electrically connected to the photoelectric chip (30), and the other end of the electrical connector being located outside the accommodating cavity (104).
- [Claim 2] The optical transceiver (1) according to claim 1, wherein,
- the transistor base (10) has a first welding end surface (106) surrounding the first opening (105), the transistor cap (20) has a second welding end surface (206), the first welding end surface

(106) and the second welding end surface (206) are located in the same plane, and the transistor base (10) and the transistor cap (20) are sealed and connected via the first welding end surface (106) and the second welding end surface (206).

[Claim 3] The optical transceiver (1) according to claim 2, wherein, the first base portion (100) has a first welding sub-surface (1060) facing the transistor cap (20), the second base portion (101) has a second welding sub-surface (1061) facing the transistor cap (20), the first side portion (102) has a third welding sub-surface (1062) facing the transistor cap (20), the second side portion (103) has a fourth welding sub-surface (1063) facing the transistor cap (20), and the first welding sub-surface (1060), the second welding sub-surface (1061), the third welding sub-surface (1062) and the fourth welding sub-surface (1063) are located in the same plane and are sequentially connected to form the first welding end surface (106).

[Claim 4] The optical transceiver (1) according to claim 3, wherein, the transistor cap (20) comprises a first cap portion (200) and a second cap portion (201) connected to each other, and a third side portion (202) and a fourth side portion (203) arranged at intervals in the first direction (X); the third side portion (202) and the fourth side portion (203) are both connected to the first cap portion (200) and the second cap portion (201) and enclose an optical path cavity (204) having a second opening; the optical path cavity (204) is

connected to the accommodating cavity (104); and the second welding end surface (206) surrounds the second opening (205); and the first cap portion (200) has a fifth welding sub-surface (2060) facing the first base portion (100), the second cap portion (201) has a sixth welding sub-surface (2061) facing the second base portion (101), the third side portion (202) has a seventh welding sub-surface (2062) facing the first side portion (102), the fourth side portion (203) has an eighth welding sub-surface (2063) facing the second side portion (103), and the fifth welding sub-surface (2060), the sixth welding sub-surface (2061), the seventh welding sub-surface (2062) and the eighth welding sub-surface (2063) are located in the same plane and are sequentially connected to form the second welding end surface (206).

[Claim 5] The optical transceiver (1) according to claim 4, wherein, the first cap portion (200) is provided with a first combining portion (2000) extending along a side away from the second cap portion (201); the first combining portion (2000) has a first combining surface (2001) facing the first welding sub-surface (1060) and a first extrusion surface (2002) away from the first welding sub-surface (1060); the first combining surface (2001) and the fifth welding sub-surface (2060) are located in the same plane and connected to each other, and the first extrusion surface (2002) is parallel to the first welding sub-surface (1060); and the second cap portion (201) is provided with a second combining portion (2010) extending along a side away from the first cap

portion (200); the second combining portion (2010) has a second combining surface (2011) facing the second welding sub-surface (1061) and a second extrusion surface (2012) away from the second welding sub-surface (1061), the second combining surface (2011) and the sixth welding sub-surface (2061) are located in the same plane and are connected to each other, and the second extrusion surface (2012) is parallel to the second welding sub-surface (1061).

[Claim 6] The optical transceiver (1) according to claim 4, wherein, the first base portion (100) has a corresponding first surface (1000) and a second surface (1001) in the second direction (Y), the second base portion (101) has a corresponding third surface (1010) and a fourth surface (1011) in the third direction (Z), and the second surface (1001) is connected to the third surface (1010); and the first cap portion (200) is opposite to the third surface (1010) in the third direction (Z), the second cap portion (201) is opposite to the second surface (1001) in the second direction (Y), and the first direction (X), the second direction (Y) and the third direction (Z) intersect each other.

[Claim 7] The optical transceiver (1) according to claim 1, wherein, the transistor cap (20) is provided with an optical port (208), the optical port (208) faces the optoelectronic chip (30), the optical port (208) is sealed with a first optical window (50), and the optoelectronic chip (30) is configured to emit or receive laser light toward the first optical window (50).

[Claim 8] The optical transceiver (1) according to claim 1, wherein,

the transistor cap (20) is provided with an observation port (209), and the observation port (209) is sealed with a second optical window (60).

[Claim 9] The optical transceiver (1) according to claim 7, wherein, the optical transceiver (1) further comprises:

a lens (70), wherein the lens (70) is arranged on a side of the first optical window (50) facing away from the optoelectronic chip (30), and the lens (70) is configured to couple laser light emitted or received by the optoelectronic chip (30).

[Claim 10] The optical transceiver (1) according to claim 1, wherein, the optical transceiver (1) further comprises:

a monitoring chip (80), wherein the monitoring chip (80) is arranged in the accommodating cavity (104), the monitoring chip (80) is connected to the second base portion (101), and the monitoring chip (80) is electrically connected to the optoelectronic chip (30) and the electrical connector (40) respectively.