BIT STREAM PROCESSING FOR REPLAY

This invention relates to the reproduction of a digitally encoded signal from a medium and in particular to the identification and processing of replay data in a multiplex format.

BACKGROUND OF THE INVENTION.

The introduction of disks recorded with digitally compressed audio and video signals, for example, utilizing MPEG compression protocols, offers the consumer sound and picture quality virtually indistinguishable from the original material. However, consumer users will expect such digital video disks or DVDs to offer features similar to those of their analog video cassette recorder or VCR. For example, a VCR may reproduce in either forward or reverse directions at speeds other than the recorded speed. Such non-standard speed playback features are also known as trick play modes. The provision of trick play features are less easily provided with MPEG encoded video signals due to the hierarchical nature of the compression which forms pictures into groups having varying degrees of compression. These groups are termed groups of pictures or GOPs, and require decoding in sequence. A detailed description of the MPEG 2 standard is published as ISO/IEC Standard 13818-2. However, in simple terms, an MPEG 2 signal stream may comprise three types of pictures having varying degrees of content compression. An intra-coded frame or I frame has the least compression of the three types and may be decoded without reference to any other frame. A predicted frame or P frame is compressed with reference to a preceding I or P frame and achieves greater degree of compression than an intra-coded frame. The third type of MPEG frame, termed a bi-directionally coded or B frame, may be compressed based on predictions from preceding and / or succeeding frames. Bi-directionally coded frames have the greatest degree of compression. The three types of MPEG frames are arranged in groups of pictures or GOPs. The GOP may for example contain 12 frames arranged as illustrated in FIGURE 1A. Since only an intra-coded frame is decodable without reference to any other frame, each GOP may only be decoded following the decoding of the I frame. The first predicted frame or P frame, may be decoded and stored based on modification of the stored, preceding I frame. Subsequent P frames may be predicted from the stored preceding P frame. The prediction of P frames is indicated in FIGURE 1A by the curved, solid arrow head

lines. Finally, bi-directionally coded or B frames may be decoded by means of predictions from preceding and or succeeding frames, for example, stored I and P frames. Decoding of B frames by predictions from adjacent stored frames is depicted in FIGURE 1A by the curved, dotted arrow head lines.

The hierarchical nature of the coded frames comprising MPEG groups of pictures necessitates that the I and P frames of each GOP are decoded in the forward direction. Thus, reverse mode features may be provided by effectively jumping back to an earlier, or preceding I frame and then decoding in a forward direction through that GOP. The decoded frames being stored in frame buffer memories for subsequent read out in reverse to achieve the desired reverse program sequence. FIGURE 1B illustrates play back in the forward direction at normal speed and at a time prior to time t0, a reverse three times speed mode trick play mode is selected. The trick play mode is initiated at time t0 where I-frame I(25) is decoded and displayed. The next frame required for decoding is I-frame I(13), thus the transducer is repositioned, as indicated by arrow J1 to acquire frame I(13). Having recovered and decoded I-frame I(13), the transducer tracks, as indicated by arrow J2 to acquire and decode frame P(16). The process is repeated as indicated by arrows J 3, J4. Following the acquisition and decoding of frame P (22) the transducer is moved as depicted by arrow Jn to recover frame I (1). To smoothly portray scene motion requires the decoding and display of I, P, and possibly B-frames. The jump and play process is repeated for preceding GOP, thereby progressing haltingly backwards through the records whilst smoothly portraying the program material in a reverse sequence at the video output.

The provision of visually smooth reproduction during trick mode reproduction requires timely disk retrieval and access to specific pictures from memory. Although each digital disk is encoded with navigation data which provides picture access points within each video object unit, these are limited in number, and may inherently contribute to temporally aliased image motion. To achieve temporally smooth trick mode reproduction, at multiple speeds in forward and reverse directions requires access to, and decoding of all encoded pictures. Although such performance is attainable at the cost of storage capacity, bit stream analysis and selection for buffer storage

provides opportunities for improved trick mode reproduction through efficient memory utilization.

SUMMARY OF THE INVENTION

An apparatus reproduces a bitstream signal from a disk. The bitstream is controlled to ensure that only requested bitstream data is coupled for MPEG decoding. A transducer is repositioned to obtain requested bitstream data prior to completion of preceding MPEG picture decoding. The bitstream data is read prior to buffer storage to select wanted data for storage and to reject unwanted data. Buffer storage is reallocated for trick play operation and is random accessed to facilitate trick play picture selection. MPEG picture decoding and storage are controlled to facilitate frame decoding within one field period. Decoded pictures are stored and read out substantially concurrently within a field period.

In an inventive arrangement, an apparatus reproduces a digitally encoded signal from a medium. The apparatus comprises a transducer for transducing the digitally encoded signal and generating a bit stream therefrom. A processor is coupled to receive the bit stream for controllably processing the bit stream. A memory is coupled to the processor for storing the processed bit stream information. A controller is coupled to control the memory and the processor for controlling identification of information within the bit stream, wherein the controller controls the processor to identify a specific sector type in the bit stream and responsive to the specific sector identification the controller controls the memory for storing the identified specific sector.

In an inventive method a start code is acquired from a plurality of start codes in a data stream arranged in a plurality of sectors transduced during reproduction by a digital disk apparatus. The method comprises the steps of searching the data stream to locate a specific sector type in the plurality of sectors. The specific sector type is searched to locate a start code from the plurality of start codes. The start code is tested to determine if it is incomplete. Searching the data stream to locate a second sector of the specific sector type in the plurality of sectors. Searching the second sector of the specific sector type to locate a second start code of the start code type from the plurality of start codes. Determining if the second start code is the residue of the incomplete start code. Combining the incomplete start

code value and the residue start code value to form a complete start code.

A further inventive apparatus for reproducing a digitally encoded signal from a medium, comprises a transducer for transducing the digitally encoded signal and generating a bit stream therefrom. A first memory is coupled to the transducer for storing the bit stream. A second memory for storing data is controllably coupled from the first memory. A controller is coupled to control the first and second memories for controlling identification of information within the bit stream wherein the controller controls the first memory to output the bit stream from a specific sector address therein, and the controller controls the second memory to store a first part of the bit stream output from the specific sector address.

In another inventive apparatus a digitally encoded signal is reproduced from a medium. The apparatus comprises a transducer for transducing the digitally encoded signal and generating a bit stream therefrom. A memory is coupled to the transducer for storing the bit stream. A processor is coupled to the memory for processing the stored bit stream to identify an MPEG start code contained therein. The processor searches the stored bit stream to identify the MPEG start code in the stored bit stream and responsive to the MPEG start code identification the processor indicates the identification and stores a sector address of the identified MPEG start code.

A further method for picture decoding and display in an apparatus reproducing from a digital disk. The method comprises the steps of transducing a digitally encoded signal from the disk. Storing the digitally encoded signal in a first memory. Decoding the digitally encoded signal to produce a picture. Storing the picture in a second memory. Coupling the picture from the second memory for display. Controlling the storing in the second memory and the coupling for display to occur substantially concurrently.

In yet a further inventive method one field of the picture is stored in a first field of the second memory and a previous picture is coupled for display from a second field of said second memory.

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is coupled for display from a first field of the second memory. The storing in said first field of said second memory and the coupling for display are controlled to occur sequentially within a field period.

In another inventive arrangement, an apparatus for reproducing a digitally encoded signal from a disk medium, comprises a transducer which transduces the digitally encoded signal. A memory is coupled to the transducer for storing the digitally encoded signal. A decoder is responsive to the digitally encoded signal for decoding a picture therefrom. A controller for the memory, wherein a first operational mode the controller controls the memory to read the stored digitally encoded signal from the memory responsive to a first sequence and in a second operational mode the controller controls the memory to read the stored digitally encoded signal from the memory in a second sequence.

In yet another inventive arrangement, an apparatus for reproduces a digitally encoded signal from a disk medium and comprises a source of a bitstream representative of a digitally encoded signal. A processor is coupled to the bitstream for processing the bitstream to extract at least a first and a second data type represented therein. A memory is controllably coupled to the processor for storing one of the first and a second data types. A controller is coupled to control allocation of the memory, wherein a first reproducing mode the controller allocates the memory for storing the first data type, and in a second reproducing mode the controller allocates the memory for storing the second data type.

In yet a further inventive arrangement, an apparatus for reproducing a digitally encoded signal from a disk medium, comprises a transducer for transducing the digitally encoded signal. A processor is coupled to receive the digitally encoded signal for processing and generating a picture therefrom. A memory is coupled to the processor for storing the picture. A controller is coupled to control the memory and the processor, wherein a first mode the picture is stored in the memory and in a second mode the picture is sub-sampled and stored in the memory.

In yet another inventive arrangement, unnecessary processing of unwanted sector data is avoided. A method for controlling data reproduced in sectors by a disk player employing optical read out, comprises the steps of transducing groups of sectors

including sectors wanted for processing, and sectors unwanted for processing.

Supplying the wanted sectors exclusive of the unwanted sectors to a data processor for processing, and processing the wanted data sectors to extract data therein representative of video information.

In still another inventive arrangement, delay in a transduced bitstream path is substantially obviated from a process for controlling a transducer position. During replay in digital disk apparatus a method comprises the steps of receiving a first and a second transducer address for controlling the transducer position responsive to a replayed address. Comparing the replayed address with the first transducer address to detect equality therebetween. In response to the detected equality moving the transducer to a new position determined by the second transducer address.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1A illustrates an MPEG 2 group of pictures.

FIGURE 1B illustrates recorded groups of pictures, during replay and reverse trick play at three times speed.

FIGURE 2 is a block diagram of an exemplary digital disk player including inventive arrangements.

FIGURE 3 shows in greater detail part of FIGURE 2 and depicting various inventive arrangements.

FIGURE 4 shows the digital disk player of FIGURE 2 including other advantageous arrangements to those of FIGURE 2.

FIGUREsS 5A and 5B depict an exemplary bit stream before track buffering.

FIGURES 5C - 5D depict exemplary data in buffer memory.

FIGURE 6 is a flow chart illustrating an inventive arrangement for the recovery of start codes distributed across sector boundaries.

Figure 7 is a chart illustrating an inventive sequence for a reverse trick play mode of 3 times play speed (3X).

DETAILED DESCRIPTION

FIGURE 2 depicts an exemplary block diagram of a digital video disk player. In block 10 a deck is shown which may accept a digitally recorded disk 14 for rotation by a motor 12. A digital signal is recorded on disk 14 as a spiral track containing pits with respective pit lengths determined by an 8/16 modulation coding responsive to respective signal data bits. The record on disk 14 is read by pick up

15 which gathers reflected illumination from a laser. The reflected laser light is collected by a photo detector or opto pick-up device. An imaging device, for example a lens or mirror, which form part of transducer pick-up 15, is servo controlled and driven by motor 11 to follow the recorded track. Different parts of the recording may be accessed by rapidly repositioning the imaging device. Servo controlled motors 11 and 12 are driven by integrated circuit drive amplifier 20. Pick up 15 is coupled to an opto preamplifier, block 30, which includes drive circuitry for the laser illuminator and a preamplifier which provides amplification and equalization for the reflected signal output from the opto pick-up device. The amplified and equalized replay signal from opto preamplifier 30 is connected to a channel processor block 40 where the replay signal is employed to synchronize a phase locked loop which is utilized to demodulate the 8:16 modulation employed for recording.

The MPEG encoded bitstream is encoded for error detection and correction by means of Reed Solomon product coding which is applied in blocks of 16 sectors, where each sector contains 2048 bytes of payload data. Thus following 8:16 demodulation the replay data stream is de-interleaved or unshuffled and error corrected by means of Reed Solomon product correction implemented in ECC buffer memories 45 and 46 of FIGURE 4. Each buffer stores 16 sectors of the replay data stream arranged as an array to facilitate de-interleaving and to enable the required row and column product processing. The cascaded ECC buffer memories introduce a delay to reproduced serial bit stream of approximately (2 * 16 * 1.4) milliseconds, where 2 represents the pair of ECC buffers, 16 represents the sectors over which the correction is applied and 1.4 milliseconds represents a sector period at 1X rotational speed. Thus the reproduced serial bit stream is delayed by a minimum of approximately 45 milliseconds.

The error corrected signal bitstream 41 is coupled via a link processor to a bit stream or mechanical / track buffer memory 60A. The track buffer comprises a DRAM memory type and is used to store an amount of replayed data such that data losses during transducer or pickup 15 repositioning will not result in any visible deficiency when decoded. Thus the final output image stream will appear to be continuous or seamless to the viewer. Bitstream buffer memory 60A is part of an exemplary 16 megabit DRAM memory. A further

exemplary 16 megabit SDRAM memory block is partitioned to provide frame buffers 60C and 60D which provide storage for at least two decoded image frames, compressed video bit stream storage in buffer 60B prior to decoding, an audio bit stream buffer 60E and other storage in buffers 60F, G and H. The channel processor 40 also includes timing control circuitry which control writing by link 505 to bitstream buffer 60A. Data may be intermittently written to the bitstream buffer as a consequence of changes in replay track addresses, for example, resulting from user defined replay video content such as a "Directors cut", parental guidance selection, or even user selectable alternative shot angles. To facilitate more rapid access and recovery of the recorded signal, disk 14 may be rotated at an increased speed resulting in the transduced bitstream having a higher bit rate, and possibly intermittent delivery.

As has been described, the recorded data stream is arranged in ECC blocks of 16 sectors. Each sector has a unique sector identification address which is protected with error correction bits that are processed by ECC block 47 of FIGURE 4. However, because the sector address is short and sector specific, any delay to sector address signal 42 resulting from error correction processing block 47 is insignificant. Sector address signal 42 is coupled to provide positional information to servo control integrated circuit 50. Integrated circuit 50 provides drive and control signals for servo motors 11 and 12. Motor 12 rotates disk 14 and provides servo controlled rotation at a plurality of speeds. The opto pickup or transducer 15 is positioned and servo controlled by motor 11 responsive to sector address signal 42, and in addition, may be controlled to rapidly reposition or jump to another sector address, or location on the disk surface in response to a sector address request, transmitted by I^2C control bus 514, and coupled via element 54 of FIGURE 4.

The digital video disk player is controlled by a central processing unit or CPU, element 510 of block 500, which accepts the reproduced bitstream and error flags from channel IC 40, and provides control instructions to servo IC 50. In addition CPU 510 accepts user control commands from user interface 90, and MPEG decoder control functions from the MPEG decoder element 530 of block 500. A system buffer memory 80 is addressed by and provides

data to CPU 510. For example, buffer 80 may comprise both RAM and PROM memory locations. The RAM may be used to store various data extracted from bitstream 41 by CPU 510, for example such data may include descrambling or decryption information, bitstream and frame buffer memory management data, and navigation data. The PROM may, for example contain advantageous transducer jump algorithms which facilitate trick mode operation at a selection of speeds in forward or reverse directions.

The MPEG encoded bitstream is coupled to link processor 505 in FIGURE 3, which may function as a hardware demultiplexor to separate MPEG encoded audio, video and control information from the DVD formatted bitstream. Alternatively, bitstream demultiplexing may be accomplished by software control of direct memory access or DMA of buffer 60A, from CPU 510 of FIGURE 3. The encoded bitstream prior to or within track buffer 60A is searched by microcontroller 510 to locate and read headers and to extract navigation data. Advantageous bit stream searching will be discussed with reference to FIGURE 6.

Microcontroller 510 is coupled the front end via I^2C control bus signal 514 to control or request transducer repositioning to acquire the next sector required by a trick play sequence. The transducer positioning may be controlled by an advantageous stored sequence, or jump play pattern which is indexed with reference to replayed sector addresses and GOP sector addresses read from navigation pack data contained in each video object unit or VOBU. Exemplary sector addresses and VOBU navigation pack are depicted in FIGURE 5A. However, following transducer repositioning, the sectors initially retrieved from the front end may be identified by exemplary microcontroller 510 as not those requested by the jump instruction. Thus, microcontroller 510 advantageously overwrites this unwanted data in track buffer 60A and ensures that only the requested data is present in the buffer.

Having identified sector addresses or headers, microcontroller 510 controls direct memory access of buffer 60A which effectively separates MPEG data from other DVD formatted data stored in the buffer. Thus, video DMA 515 separates compressed video bits which are coupled for storage in exemplary video bit buffer 60B. Similarly compressed audio bits are read from buffer 60A and

stored in audio buffer 60E. Sub-picture data is also retrieved from track buffer 60A by DMA and stored in buffer 60F.

The compressed video bit stream in video bit buffer 60B is searched to locate picture or higher level start codes by start code detector 520. A detected start code signal 512 is coupled to microcontroller 510 which then communicates with MPEG decoder 530, via signal 511, to indicate the next picture type, the quantizer setting and to initiate decoding. A decoder status signal 513 is coupled back to microcontroller 510 to indicate the completion of decoding and that picture data available for display or storage. Compressed video bit buffer 60B may be considered to function as a FIFO or circular buffer where the stored bitstream is sequentially accessed for MPEG decoding, however, trick mode operation may be advantageously facilitated by random access of buffer 60B, as will be described.

Within MPEG decoder 530 the video bit stream is processed by a variable length decoder 531 which searches the bitstream to locate slice and macro-block start codes. Certain decoded pictures from each group of pictures are written to frame buffers 60C and 60D for subsequent use as predictors when deriving or constructing other pictures, for example P and B pictures, of the GOP. Frame buffers 60C and 60D have a storage capacity of at least two video frames. Separated audio packets are stored in audio bit buffer 60E which is read out and coupled for audio decoding in block 110. Following MPEG or AC3 audio decoding a digitized audio signal results which is coupled to an audio post processor 130 for digital to analog conversion and generation of various base band audio signal outputs. A digital video output signal is transformed into raster scan format by display buffer 580 from decoded blocks read from reference frame buffer 60C/D. However, during trick mode operation the output signal source may be a field memory advantageously reconfigured from memory unused during tick mode operation. Thus block to raster scan conversion within display buffer 580 may be advantageously controlled responsive to trick mode operation. The display buffer is coupled to encoder 590 which provides digital to analog signal conversion and generates baseband video components and encoded video signals.

Operation of the exemplary video player illustrated in FIGURE 2 may be considered with reference to FIGURE 1B which illustrates a forward play and reverse trick play sequence. As described previously, the coded relationship existing within each GOP necessitates that each group of pictures is decoded in a forward direction starting from an I-frame or picture. Thus, reverse mode features may be provided by effectively jumping back to transduce an earlier, or preceding I picture and then decoding in a forward direction through that GOP. The decoded pictures are stored in frame buffer memories for subsequent read out in reverse order. However, sequences that include B pictures may utilize further advantageous features which will be described. In FIGURE 1B it will be assumed that at some time prior to time t0, for example at I-picture I(1), the exemplary video player assumed a forward play condition in response to a user command. Each group of pictures is decoded in the forward direction as illustrated in FIGURE 1A by the arrow headed lines linking I, B and P frames. At a time prior to time t0, a three times play speed reverse trick mode is selected, and initiated at time t0 where I-picture I(25) is decoded and displayed. As previously described the next picture required for reverse trick play decoding is I-picture I(13), thus the transducer is moved, as indicated by arrow J1 to acquire picture I(13). The signal recovery and decoding then follows a play sequence indicated in FIGURE 1B by arrows J1, to acquire I(13), J2, to acquire P(16), J3, to P(19), J4 to P(22) ... Jn. The intervening B pictures shown in FIGURE 1B are transduced but may be discarded, for example, in the buffer by over writing or by decoder inhibit, as required specific to each trick play mode. To avoid the previously described requirement for additional reverse mode video buffering, various advantageous methods for MPEG decoder, buffer memory control and allocation are employed.

The determination of picture data may be performed in units of sectors referenced in bit stream 41 or track buffer 60A. However, since an MPEG picture start code is buried within DVD data formatting and is not constrained to start coincident with a sector boundary the resulting location of picture start codes in units of sectors may inevitably include fragments of a preceding, possibly non-video sector. FIGURE 5A shows part of exemplary bit stream 41 including a video object unit containing audio video and sub-picture data sectors.

Each sector contains 2048 payload bytes with sector addresses shown shaded at the sector boundary. In FIGURE 5B video picture A is shown ending in sector 54 and is immediately followed by the start code for video picture B. However, the remainder of video picture B start code occurs in sector 65, with intervening sectors 55 - 64 containing sub-picture and audio data. Determination or location of picture data / video sectors in units of sectors is illustrated in FIGURE 5C where a start code for exemplary picture A is shown in sector 2 with the start code of next picture B, occurring in sector 9. Equation 1 shows picture data location by sector count, since picture A starts in sector 2 and ends in sector 9, picture A has a duration of 8 sectors. Unwanted data fragments are illustrated FIGURE 5C, where video data is depicted referenced to (video) sector numbers. However such video sector numbering may be directly related to the sector number or address in the reproduced bit stream. In FIGURE 5C a video bit stream is shown with an exemplary picture A depicted with a picture start code initiated at byte 1000 of video sector 2. Clearly the preceding 999 bytes of sector 2 correspond to data from a preceding picture. It is possible to employ more detailed processing where the picture data is located the units of bytes. Byte accurate processing may require more complexity of memory control than that required for sector level accuracy. However, if byte accurate processing is employed only complete picture data are stored in the video bit buffer, thus fragments are eliminated and hang up of MPEG decoder 530 is avoided. Byte accurate picture determination is shown in FIGURE 5C for exemplary picture A, where a picture start code starts at byte 1000 of video sector 2 and picture B start code starts at byte 500 of sector 9. Hence the size of picture A may be calculated, by use of equation 2, as 13,835 bytes. Thus byte accurate picture addresses allow microprocessor 510 to point to a specific byte in exemplary video bit buffer 60B from which variable length decoder VLD 531, of FIGURE 3, is to start decoding.

If picture data is determined in units of sectors, the MPEG decoder reading pictures from the video bit buffer must be protected from hang up due to fragments of discarded pictures occurring before or after the wanted picture is decoded. Such picture fragments are depicted in exemplary video bit buffer of FIGURE 5D which shows multiple sectors containing P and B pictures where unwanted data

from a previous, or following picture are shown with diagonal shading. Each video object block unit or VOBU includes navigation data that identifies the end sector address of the first I picture and the last sector addresses of two following reference or P pictures of the first GOP of the VOBU. In addition the navigation data includes sector addresses of I-pictures in preceding and succeeding VOBUs, hence an I-picture only trick mode may be readily provided. However, problems resulting from picture fragments may be avoided if the end byte of the wanted picture can be identified. Microprocessor 510/A, for example type ST20, is advantageously configured as a hardware search engine which searches through the data stored in the track buffer to locate the ending byte of the I-picture within the ending sector stored in the buffer 60A. Thus by identifying an I-picture, it alone may be loaded into video bit buffer 60B, hence avoiding the storage of partial pictures which may cause problems of decoder lockup. The exemplary microprocessor 510/A may be employed to find start codes in an I-picture only mode since the ending sector is known from the navigation data. However, for P, B or multiple I-pictures, the exemplary microprocessor may not provide a practical solution since testing has to be performed on every byte of data in the bitstream, which represents an operationally intensive usage of microprocessor 510.

The location and determination of start codes prior to decoding may be facilitated by an arrangement which utilizes the link interface block 505 of FIGURE 3 to search for start codes in the bitstream prior to track buffer 60A. Such use of link interface 505 advantageously provides early pre-processing or parsing for picture and or audio headers which may be signaled to microprocessor 510. Thus, having identified headers in the incoming bitstream prior to the track buffer, pictures and audio required by a specific trick mode may be stored in exemplary track buffer 60A with unwanted pictures and or other data deleted in the buffer by overwriting.

In a first arrangement start codes are located by use of start code detector 520 which searches the bit stream in either the mechanical / track buffer 60A or the video bit buffer 60B. Although this method has an advantage in that MPEG start code detector design is known, the detector however requires contiguous data. Hence only data in the video bit buffer, stripped of DVD and transport data

structure may be searched. Thus searching for MPEG data within the mechanical/track buffer may be difficult to facilitate, may not optimally use memory, and exemplary microprocessor 510 may be heavily loaded with interrupts, thus requiring the addition of a second microprocessor for example, 510A specifically to implement start code detection.

In an advantageous arrangement, start code detection is facilitated by a start code detector which searches the bit stream exclusively for MPEG start codes prior to, or within track buffer 60A. Thus by advantageously providing early parsing for MPEG video headers within the bit stream, trick play picture requirements may be anticipated and memory manipulation specific to trick play operation may be performed. The same advantageous parsing may be applied to the video packet stream prior to the video bit buffer during trick mode operation. For example, in a reverse replay mode, such pre-processing permits trick play specific selection between pictures to be buffered for decoding, and those unwanted pictures to be discarded before storage. Such picture selection, for example discarding B-frames, may approximately double the number of I and P pictures stored in exemplary video bit buffer 60B during trick play operation. Thus the identification of wanted from unwanted data is a direct consequence of pre-processing or parsing prior to buffer storage which allows video bit buffer 60B to store only wanted, or trick play specific pictures. Hence more trick play specific video object units or VOBUs may be stored facilitating smooth trick play motion rendition.

In an advantageous arrangement the storage capacity track buffer 60A and video bit buffer 60B are increased during a trick play mode by only selecting for storage data that is to be used subsequently. For example, in an exemplary trick play mode B frames may not be decoded, hence need not be stored in the track or video bit buffers. Thus only needed pictures are stored, and unwanted picture or other data is discarded. To facilitate this advantageous selection between wanted and unwanted pictures requires that the bit stream or video packet stream be pre-processed, parsed or searched to locate a sequence_header, group_of_picture_header or picture_header prior to storage. Thus parsing or pre-processing of the compressed bit stream allows the determination of MPEG parameters such as, time_code, closed_gop,

and broken_link data for each group of pictures or GOP. In addition, by pre-processing the packet stream the picture_start_code may be located thus permitting processing of the picture_header which in turn allows the determination of, for example, the temporal_reference, picture_coding_type (I, P and B). However, such advantageous MPEG parsing is difficult, as has been described, due to DVD partitioning MPEG like data into sectors of 2048 bytes. In addition, because the MPEG start codes (4 bytes) are not sector aligned, an exemplary picture start code may be distributed across a sector boundary. FIGURE 5B illustrates a bitstream prior to track buffer 60A where video picture A ends in sector 54 and is immediately followed by the start code for video picture B. However, the remainder of video picture B start code occurs in sector 65, with intervening sectors 55 - 64 containing sub-picture and audio data. FIGURE 5C illustrates a demultiplexed video sector bitstream prior to video bit buffer 60B where a start code for exemplary picture A is shown in sector 2 with the start code of next picture B, occurring in sector 9. A distributed start code occurs for picture C which is initiated at byte 2046 of sector 12 and continues in sector 13. Hence, part of the start code is in one video sector with the remainder in the next video sector.

To enable a bitstream with distributed start codes to be parsed an inventive exemplary method is shown in FIGURE 6. The exemplary method identifies and saves sector types and addresses, and in addition identifies and saves wanted start codes. Distributed or partial start codes are identified and saved by the use of an inventive partial start code flag which indicates the occurrence. The remainder of the start code occurring in the next video sector is identified and recovered to complete start code. The inventive method of FIGURE 6, depicts searching and MPEG parsing applied to bit stream 41 prior to track buffering. The bit stream is searched for wanted sectors, for example a video sector, which is then searched for distributed start codes. A distributed start code may be separated by other non-video sectors containing for example audio, sub-pictures, navigation data etc. Thus the bit stream is searched and the subsequent video sector identified and processed, while the intervening non-video sectors, not currently required, for example during a specific trick mode, are not processed and may be discarded

prior to storage or over written in exemplary track buffer 60A. Thus having identified the next video sector, the packet data is searched to locate the next start code. However, because the partial start code flag is set, the remainder of the partial start code is searched for, and with its occurrence this remainder is combined with that of the preceding video sector to complete the start code.

The exemplary chart in FIGURE 6 illustrates the inventive method employed for bit stream searching to identify wanted sector addresses, picture types and addresses, and for detecting and reassembling distributed start codes. The method starts at step 10 where an error corrected bitstream is searched to locate specific wanted sectors from a plurality of sectors including, navigation, audio video sector sub-picture data sectors. A video sector is detected at step 100 where a NO result forms a loop which continues the bitstream search. Similarly, an audio sector may be detected at step 105 and its sector address stored accordingly. If step 100 tests YES, a video sector is detected and the sector address is stored at step 101. A detected video sector initiates a further test at step 200 to detect a start code within the video sector. Step 200 depicts picture start code, however, various start codes may be present, for example sequence-headers, GOP headers or picture-headers all exist within the video sector hence any may suffer distribution across a sector boundary. A NO at step 200 forms a loop which continues to search for a start code within the video sector. A YES at step 200 indicates detection of a start code which initiates a further test to detect a partial start code at step 250. The determination between partial and complete start codes depicted at steps 200 and 250 may be considered to occur both concurrently and serially since any start code becomes partial or incomplete when interrupted by an occurrence of a sector boundary and sector address, as illustrated in FIGURES 5B and 5C. A NO at step 250 forms a loop to wait for a partial start code occurrence. In addition, the NO at step 250 also indicates detection of a complete start code which is tested at step 255 to determine if it is a wanted type. Wanted start codes test YES at step 255 which results in the storage of the type and byte location within the sector address at step 260.

Detection of a partial start results in a YES at step 250 which causes the sequence to restart searching the bitstream to locate the

next video sector by looping back to step 100. The YES at step 250 also initiates a test at step 300 to determine if a partial start code flag is set. The partial start code flag is not set until a first distributed or partial start code is detected. Thus NO at step 300 sets the partial start code flag at step 350, and in addition stores the value of the partial start code at step 400. A YES at test 300 indicates detection of the remainder or residue of the distributed start code and results in resetting the partial start code flag at step 500. The YES at step 300 also results in storage of the detected start code remainder at step 450. At step 550 the values of the partial start code from step 400 and its remainder from step 450 are combined to reform the distributed start code. Finally at step 575 the reformed start code type, byte and sector address are stored. Hence the inventive method described identifies and stores specific sector types and addresses, identifies and stores start code types and byte addresses within sectors, and identifies and reassembles distributed start code fragments. Thus a DVD format bit stream may be parsed to determine for example, specific MPEG coded picture types, prior to buffer storage.

It is advantageous to control MPEG picture decoding order based on knowledge of where the pictures start and stop in the video bit buffer. Thus knowledge of picture location in the video bit buffer 60B, for example as illustrated in FIGURE 5C or as determined by bitstream search of FIGURE 6 permits memory start pointers in the start code detector 520 and variable length detector 531 to be advantageously directed to randomly access pictures as required, for example, during trick mode operation. Operation in reverse at play speed and or slow motion playback requires the reproduction of B-frames. Such reverse mode operation may be advantageously simplified in terms of buffer memory requirements by reversing the order in which adjacent B pictures are decoded. This reversal of decoding order is advantageously achieved by setting the memory start pointers to enable decoding of the picture required by the trick mode. In addition buffer memory size and control may be simplified during trick play operation by advantageously skipping or not reading pictures in the video bit buffer as required by specific trick play algorithms. Memory size and control may be further optimized during trick play buffer by advantageously enabling multiple

decoding of pictures either immediately or as specifically required by the trick play algorithm. The provision of these advantageous features requires careful control of read/write functions and the synchronization therebetween.

During trick mode operation, and particularly during reverse play speed operation, maximized picture buffer capacity is required to store a group of pictures for read out in reverse order. During such trick modes certain player functions or features may not be required, may be non-useful or unavailable. Such functions or features include audio, multiple languages, sub-pictures and on screen displays and all utilize buffer memory capacity. Thus buffer memory capacity unused by these functions or features may be reallocated during trick mode operation to provide additional picture storage. However, during certain trick modes, for example a fast play mode, there may be a beneficial requirement for the accompanying audio to be reproduced at high speed, and pitch corrected to assist in scene location. In addition a limited on screen display may be required to indicate trick play speed and direction. Thus unused buffer memory capacity may be dynamically reconfigured to advantageously facilitate trick mode buffering for compressed pictures, decoded frame predictors, and video display fields.

In an inventive arrangement SDRAM buffer memory 60E - H is functionally reallocated between operation in forward and trick play modes. The memory capacity allocated during forward play mode to audio 60E, sub-picture 60G may be used during trick play to provide additional compressed picture storage, to augment video bit buffer 60B and to provide an additional predictor frame for decoding. Similarly, buffer memory may be reallocated for example, for certain trick play modes storage of extra compressed pictures may not be required, thus unused or non-required buffer memory capacity is reconfigured to provide an output display buffer memory, depicted as 60H in FIGURE 3. The output display buffer memory may store either a frame or field of video data for display. This dynamically allocated memory facilitates output picture derivation and is not used as a predictor, thus simplifying memory management during trick mode operation. The reallocation of memory may be initiated by user selection, however the dynamic allocation may be determined by advantageous stored trick play sequence requirement and or use of

advantageous picture anticipation derived from bit stream parsed identification of compressed picture type, as has been described.

In a further advantageous arrangement, frame buffer memory capacity may be effectively be doubled during trick play operation by horizontally sub-sampling the decoded picture data prior to buffer storage. Horizontal sub-sampling, for example implemented by exemplary block 62 averages horizontally adjacent pixel pair values responsive to a trick mode control command from controller 510. In FIGURE 3 signal S1 represents full bandwidth data coupled to sub-sampler 62 with the subsampled output data represented by signal S2. Thus the sub-sampled picture contains approximately half the original number of pixels, and hence requires half the memory capacity allowing a picture, or video frame, to be stored in the capacity of a field. Thus by horizontally sub-sampling during trick play operation additional frame buffer storage is available as required by a trick play algorithm. In addition to increasing trick mode memory capacity, the inventive use of sub-sampling beneficially reduces data and address bus control by a memory manager during trick mode memory access. For example only half the data is communicated for half the time hence simplifying memory control and management.

The horizontally sub-sampled picture is read from memory, for example 60C, D or inventively reallocated buffer H to be restored by sub-sampler 62. In FIGURE 3 signal S3 represents sub-sampled reference picture data read from memory for pixel count restoration. Sub-sampler 62 may address each sub-sampled memory location twice, however this action doubles data and address bus utilization which was beneficially reduced during the storage process. Hence the sub-sampled picture is restored by duplicating each pixel value and output as signal S4 for coupling directly MPEG decoder 530 to prior to MPEG decoding. Although this method doubles buffer capacity, and reduces both data and address bus utilization, horizontal spatial resolution is reduced. However, this reduction in horizontal resolution occurs during trick play operation, and with increased image motion rates, human psycho-visual perception may rendered the reduction imperceptible.

The block diagram of FIGURE 4 shows the same functions and element numbering as those depicted in FIGURE 2, however, FIGURE 4 includes additional inventive arrangements which will be explained.

The exemplary digital video disk player shown in FIGURES 2, 3 and 4 may be considered to comprise two parts namely a front end and a back end. The front end controls the disk and transducer with the back end providing MPEG decoding and overall control. Such functional partitioning may represent an obvious solution for consistent, steady state, MPEG decoding. However, with such partitioning of processing and control at the back end the microcontroller may become overloaded, for example, during trick mode operation and in particular when playing in the reverse direction.

As has been described, microcontroller 510 is required to manage the incoming bitstream 41 received from the front end and identify wanted from unwanted data. In a first advantageous arrangement bitstream 41 is controllably coupled between the front and back ends. In the exemplary player of FIGURE 2 opto-pickup or transducer 15 may be repositioned, as has been described. Sector addresses derived in the back end are sent via an I^2C control bus 514 to the front end servo system 50 to reposition transducer 15. However, the opto-pickup or transducer 15 is servo controlled responsive to a sector address which is truncated to remove the least significant digit. This address truncation allows acquisition of sectors in groups or blocks of 16 sectors. This grouping is required to facilitate error correction (ECC) by means of Reed Solomon product coding and payload data interleaving applied over 16 sectors during recording. Thus information is acquired from the disk in ECC groups of 16 sectors, and in general, the retrieved data containing the wanted sector address is in advance, or preceding that address requested by the back end processing. In addition, the transducer moves relative to the rotating disk with either radial or tangential motion to acquire the track containing the ECC block of sectors within which the wanted sector address or addresses reside. Thus, following repositioning, the transducer refocusses and sectors are transduced as the disk rotates towards the ECC sector block containing the requested or wanted sectors address. Hence, if worst case positioning of transducer and wanted sector address are considered, many hundreds of unwanted

sectors may be transduced. The since the number of sectors increases with increasing disk radius, so too will the number of unwanted sectors reproduced. In addition acquisition of an earlier or preceding address may possibly require a complete disk revolution with resulting unwanted sector reproduction. Thus very significant amounts of unwanted data are produced prior to the occurrence of the wanted sector address. This bit stream is depicted in FIGURE 4 as signal 44, and contains both wanted and unwanted data which is coupled for error correction at ECC blocks 45 and 46. The error corrected bitstream is output from ECC processing as signal 41 which is coupled to the back end where microcontroller 510 identifies wanted from unwanted data.

An inventive arrangement is shown in FIGURE 4, where data signal 44 output from an 8:16 code demodulator and is coupled via a control element 45A, for example a transmission gate, or logic function, to Reed Solomon error correction blocks 45 and 46. Control element 45A is controlled by element 43 which functions to compare the recovered, current replay sector address, error corrected in block 47 and output as address signal 42, with a sector address 53A, derived from the back end, which represents the next wanted data, for example picture type. The comparison may be facilitated by a comparitor or logical function. Thus when the replay sector address 42 equals address 53A requested by the back end, the demodulated data output is enabled by signal 43A for coupling to error correction buffer blocks ECC 45 and 46. Since error correction is applied to groups of 16 sectors, the comparison of requested address with actual address is performed such that the ECC block of sectors containing the wanted sector is enabled for Reed Solomon correction. For example, sector address comparison may be facilitated with addresses having a least significant bit truncated.

Since, for example, a B type MPEG picture may occupy 3 sectors where as an I type MPEG picture may require 30 sectors or more, the requested sector address represents the initial data sector of a wanted picture type. In addition signal 43A, which represents substantial equality between wanted and replay sector addresses, may be considered to represent a latch function where the logical state is maintained until the wanted address is changed i.e. until a further transducer jump is requested. The receipt of a new sector

address changes the state of signal 43A, which inhibits reproduced data until the new wanted address occurs in the replay signal and is detected by comparitor 43. Stated differently, signal 44 remains enabled for error correction, ECC blocks 45 and 46 are enabled and output signal 41 is sustained, or in simple terms, the disk continues to play until a different transducer position is requested.

The detected replay occurrence of the wanted sector may be performed by comparison with truncated sector addresses to ensure that error correction buffers 45 and 46 are filled with the number of sectors required for RS correction. In a further embodiment, the same detected replay occurrence may be employed using signal 45B to control or enable operation of error correction buffer memory 45 and 46. In an alternative inventive arrangement only the requested sector is enabled via output control element 46A. Selection by element 46A is different from the control provided by elements 45A and 45B which, because of the interleaved, or shuffled data format enable the ECC block containing the requested sector. Detection of the wanted replay sector may be performed by comparison of the actual replay sector address and the requested or wanted address. However, because this control function is performed essentially following error correction and de-shuffling which utilize buffer memory, the resultant output signal 41 is delayed by at least one ECC block time period. Hence error corrected output data corresponds to groups of sectors transduced in advance of the wanted data (address) identified as present at the ECC buffer input. Clearly since the buffer delay is known it may be compensated for in the control coupling of signal 43A to element 46A, for example by use of a delaying method depicted as t. Control element 46A is depicted as a series switch element capable of enabling or disabling bitstream supply to the back end. Thus signal 43A, suitably timed to compensate processing and buffer delays, may be applied to selectively enable de-interleaving bitsream 41 for transmission to processing block 500. The use of the preceding inventive embodiments permits only transduced data from requested sectors to be coupled to the back end for storage and decoding, thus reducing microcontroller 510 work load.

As has been described, transduced signal 31 is demodulated at block 40 to remove the 8:16 modulation, and produce output signals 44 and 44A. Signal 44 is coupled for de-interleaving and error

correction, with signal 44A being separately error corrected to produce replay sector addresses. De-interleaving and error correction is performed in ECC buffer memories 45, and 46 of FIGURE 4. Each buffer stores 16 sectors of the replay data stream arranged as an array to facilitate de-interleaving and to enable the required row and column product processing. The cascaded ECC buffer memories introduce a delay to reproduced serial bit stream which, at 1X rotational speed, may be approximated to with the following calculation (2 * 16 * 1.4) milliseconds, where 2 represents ECC buffers 45 and 46, 16 represents the sectors over which the correction is applied and 1.4 milliseconds represents the period of a sector at 1X rotational speed. Thus the reproduced serial bit stream is delayed by a minimum of approximately 45 milliseconds.

Bitstream 44A is processed at ECC block 47 to error correct sector identification addresses. However, because the sector address is short and sector specific, error correction block 47 introduces an insignificant delay to the replay sector address signal 42.

As described already, the error corrected bitstream is subject to an error correction delay. Bitstream 41 is received at the back end where the various MPEG packets are separated from DVD data. Video packets are stored in exemplary buffer 60B for decoding by MPEG decoder 530. As described previously, decoder 530 sends signal 513 to controller 510 to indicate completion of each picture decoded, which in turn results in the acquisition of the next picture to be decoded. Hence at the end of a particular picture, for example, the picture contained in video sector marked A in FIGURE 5A, signal 513 is generated by the decoder. An exemplary next picture wanted for decoding must be recovered from the disk, hence transducer 15 must be repositioned to the sector address containing the wanted picture. FIGURE 5A shows part of bitstream 41, coupled to buffer 60A, including a video object unit composed of multiple sectors each containing video, audio, sub-picture and navigation data. The end of sector A, may be advantageously determined in, or prior to, track buffer 60A by the occurrence of the next sector address, or following MPEG decoding as indicated by signal 513. Hence the arrow labeled NEXT in FIGURE 5A shows the approximate timed occurrence of the next sector address request from microcontroller 510 to the front end. This address and jump request is transmitted by an I^2C control bus

which, depending on interrupt prioritization delays issuance of the wanted sector request.

In a further advantageous arrangement, interrupt prioritization of microcontroller 510 interrupts are reordered between operational modes. For example, in a forward play mode memory addressing and control requirements are different to those required for operation in trick modes, and in particular during operation at play speed in reverse. During trick mode operation certain features, and consequently their memory and MPEG decoder control are not required. For example, audio decoding, and sub-picture processing are not required during trick mode operation hence address, data and control bus interrupt priorities may be assigned a lower priority with a higher priority assigned to picture access from the track and video bit buffers.

The timely acquisition of requested sectors is particularly important during trick mode operation. However, the execution of wanted sector acquisition responsive to back end processing, forms a control loop with multiple delay elements, as has been described. An inventive arrangement is shown in FIGURE 4 which reduces delay in sector acquisition, which stated simply, permits a detected replay occurrence of a last wanted sector to initiate transducer movement to a previously received new sector address. FIGURE 5A shows arrow B positioned to indicate an approximate time relationship between replayed bit stream 41, or track buffer 60A, and the issuance to the servo of inventive next/end sector addresses. In FIGURE 5A arrow B is shown occurring shortly after the navigation pack, shown shaded, has been read from the bitstream. At picture A,. arrow NEXT is shown to illustrate the occurrence, approximately seven sectors later, of signal 513 (decode completed). However, in reality I and P type pictures contain considerably more sectors than those depicted in FIGURE 5A, hence arrow NEXT, corresponding to issuance of an address and jump request, occurs considerably later than illustrated. Thus the inventive next/end sector addresses are generated by microcontroller 510 following navigation pack acquisition and or advantageous picture / sector address determination and table construction. The employment of next/end sector addresses recognizes that the wanted sector address may be temporally separated from the transducer instruction to jump. The next/end

sector addresses are effectively pre-loaded in the transducer servo system with the transducer jump executed in response to the reproduction of the first unwanted sector address. Since the sector addresses are not subject to the lengthy ECC delay of bitstream 41, the transducer is moved before the last wanted sector emerges from ECC blocks 45 and 46.

In FIGURE 4 control data is transmitted by an I^2C control bus 514, which communicates the next wanted replay sector address to servo control system 50. The next wanted replay sector address is generated by microcontroller 510 which processes address data originating from a stored trick play, speed specific sequence, replayed and stored navigation data, or from advantageously determined replayed picture data. The next address is read from the I^2C bus and stored in element 53. The I^2C data also includes an inventive end/last sector address, or first unwanted sector address. The end/last sector address may be obtained from recovered and stored navigation data, however this provides only a limited number of predetermined picture addresses, thus for trick modes the advantageously determined end of picture sector addresses are employed. The end/last sector address is read from the I^2C bus and stored in element 52. The last sector address may modified either prior to bus transmission or upon receipt, to prevent wanted sector loss, by for example, the addition of one unit count to sector address thus ensuring addressing and detection of the first unwanted sector. The last sector address, or modified address 52A is coupled for comparison with the replay sector address signal 42 in an exemplary comparitor 51. Thus, when the replay sector address 42 equals address 52A, the first unwanted sector is about to be transduced and comparitor 51 generates control signal 51A. Control signal 51A enables coupling from element 53, for example by loading or shifting the stored address data to the servo, or as depicted by exemplary selector switch 54 which couples the next sector address to the servo system and initiates repositioning of transducer 15. As has been described, the transducer is moved to the track containing the next wanted picture and data output signal 41 is advantageously enabled by element 43 when the wanted picture is reproduced.

The transducer continues to follow the track reproducing wanted sectors which are processed by the back end. In response to

data recovered from these sectors a new pair of next and end sector addresses are generated and transmitted via the I^2C bus. These new address are received and stored as before in elements 52 and 53. However to avoid initiating a transducer jump before the new end sector address is replayed and detected by element 51, exemplary selector 54 is reset or opened preventing premature initiation and acquisition of the new sector address.

The inventive transducer control sequence described above initiates transducer movement by comparison between essentially undelayed replay sector addresses and pre-loaded wanted sector addresses, thus delay in the acquisition of the new replay bitstream is obviated, facilitating enhanced trick mode operation.

MPEG picture decoding order is determined, as is well known, by the encoded picture hierarchy, hence forward mode operation the decoding sequence is followed. However, trick play operation may be advantageously facilitated by controlling MPEG picture decoding order based on picture sequences required by a predetermined trick play algorithm and knowledge of where the pictures start and stop in the video bit buffer. Thus knowledge of picture location in the video bit buffer 60B, for example as calculated in FIGURE 5C, or as determined by bitstream search of FIGURE 6, permits memory start pointers in the start code detector 520 and variable length detector 531 to be advantageously directed to randomly access pictures as required, for example, during trick mode operation. An exemplary video bit buffer is shown FIGURE 5D containing picture fragments as described previously. A start code detector memory pointer is depicted as arrow SCD which searches through the exemplary video bit buffer to locate MPEG start codes. However in the third sector of the first P picture the start code detector memory pointer SCD1 indicates detection of a start code from the next, but unwanted picture. Hence by advantageously directing the start code memory pointer to known byte accurate memory locations unwanted pictures and undesirable decoder hang ups are avoided, as is indicated by arrow SCD2 of FIGURE 5D.

In a further advantageous trick mode arrangement, unwanted data from previous pictures is cleared input and output FIFOs, first in first out registers of start code detector (SCD) 520 and variable length decoder (VLD) 531. Signals 521/532 depicted in FIGURE 3 clear or

reset respective FIFOs to purge data remaining from previous decode operations. Such clearance or flushing of the FIFOs ensures that the SCD and VLD start the next decode operation with new data from exemplary bit buffer 60B thus eliminating a further source of decoder mis-operation resulting from residual prior data.

Operation in reverse at play speed requires the reproduction of B-frames and in a further trick mode optimization reverse mode operation is advantageously simplified in terms of buffer memory requirements by reversing the order in which adjacent B pictures are decoded. This advantageous reversal of decoding order is achieved by setting or controlling the memory start pointers to enable decoding of specific pictures required by the trick mode. In another trick mode optimization, buffer memory size and control may be simplified during trick play operation by advantageously skipping or not reading pictures in the video bit buffer by address manipulation as required by specific trick play algorithms. Memory size and control may be further optimized during trick play by advantageously enabling multiple decoding of pictures either immediately or as specifically required by the trick play algorithm. The provision of these advantageous features requires careful control of read/write functions and the synchronization therebetween.

In yet a further trick mode optimization, a decoder control capability which facilitates audio video synchronization or lip-syncing by skipping picture decoding is advantageous increased in control range and utilized during trick mode operation to allow a number of pictures, selectable between 2 and at least 6 to be skipped or not decoded. Such picture manipulation advantageous facilitates trick play operation at six times play speed by skipping over B-pictures within each GOP.

In addition to memory control and allocation requirements for trick mode operation, MPEG decoding may be advantageously optimized, for example, by an essentially concurrent operation of decoding I or P pictures and writing the decoded result for either display and or memory storage within a field period. An ability to decode B type pictures without use of buffer memory is assumed. Such B type picture decoding is known as B frames-on-the-fly (BOF). In addition trick play operation may be advantageously enhanced by writing a decoded field to memory and concurrently reading a display

field from an interlaced location within the same memory. The display field may be from a temporally separate picture. Such virtually simultaneous read write operation may be accomplished within a display field period. However, the decoded field must not overwrite or interfere with the display field readout. This interlaced read write operation is not required for B pictures due to the ability to decode without buffer storage.

In an exemplary player with reverse direction trick play decoding, a bitstream or track buffer 60A is employed to store the compressed MPEG video bitstream recovered from the medium. Track buffer 60A or compressed video bit buffer 60B may be used to facilitate multiple accessing of individual MPEG pictures. The decoded trick play output signal must comply with TV signal standards to enable display by a normal TV receiver. The following example illustrates an inventive control sequence for MPEG decoding in a DVD player. Figure 7 is a chart illustrating an inventive arrangement for a reverse trick play mode of 3-times play speed (3X) in a video player. This exemplary chart has columns which represent MPEG coded I pictures and P pictures which comprise groups of pictures or GOPs A, B, C and D. Each GOP has contains twelve pictures which are not derived from a film source.

In this exemplary trick play sequence, decoding in the reverse direction may be facilitated with an advantageous arrangement of an MPEG decoder and two frame buffers which provide both decoding and display of the decoded video in reverse order. In this example only I pictures and P pictures are decoded, hence only these are charted. FIGURE 7 illustrates a sequence of 37 encoded pictures, with the picture number indicated in parentheses. The extreme right column is labeled "output field #", and represents a time axis incremented in field periods. The first field, output field #1 marks the start of trick play reproduction. Each row of the chart shows the inventive processing occurring within that respective field period. The following abbreviations are used in FIGURE 7. The frame buffers are numbered 1 and 2. An upper-case "D" signifies decoding the picture / frame indicated at the top of the specific column. The process of decoding a picture and storing the result is depicted by "D>1", where the number indicates the destination frame buffer number, i.e. 1. A lower-case "d" indicates the display of a field from

the frame specific to the column. The output field may be selected to preserve the output signal interlace sequence. To provide a continuous output field sequence clearly requires that each chart row contains one field display instruction "d".

The sequence illustrated in FIGURE 7 starts at output field #1, where I-picture I(37) is decoded and stored in frame buffer 1, 60C. Concurrent with the decoding of I picture (37), one field, for example, the top field of I-frame (37) is displayed. An advantageous decoder 530 is employed to facilitate decoding and the concurrent display of the decoded video signal. During output field #2, MPEG picture I(25) is retrieved from bitstream buffer 60B, decoded and stored in frame buffer 2, 60D. At the same time, another field, for example the bottom field of I(37) read from frame buffer 1, 60 C and displayed.

During the period of output field #3, an action takes place which exemplifies an inventive aspect. During field #3 the exemplary top field of I(37) is repeated by reading from frame buffer 1, 60C. Concurrent with the read out of the repeated top field of I(37), predicted picture P(28) is decoded, with reference to I(25), and stored in frame buffer 1, 60C. With accurate, synchronized timing, decoded frame P(28) is written into frame buffer 1, 60C. This concurrent operation is achieved by decoding picture P(28) sequentially on a line-by-line basis following the read out of the display field of picture I(37). The sequential reading and writing of frame buffer 1, is a further advantageous capability provided by this exemplary decoder and memory management system.

At the end of output field #3, pictures I(25) and P(28) of GOP C are stored in frame buffers 1 (60C), and 2 (60D) respectively. However, these frames represent temporally earlier events and are required to enable the decoding of the frames which occurred subsequently, for example frames P(31) and P(34). Intra-coded picture I(25), resident in memory 2 (60D), was utilized to decode frame P(28), and is not currently required. Thus, in order to provide a display for output field #4, frame memory 2 is over written with frame I(37), re-read and decoded from video buffer 60B. To maintain the output interlaced field sequence, the appropriate field of frame I(37) is accessed from frame buffer 2 for display. At output field #5 the advantageous concurrent processing performed at field #3 is repeated. Output field #5 is derived by reading a field of picture

I(37) from frame buffer 2. Simultaneously picture P(31) is decoded with reference to picture P(28), from frame memory 1, and the decoded result is stored in buffer 2. Thus, the first five output fields of this exemplary three times reverse direction replay comprise a still, or frozen image of I-picture (37). However, the end of output field #5, with pictures I(28) and P(31) stored in frame buffers 1 and 2 respectively trick play output signal generation is commenced.

At output field #6, predicted picture P(34) is read from bitstream buffer 60A or video bit buffer 60B, decoded and an appropriate field displayed without storing. Thus field #6 initiates the display of 3 times speed reverse motion. At output field #7, picture P(34) is retrieved again, decoded and the other field selected for display. Picture P(31), previously decoded and stored in frame buffer 2 is read and provides output fields #8 and #9 respectively.

At the end of output field #9 there is no further requirement to store picture P(31), thus intra-coded picture I(13) of the next preceding GOP B is obtained, decoded and stored in frame buffer 2. Output fields #10 and #11 are read from frame buffer 1 which contains predicted picture P(28). Concurrently with the read out of field #11, predicted picture P(16) is obtained from bitstream buffer 60B, decoded and sequentially stored in frame buffer 1. Since both frame buffers contain the anchor frames of the next preceding GOP B, output fields #12 and #13 are derived in the same manner as output fields #6 and #7. Predicted picture P(25) is read from bitstream buffer 60B, decoded and the appropriate field displayed without storing.

Thus the next preceding GOP B, containing pictures I(13), P(16), P(19) and P(22), is processed as described for GOP C.

CLAIMS

1. A method for acquiring a start code from a plurality of start codes in a data stream arranged in a plurality of sectors transduced during reproduction by a digital disk apparatus, comprising the following steps:

a) searching said data stream to locate a specific sector type in said plurality of sectors;

b) searching said specific sector type to locate a start code from said plurality of start codes;

c) determining said start code to be incomplete;

d) searching said data stream to locate a second sector of said specific sector type in said plurality of sectors;

e) searching said second sector of said specific sector type to locate a second start code of said start code type from said plurality of start codes;

f) determining said second start code to be a residue of said incomplete start code;

g) combining said incomplete start code value and said residue start code value to form a complete start code.

2. An apparatus for reproducing a digitally encoded signal from a medium, comprising:

a transducer for transducing said digitally encoded signal and generating a bit stream therefrom;

a processor coupled to receive said bit stream for controllably processing said bit stream;

a memory coupled to said processor for storing processed bit stream information; and

a controller coupled to control said memory and said processor for controlling identification of information within said bit stream;

wherein said controller controls said processor to identify a specific sector type in said bit stream and responsive to said specific sector identification said controller controls said memory for storing said identified specific sector.

3. An apparatus for reproducing a digitally encoded signal from a medium, comprising:

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a transducer for transducing said digitally encoded signal and generating a bit stream therefrom;

a first memory coupled to said transducer for storing said bit stream:

a second memory for storing data controllably coupled from said first memory; and,

a controller coupled to control said first and second memories for controlling identification of information within said bit stream;

wherein said controller controls said first memory to output said bit stream from a specific sector address therein, and said controller controls said second memory to store a first part of said bit stream output from said specific sector address.

4. An apparatus for reproducing a digitally encoded signal from a medium, comprising:

a transducer for transducing said digitally encoded signal and generating a bit stream therefrom;

a memory coupled to said transducer for storing said bit stream;

a processor coupled to said memory for processing said stored bit stream to identify an MPEG start code contained therein;

said processor searches said stored bit stream to identify said MPEG start code and responsive to said MPEG start code identification said processor indicates said identification and stores a sector address of said identified MPEG start code.

5. A method for controlling a transducer position during replay in digital disk apparatus, comprising the following steps:

receiving a first and a second transducer address for controlling said transducer position responsive to a replayed address;

comparing said replayed address with said first transducer address to detect equality therebetween; and

moving said transducer responsive to said detected equality to a new position determined by said second transducer address

6. An apparatus for reproducing a digitally encoded signal from a medium, comprising:

a transducer positionally controlled for transducing said digitally encoded signal; and,

a controller coupled said transducer for controlling a position thereof responsive to said digitally encoded signal and an address coupled thereto, wherein,

responsive to said digitally encoded signal and said address being substantially equal said controller controls said transducer to a second position determined by a second address.

7. An apparatus for reproducing a digitally encoded signal from a medium, comprising:

a transducer positionally controlled for transducing said digitally encoded signal;

a first controller coupled said transducer for controlling a position thereof responsive to said digitally encoded signal and an address coupled thereto; and

a comparitor for comparing said digitally encoded signal and a first address, and coupled to said controller for changing said transducer position,

wherein responsive to said digitally encoded signal and a first address being equal said comparitor controls changes said transducer to a second position determined by a second address.

8. A method for controlling data reproduced in sectors by a disk player employing optical read out, comprising the following steps:

transducing groups of sectors including a sector wanted for processing, and sectors unwanted for processing;

supplying said wanted sector exclusive of said unwanted sectors to a data processor for processing; and,

processing said wanted sector to extract data therein representative of video information.

9. A method for controlling MPEG compatible data reproduced in sectors, comprising the following steps:

transducing groups of sectors including a requested sector having MPEG compatible data required for processing, and

unrequested sectors having MPEG compatible data not required for processing;

transmitting said requested sector exclusive of said unrequested sectors to a data processor for processing; and,

processing said requested sector to extract said required MPEG compatible data representative of video information.

10. A digital disk player for reproducing sectors containing MPEG compatible data, comprising:

a transducer for transducing from a disk groups of sectors including a requested sector having MPEG compatible data required for processing and unrequested sectors having MPEG compatible data not required for processing;

a first data processor coupled to said transducer for processing and coupling said requested sector having MPEG compatible data exclusive of said unrequested sectors having MPEG compatible data not required for processing; and,

a second processor coupled to said first processor for receiving said requested data sectors and extracting said required MPEG compatible data representative of video information.

11. An apparatus for optically reproducing a digitally encoded signal from a disk, comprising:

a transducer positionally controlled for transducing said digitally encoded signal having an address and other data;

a controller coupled said transducer for controlling a position thereof responsive to said address and a requested address coupled thereto; and,

a processor coupled to receive said digitally encoded signal from said transducer and controllably coupled to said controller for controlling processing of said encoded signal,

wherein responsive to said address and said requested address being substantially equal said controller enables said processing.

12. An apparatus for optically reproducing a digitally encoded signal from a disk, comprising:

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a transducer positionally controlled for transducing said digitally encoded signal having an address and other data;

a controller coupled said transducer for controlling a position thereof responsive to said address and a requested address coupled thereto; and,

a processor coupled to receive said digitally encoded signal from said transducer and controllably coupled to said controller for controlling processing of said encoded signal,

wherein responsive to receiving a requested address, said controller disables said processing of said encoded signal until said address and said requested address are substantially equal.

13. An apparatus for reproducing a digitally encoded signal from a disk medium, comprising:

a source of a bitstream representative of said digitally encoded signal;

a processor coupled to said bitstream for processing said bitstream to extract at least a first and a second data type represented therein;

a memory controllably coupled to said processor for storing one of said first and a second data types; and,

a controller coupled to control allocation of said memory, wherein a first reproducing mode said controller allocates said memory for storing said first data type, and in a second reproducing mode said controller allocates said memory for storing said second data type.

14. An apparatus for reproducing a digitally encoded signal from a disk medium, comprising:

a transducer transduces said digitally encoded signal;

a processor coupled to receive said digitally encoded signal for processing and generating a picture therefrom;

a memory coupled to said processor for storing said picture; and,

a controller coupled to control said memory and said processor wherein a first mode said picture is stored in said memory and in a second mode said picture is sub-sampled and stored in said memory

15. An apparatus for reproducing a digitally encoded signal from a disk medium, comprising:

a source of a bitstream representative of said digitally encoded signal;

a processor coupled to said bitstream for processing said bitstream to extract first and second types of data represented therein;

a memory controllably coupled to said source and said processor for storing said bitstream and said first and second types of data; and,

a controller coupled to control allocation of said memory, wherein a first reproducing mode said controller allocates said memory for storing said bitstream and said first and second data types, and in a second reproducing mode said controller allocates said memory for storing said bitstream and said first data types.

16. An apparatus for reproducing a digitally encoded signal from a disk medium, comprising:

a transducer transduces said digitally encoded signal;

a memory coupled to said transducer for storing said digitally encoded signal;

a decoder responsive to said digitally encoded signal for decoding a picture therefrom;

a controller for said decoder, wherein a first operational mode said controller controls said decoder to read said stored digitally encoded signal from said memory responsive to a first sequence and in a second operational mode said controller controls said decoder to read said stored digitally encoded signal from said memory in a second sequence.

17. An apparatus for reproducing a digitally encoded signal from a disk medium, comprising:

a transducer transduces said digitally encoded signal;

a memory coupled to said transducer for storing said digitally encoded signal;

a decoder responsive to said digitally encoded signal for decoding a picture therefrom;

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a controller for said memory, wherein a first operational mode said controller controls said memory to read said stored digitally encoded signal from said memory responsive to a first sequence and in a second operational mode said controller controls said memory to read said stored digitally encoded signal from said memory in a second sequence.

18. A method for picture decoding and display in an apparatus reproducing from a digital disk in a first operating mode, comprising the steps of:

transducing a digitally encoded signal from said disk;

storing said digitally encoded signal in a first memory;

decoding said digitally encoded signal to produce a picture;

storing said picture in a second memory;

coupling said picture from said second memory for display; and,

controlling said decoding, said storing in said second memory to occur within a field period and said coupling for display occurring during a subsequent field period;

and in a second mode,

transducing said digitally encoded signal from said disk;

storing said digitally encoded signal in said first memory;

decoding said digitally encoded signal to produce said picture;

storing said picture in a second memory;

coupling said picture for display; and,

controlling said decoding, said storing in said second memory and said coupling for display to occur essentially concurrently within a field period.

19 A method for picture decoding and display in an apparatus reproducing from a digital disk, comprising the steps of:

transducing a digitally encoded signal from said disk;

storing said digitally encoded signal in a first memory;

decoding said digitally encoded signal to produce a picture;

storing said picture in a second memory;

coupling said picture from said second memory for display; and,

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controlling said storing in said second memory and said coupling for display to occur substantially concurrently.

20. An apparatus for reproducing a digitally encoded signal from a disk medium, comprising:

a transducer transduces said digitally encoded signal;

a first memory coupled to said transducer for storing said digitally encoded signal;

a decoder responsive to said digitally encoded signal for decoding a picture therefrom;

a second memory for storing said picture and coupling said picture for display; and,

a controller for said decoder and said first and second memories,

wherein a first operational mode, within a field period said controller sequentially controls coupling said stored digitally encoded signal from said first memory to said decoder for picture decoding, and controllably couples said picture to said second memory and in subsequent field period controls coupling of said picture for display and in a second operational mode within a field period said controller controls coupling said stored digitally encoded signal from said first memory to said decoder for picture decoding, and controllably couples said picture to said second memory and concurrently controls coupling of said picture for display.

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