

ABSTRACT

A memory device according to embodiments of the present disclosure may comprise a word line buried in a substrate and extending in a first direction, a bit line contact disposed between word lines, contacting
5 an active area of the substrate, and having at least a portion of a side surface concave toward a center in a second direction perpendicular to the first direction, and a gate capping layer including a first capping portion contacting an upper surface of the word line and a second capping portion positioned on the first capping portion, overlapping with at least a portion
10 of the side surface of the bit line contact in the second direction, and having a width different from a width of the first capping portion.

FIG. 2