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## (54) INFORMATION STORAGE AND PROCESSING

- (71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195 Broadway, New York City, New York State, United States of America, a Corporation organized and existing under the laws of the State of New York, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly escribed in and by the following statement:—

This invention relates to information storage and processing apparatus.

- The term "multidimensional interconnection of logic cells" as used herein indicates that memory and logic functions are performed within a storage facility. Equipment capable of operation in this manner is referred to as a distributed logic arrangement and is known to permit functional simplicity in systems organization. For example, vast amounts of information can be operated upon simultaneously in such an arrangement permitting considerable programming and cycle-time advantages.

- Unfortunately, the practical implementation of such an arrangement is difficult. Typically, attempts have produced arrangements having such a significant amount of additional logic circuitry over and above that necessary to perform the memory function alone that it is economically preferably to perform logic in peripheral equipment physically separate from a conventional memory. A content addressable memory provides a good example of a distributed logic arrangement, promising the above-mentioned advantages in programming and in cycle time. In spite of such advantages, content addressable memories, as a practical matter, are not competitive with, for example, random access memory organizations where the memory and logic operations are physically separated.

Copending application No. 36777/67 (Serial No. 1,187,623) describes an arrangement wherein single wall, reverse-magnetized domains are propagated controllably, by pulses on X and Y oriented propagation conductors, in a sheet of a magnetic material having a preferred direction for flux substantially normal to the plane of the sheet. It has since been discovered that next adjacent single wall domains of such an arrangement exhibit interaction forces which, inter-alia, tend to repel one another as do like charged pith balls.

A single wall domain is bounded by a single domain wall that has a shape independent of the geometry of the magnetic sheet or film or, in other words, a single wall domain, as the term is used herein, is not bounded by an edge of the magnetic sheet or film.

Specifically, it has been discovered that the controlled movement and interaction of single wall domains permit the realization of complete sets of logic functions at arbitrary sites in a memory defined in a sheet of magnetic material in which such single wall domains can be moved controllably.

According to one aspect of the invention there is provided information storage apparatus comprising a sheet of magnetic material having an information representative pattern of presences and absences of single wall domains (as defined herein) at some of a plurality of possible positions, or blocks, for such domains, and means for controlling generation in the sheet of successive patterns of magnetic fields to effect a logic operation between the blocks of at least part of said information representative pattern.

According to another aspect of the invention there is provided information storage apparatus comprising a sheet of magnetic material capable of having single wall domains (as defined herein) established therein at any of a plurality of possible positions, or blocks,

thereof, means energizable to introduce domains for forming an information representative pattern of presences and absences of single wall domains at some of said blocks, and means for controlling generation in the sheet of successive patterns of magnetic fields effective to manipulate at least part of a said information representative pattern established in the sheet so as to accomplish a logic operation between the blocks of that part.

According to a further aspect of the invention there is provided information storage apparatus comprising a sheet of magnetic material having an information representative pattern of presences and absences of single wall domains (as defined herein) at some of a plurality of possible positions, or blocks, for such domains, and means for controlling generation in the sheet of successive patterns of first and second magnetic fields for selectively moving and annihilating, respectively, said domains in a manner to perform a logic operation between the blocks of at least part of said information representative pattern.

The invention is based on the realization that if information is represented in a magnetic sheet as the presence and absence of single wall domains in each of a plurality of multiposition bit locations, the information can be moved about and removed selectively in a manner to provide all logic functions as well as the memory function in response to different pulse programs on propagation conductors, in the absence of any additional structural implementations over and above what is necessary to perform the memory function alone. Removal of a domain may be by annihilation or an equivalent operation. It is known that a distributed logic capability permits the realization of any computer function. A specific recitation of bit capacities and operational parameters hereinafter will indicate the practicality of such an arrangement.

In one embodiment of this invention, X and Y oriented conductors on a magnetic sheet are pulsed in a program to operate a sheet of magnetic material as a content addressable memory. The sheet may comprise a rare earth orthoferriite material. The conductors are organized, illustratively, into sets which divide the memory into operational units, to be defined hereinafter, each including fifty-four possible positions for a single wall domain. By controlled movement of, and interaction between, domains, logic operations may be carried out in each of the operational units. Proper sequencing of field patterns in the magnetic sheet enables the logic operations to be performed and the results of those operations to be collected in prescribed portions of the sheet, permitting the realization of an illustrative content addressable memory operation. An operation such as obtaining a related set of stored items, accordingly, may be performed by programs independent of information

stored in the magnetic material and without the need of sensing any effects occurring in the sheet.

As compared with prior arrangements practical embodiments of the present invention can provide a multi-functional organization in which all computer operations including memory, shift register, arithmetic, etc., functions may be carried out in a relatively simple structure comprising again a single sheet of magnetic material and X and Y oriented propagation conductors for moving single wall domains controllably in X and Y directions.

The principles underlying this invention may be better understood from the following, exemplary, description of apparatus embodying the invention and made with respect to the accompanying drawings, in which:

FIG. 1 is a schematic illustration of a memory arrangement embodying this invention;

FIGS. 2 to 42 are schematic illustrations of portions of the arrangement of FIG. 1 illustrating magnetic configurations therein during operation; and

FIG. 43 is a schematic illustration of a system organization of the memory arrangement of FIG. 1.

FIG. 1 shows a content addressable memory 10 comprising a sheet 11 of magnetic material having a preferred direction of magnetization substantially normal to the plane of the sheet. A first plurality of propagation conductors PY1, PY2, ..., and PY<sub>n</sub> overlie sheet 11 and are connected between a Y driver 12 and ground as shown. A second plurality of propagation conductors PX1, PX2, ..., and PX<sub>m</sub>, oriented conveniently in a direction perpendicular to the first plurality of propagation conductors, also overlie sheet 11. Conductors PX1...PX<sub>m</sub> are connected between an X driver 13 and ground. The propagation conductors may be made conveniently by means of printed circuitry techniques and may take the form of interconnected current loops as disclosed in the aforementioned copending application. Alternatively, and analogously, the conductors may be of a form to produce repetitively varying fields when pulsed.

As will become clear, such a structure can be operated in a more flexible manner to provide a variety of functions as will become clear from the detailed description of the illustrative logic operations and the use thereof in a content addressable memory operation.

In order to so operate the structure, it is necessary to pulse the propagation conductors PY1...PY<sub>n</sub>, and PX1...PX<sub>m</sub> in a programmed fashion. To this end, the X and Y drivers are connected by representative conductors 14 and 15, respectively, to a control circuit 16 which, in turn, is responsive to coded input signals on input conductors designated *i* collectively in FIG. 1.

A utilization circuit 18 also is connected to

the control circuit 16 via a conductor 19. Circuit 18 includes a plurality of inputs each coupled to a different position of sheet 11 in a manner discussed hereinafter.

5 The various circuit elements may be any such elements capable of operating as described hereinafter.

10 The use of the sheet 11 and the propagation conductors and drivers as a two-dimensional shift register is disclosed in the above-mentioned application No. 36777/67. There, various implementations for introducing single wall domains into sheet 11 are discussed. It will be assumed that a source of domains is present in sheet 11 and that pulses applied to the propagation conductors move domains from the source to positions required initially in accordance with the following detailed description in a manner consistent with the teaching in that application.

20 Information is stored herein in sheet 11 as the presence and absence of single wall domains in selected positions as in each of the aforementioned applications. However, for the purposes of the present application, the information is represented as a pattern of single wall domains in bit locations so organized and spaced apart as to enable various logic operations.

30 The various logic operations are discussed first together with pulse programs for performing such operations. Then, various of those logic operations are described in terms of consecutive input pulse programs for providing all match words in memory as is required of content addressable memories. In order to understand the various logic operations, however, it is helpful first to understand fully an illustrative organization and such an organization is now discussed as a basis for the discussion of the logic operations.

40 This organization of the arrangement of FIG. 1 may be understood in terms of imaginary blocks related to the propagation circuit which operates to move single wall domains

in the magnetic sheet. The aforementioned application No. 36777/67, for example, describes interconnected conducting loops which are pulsed in a three-phase manner to move single wall domains in a selected direction. Such interconnected loops are shown in FIG. 2 superimposed on an imaginary arrangement of blocks which provide a handy symbol representing a basic operational unit of the arrangement of FIG. 1 as described hereinafter. The blocks may be thought of as arranged in rows and columns. Propagation conductors including interconnected conducting loops oriented along rows of blocks are designated H (for horizontal), those oriented along columns of blocks being designated V (for vertical). There are six representative H conductors H1...H6 and nine representative V conductors V1...V9 shown. Each representative conductor indicated by the brackets in the figure includes three distinct sets of interconnected conducting loops P1, P2, P3 as designated for conductors H6 and V1. The P1 set couples the first, fourth, ..., blocks; the P2 set couples the second, fifth, ..., blocks; and the P3 set couples the third, sixth, ..., blocks reading from left to right for conductor H6 or from bottom to top for the V1 conductor.

Each block may be designated by the representative propagation conductor and by the phase (P1, P2, or P3) coupled to the magnetic sheet at that block. In this way, the blocks from bottom to top coupled by conductor V1 are designated V1P1, V1P2, V1P3 and then the block designations repeat. The designations of the blocks from left to right along conductor H6 are H6P1, H6P2, H6P3, and then the designations repeat. Each block is, of course, associated with two conductors and, accordingly, may be designated in two ways. The following table shows the designations for each block in a group of eighteen blocks in column I of FIG. 2. Specifying the designations of these two circuits identifies uniquely a block in that set of eighteen blocks.

TABLE I

|              |              |              |
|--------------|--------------|--------------|
| H6P1<br>V1P3 | H6P2<br>V2P3 | H6P3<br>V3P3 |
| H5P1<br>V1P2 | H5P2<br>V2P2 | H5P3<br>V3P2 |
| H4P1<br>V1P1 | H4P2<br>V2P1 | H4P3<br>V3P1 |
| H3P1<br>V1P3 | H3P2<br>V2P3 | H3P3<br>V3P3 |
| H2P1<br>V1P2 | H2P2<br>V2P2 | H2P3<br>V3P2 |
| H1P1<br>V1P1 | H1P2<br>V7P1 | H1P3<br>V3P1 |

This table establishes a set of unique correspondences between the various imaginary blocks of a set of eighteen blocks as shown in FIG. 2 and the H and V propagation conductors which couple those blocks.

Such a set of eighteen blocks defines a bit location in which the presence and absence of a domain represents a binary value. Starting with a sheet of magnetic material having the preferred direction for magnetization normal to the sheet and assuming the sheet to be saturated in a direction away from the reader, the negative direction, then a small domain magnetized towards the reader may be represented by an encircled plus sign. Such a domain may occupy the position of any block in FIG. 2. If a domain is stored in one of the blocks V2P2 also coupled by a conductor H5P2 or H2P2 (and a domain is absent in the other), it represents a binary one and a binary zero respectively. The binary one and zero positions for a domain are shown by the encircled plus signs in FIG. 2. The associated absence of a domain is, hereinafter, represented by a circle with no plus sign. Each set of eighteen blocks as shown in the table and in FIG. 2, then, corresponds to a bit location. Only one domain at a time is present normally in a bit location.

Binary one and zero representations are moved selectively by pulses on the propagation conductors. A (propagation) pulse on a propagation conductor generates a (positive) field directed toward the reader at each conducting loop therealong. Actually, the positive field is generated only within the conducting loops along the pulsed conductor. Outside the loops are negative fields directed away from the reader. A single wall domain thus actually sees a field gradient which causes movement of that domain and a positive pulse on a propagation conductor is taken to cause such a gradient. A pulse on conductor V2P3 then moves upward, one block to the correspondingly designated blocks, either the one or the zero representation shown in FIG. 2 (only one representation at a time being present in a bit location). Similarly, a pulse on conductor V3P2 moves either representation one block to the right. A pulse on conductor H2P3, however, moves to the right only a domain in the block H2P2 of the table while a pulse on conductor H5P3 moves to the right only a domain in the block H5P2. The propagation circuitry may be seen to be organized to generate a propagation field in any selected block in the described set of eighteen blocks.

Each uniquely accessed set of eighteen blocks comprising a bit location has adjacent to it, in either the horizontal or vertical direction, similar uniquely accessed sets of eighteen blocks comprising other bit locations. Each of those blocks may be designated as discussed above, remembering that the V conductors are designated one to nine and the H conductors

of blocks will reflect such conductor designations. The sheet, accordingly, may be thought of as organized into sets of eighteen consistently designated blocks, each set comprising a bit location.

A basic operational unit may be defined in terms of related bit locations on the basis of normal usage. In the illustrative organization, specifically, not all bit locations are normally each of columns I, II, and III as shown in used for storage. It is convenient, at this juncture, to think of the magnetic sheet of FIG. 1 organized into rows and columns of bit locations. The columns are designated I, II, III, I, III, etc. in FIG. 2 for adjacent bit locations in a row of bit locations. Only the bit locations in a column I are utilized as permanent information storage areas. The remaining columns of bit locations are reserved for operations on the binary representations stored in a column I. A basic operational unit for the illustrative organization, accordingly, may be defined as a row of three sets of eighteen blocks, one in each of columns I, II and III as shown in FIG. 2. The representative H and V conductors shown in FIG. 2 now may be seen to be designated to correspond to the basic operational unit.

All like designated blocks in bit locations along a particular row or column of bit locations have like fields generated therein when the propagation conductor coupled to the magnetic sheet at those blocks is pulsed. It is noted in FIG. 2 that the designations for the columns of bit locations repeat, indicating that the basic operational unit repeats along any given row of bit locations. The vertical (V) conductors associated with a basic operational unit are designated 1 to 9 in FIG. 2. Along any given row of bit locations, therefore, many vertical conductors have like designations. In the illustrative operation, all like designated vertical conductors are assumed pulsed in parallel. Similarly, the horizontal (H) conductors associated with a basic operational unit are designated 1 to 6. Accordingly, along any given column of bit locations, many horizontal conductors have like designations. In the illustrative operation, however, we assume that like designated horizontal conductors are pulsed individually.

The blocks of a bit location may be thought of as arranged in cells. A set of eighteen blocks corresponding to a bit location is represented in two distinct sets one below and one above a double line in column I of FIG. 2. The set of nine blocks above the double line in each bit location is referred to as a cell designated C1; the set below the double line is similarly designated C2. Cells C1 and C2, then, together comprise the bit location labelled BL111 in FIG. 2. If a domain, as shown in FIG. 2, is present in cell C1 but not in cell C2, a binary "1" is said to be stored in bit location BL111. On the other hand, if a domain

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is present in cell C2 but not in cell C1, a binary "0" is said to be stored.

The cells of a bit location may be arranged in either of two orientations. FIG. 2 shows a cell C1 and a cell C2 arranged vertically with respect to one another. Such an arrangement is designated type A. Another arrangement is where cell C1 and cell C2 are arranged horizontally with respect to one another as shown in FIG. 3. The latter is designed type B. FIG. 3 shows the type B arrangement in abstract form including only cells C1 and C2 separated by a double line without the block or propagation conductor representations. Both a one and a zero representation are shown as would be the arrangement if neighbouring bit locations included the specified information. A blockwise rotation of 90 degrees of either representation in FIG. 3 permits a simple visualization of the correspondence between the type A and type B form and the origin of the abstraction used in FIG. 3. The information format will be changed from type A to type B during the illustrative operation described hereinafter and it is convenient to refer to the two cell symbol as a "domino" during that description.

Various logic operations are now described in terms of the foregoing organization. It is noted that there are four basic physical steps underlying those operations, i.e. when a domain is (1) moved, (2) annihilated, (3) split into two, and when two domains repel each other in any attempted collision therebetween. These steps will be explained during the discussion of the logic operations when these steps will be referred to again.

#### *Logic Operations*

##### *Replicate*

The first logic operation to be described is called a replicate operation and results in a duplication of information in memory. FIG. 4 shows first and second adjacent sets of eighteen blocks for which the block designation discussed in connection with the chart above applies. The sets of blocks conveniently are arranged in columns I and III, respectively, as shown in FIG. 2. Each set of blocks includes a cell C1 and a cell C2. A binary zero representation is shown as a circle and an associated encircled plus sign stored in the cells C1 and C2 of column I respectively. The binary representation shown is moved one column of blocks to the right conveniently by a pulse on conductor V3P2 which generates (+) propagation fields in the blocks indicated in FIG. 4. The information representation, in response, moves to blocks H2P3 and H5P3 as shown in FIG. 5. In accordance with assumed pulsing arrangement, fields are generated in other blocks. Such fields are ignored in the description of the various logic operations. Next, pulses are applied concurrently to conductors V2P2 and V4P2 generating the propagation fields (+) shown in FIG. 5. The binary representation

splits, moving in response to positions shown in FIG. 6. Those pulses are followed by a pulse on conductor V5P2 generating propagation fields indicated by the plus signs in FIG. 6. FIG. 7 shows the resulting disposition of binary representations. The binary representation originally only in a bit location in column I now appears, as well, in an associated bit location of column III and the replicate operation is complete.

It will be appreciated that the replicate operation is carried out in response to propagation fields generated simultaneously in blocks to each side of a binary representation. The operation is basically that of moving information. But when a field of a polarity to move information is generated to each side of a binary representation, a constraint is imposed on the movement of the representation in response. It is remembered that a binary representation comprises a domain present in a first position and absent in a second position. In order to simplify the explanation, a convention is used in which a binary representation is taken to comprise two indications, one of which is a domain and the other of which is an absent domain. The constraint, then, necessitates that each indication split. This is no problem for an absent domain of course. A domain, however, is thought to change its shape during the splitting process to first an oval then a dumb-bell configuration before being split by the negative field generated about each positive propagation field. In some circumstances an additional negative field may be generated in the position of the constricted portion of the dumb-bell in order to foster splitting. But for the most part such additional negative fields are unnecessary. An understanding of the nature of the splitting of a domain, however, is not important for understanding this description. It is sufficient that the splitting of a domain in response to the generation of propagation fields to both sides thereof occurs. Typically, the fields for accomplishing such a split are greater than an ordinary propagation field, which is of the order of a few oersteds for most suitable magnetic materials, as is discussed further hereinafter.

##### *Invert*

The next logic operation is called an invert operation and results in the reversal of a binary representation. For example, if a binary one is represented by a domain in a block H5P2 and the absence of a domain in a block H2P2 of an illustrative bit location as shown in FIG. 8, the invert operation results in a domain in block H2P2 and the absence of a domain in block H5P2.

The operation is carried out by generating a sequence of pulses which propagate domains (and the absence thereof) from one position to the next. This may be carried out in many ways. Illustratively, the pulse sequence H2P3, V3P3, V3P1, V3P2, and H5P2 moves a do-

main (or absence thereof) from block V2P2 (or H2P2) to block H5P2. The pulse program H5P1, V1P1, V1P3, V1P2, and H2P2 concurrently moves a domain (or absence thereof) from block H5P2 to block H2P2.

FIGS. 8 to 13 show the consecutive results of the steps of the invert operation. Each figure includes plus signs representing the fields for effecting the next consecutive movement. A comparison between FIGS. 8 and 13 shows that inversion is realized.

#### *The AND Operation*

It is recalled that each binary representation is in a form taken to comprise first and second indications in a cell C1 and a cell C2 respectively. Corresponding cells C1 in two adjacent binary representations include the presence or absence of a domain and those indications are in blocks H5P2 as shown in FIG. 2, spaced apart by two intervening blocks. Similarly, each of cells C2 of adjacent bit locations includes an indication in a block H2P2 and those blocks are also spaced apart by two blocks. For convenience, when both indications of a binary representation are referred to they are described as occupying or being moved to "positions." When only a single indication is referred to, the block indication is used.

The AND operation between first and second binary representations comprises initially moving those representations to first and second positions spaced apart by an intermediate position. The indications in adjacent like designated cells, accordingly, are stepped together by one block. The operation comprises a program of pulses in first and second positions and in intermediate positions. The first and second positions are defined specifically as positions occupied by first and second binary representations of, for example, type A form as shown in FIG. 2 spaced apart one column of blocks. The "intermediate position" refers collectively to the two blocks, of the intermediate column of blocks, separating the indications in the first and second binary representations.

The operation between the indications in adjacent cells C1 is different from the operation on the indications in adjacent cells C2. With respect to adjacent cells C1, a propagation field is generated to move domains (or the absence of domains) into the intermediate block. If two domains are present, only one moves into the intermediate block to the exclusion of the other because of a mutual repulsion exhibited between two adjacent domains (like charges). Next, a field is generated, in the intermediate block, of a polarity to annihilate any domain there. Subsequently, another propagation field is generated in the intermediate block to move there any domain remaining in the adjacent blocks of the first or second positions. It is clear that a domain now occupies the intermediate block only if a domain were present in each of the adjacent cells C1 and

to this extent constitutes an AND operation between adjacent cells.

The AND operation between adjacent binary representations, however, is not yet complete. The domains (and absence of domains) in adjacent cells C2 of those representations must be operated upon. A propagation field is generated in the corresponding block of the intermediate position, to this end, and again only one domain (if present) moves in response. In this instance, however, fields of a polarity (negative) to annihilate domains are generated in the adjacent blocks of the first and second positions rather than in the intermediate block. If a domain were present in either the associated blocks of the first or second position initially, a domain occupies the intermediate block at the termination of the pulse sequence. To the extent that a domain does occupy the intermediate block if at least one of the associated blocks of the first and second positions were occupied by a domain initially, the operation may be thought of as an OR operation between two adjacent cells C2. The AND operation between two adjacent binary representations may be thought of, then, as an AND operation between cells C1 of those representations and an OR operation between cells C2 of those representations. In order to avoid ambiguities, an AND operation between adjacent cells is referred to as a "MINOR AND" operation and an OR operation between adjacent cells is referred to as a "MINOR OR" operation. The AND operation between adjacent representations is referred to as an AND operation. As is described hereinafter, an OR operation between adjacent representations is referred to as an OR operation.

The MINOR AND operation will now be considered in detail. It will be assumed that a domain is stored as shown in FIG. 14 in cells labelled C1 in columns I and II respectively. The MINOR AND operation, illustrated in FIGS. 14 to 18, can be described briefly as follows: Vertical conductors V4P<sub>i</sub> identify the selected column of blocks including an intermediate block in which the final indication is stored. The desired result is that a domain be left in this intermediate block only if domains were present initially in both cells C1 in columns I and II as shown in FIG. 14.

The MINOR AND pulse sequence involves several steps including, principally, the annihilation of one domain and placing of the remaining one in the intermediate column. As may be seen from the following description, it is immaterial which domain is annihilated. In FIG. 15, a pulse is applied to conductor V4P2 so as to produce an attractive field at block V4P2 as indicated. Only one of the two domains moves to the intermediate block, the other being excluded by the repulsion forces

present during an attempted collision between adjacent domains.

It is conceivable that specially symmetric positions would result in a situation of unstable equilibrium in which neither domain would enter fully the intermediate block but both would move in only part way. (This unstable equilibrium has not been found to be of practical importance and an actual situation has never been observed to occur. The possibility of such an equilibrium may be avoided altogether by deliberately altering the symmetry of the propagation wiring geometry slightly such as making the current driving loops somewhat noncircular.

The result, in which the domain from column I moves to the intermediate block, is illustrated in FIG. 16. That domain is annihilated by generating a field of negative polarity in the intermediate block via pulse on conductor V4P2. The field is indicated by the minus sign in FIG. 16. It is evident that had the domain initially in column III in FIG. 15 moved to the intermediate block it would have been annihilated.

A (positive) propagation pulse is next applied to conductor V4P2 as shown in FIG. 17 so that the remaining domain is drawn to block V4P2 as shown in FIG. 18.

From the foregoing it is evident that a domain will appear in the intermediate block if and only if domains were present originally in both of the two C1 cells of columns I and II. If only one domain is present it would be destroyed by the operation described in connection with FIGS. 16 and 17 so that no domain would be present in the final situation.

The MINOR OR operation functions so that a domain would be left in the intermediate

block if one were present in either of two spaced apart cells. This is illustrated in FIGS. 19—22 for a specific case in which a domain is present in the C2 cell of column I and absent in the cell C2 of column II. This domain disposition corresponds to representations in the bit locations of column I and column II of a zero for column I and a one for column II, as shown in FIG. 19.

The operation proceeds initially in the same fashion as the MINOR AND and in fact the same set of vertical conductors can be used up to the point corresponding to FIG. 16 for the MINOR AND. This is clear from a comparison between FIGS. 14 and 19 and FIGS. 15 and 20. A comparison between FIGS. 16 and 21 shows that a domain occupies the intermediate block in each case. It is evident in the MINOR OR operation that a domain exists in the intermediate block if one were present in either column I or column II initially.

The annihilate step is however different for the MINOR OR as stated above. As illustrated in FIG. 21, annihilation fields are developed not in the intermediate block as for the MINOR AND operation but instead in the associated blocks of adjacent cells C2 in columns I and II. The effect is to leave, after the fields represented by minus signs have been applied in FIG. 21, one and only one domain present in the intermediate block only if a domain were present in either of the two C2 cells or in both initially. FIG. 22 represents the shift of this domain to the centre block of cell C2 in column II which is its normal position for a representation in column II.

The following truth Table II is well understood in connection with logic operations:

TABLE II

| AND | 0 | 1 |
|-----|---|---|
| 0   | 0 | 0 |
| 1   | 0 | 1 |

It is clear from the table that the AND operation functions to provide a binary one representation only when two binary one representations are operated upon. It may be seen from FIGS. 2 and 3 that information processed as described, where a MINOR AND operation is carried out between adjacent cells

C1 and a MINOR OR operation is carried out between adjacent cells C2, provides results consistent with the table.

#### The OR Operation

The following truth Table III is also well understood in connection with logic operation:

TABLE III

| OR | 0 | 1 |
|----|---|---|
| 0  | 0 | 1 |
| 1  | 1 | 1 |

It is clear from the table that the OR circuit functions to provide a binary one representation except when two binary zero representations are present initially. Such an operation is realized between adjacent representations by carrying out a MINOR OR operation between adjacent cells C1 and a MINOR AND operation between adjacent cells C2. It may be appreciated that the operation is the reverse of the AND operation as is also indicated by a comparison between Tables III and IIII.

In carrying out the various logic operations herein, it is necessary to provide certain fields in the various blocks shown in FIG. 2. Each such field may be provided by a pulse on an H or a V conductor. The particular conductor selected for pulsing in a particular operation is determined by the effect on other bit locations of a pulse applied to that conductor. A proper choice of conductors permits certain economies, for example, when an AND operation is carried out because both the MINOR AND and the MINOR OR operations may be carried out simultaneously requiring like pulses except for the annihilate steps in the operations. Useful circuits, accordingly, are arranged such that like operations are carried out along one co-ordinate conductor to economize, and annihilate operations are carried out along the other co-ordinate conductors for affecting alike only like designated cells of different bit locations.

Having discussed the basic organization of an arrangement embodying this invention and a number of the possible logic operations capable of being performed thereby, an illustrative content addressing operation comprising some of the illustrated logic operations will now be described.

The illustrative content addressing operation will be seen to comprise familiar functions. First, a duplicate representation for each word in memory is provided. Second, that duplicate is operated upon, in accordance with an applied match character, designated the "input tag", for generating match and mismatch indications. Third, all match indications and associated stored words are made available. All operations are carried out merely by providing fields in selected blocks of various bit locations for moving domains from block to block or for annihilating domains in selected blocks.

These general functions may be translated

into terms of consecutive logic operations thus providing, in outline, the following illustrative operation.

1. The duplication of all words in memory, of course, is carried out by the replicate operation. Since all bits of all stored words are to be duplicated, V conductors are used for the operation. Only bit locations in column I are used for storage. The replicate operation thus merely provides a duplicate word in each instance in the associated column III.

2. In order to generate the match and mismatch information, the duplicate words are moved, illustratively, to a separate portion of the memory where operations thereon do not disturb stored information. To this end, V conductors are employed to propagate information along columns III to a separate "logic" portion. It is evident that H conductors may be used to operate on information in column III in the logic portion of the memory without disturbing associated information in columns I of the original storage portion.

An invert operation is next carried out on information in columns III in the logic portion by means of pulses on H conductors.

It should be made clear at the outset that the invert operation is responsive to an external signal. The signal in this case is the input tag which specifies what the first group of binary representations should be for a desired match. It is to be understood that these representations can be any group of binary representations anywhere along the word. This input signal selects the appropriate H conductors in the logic portion. In response to that signal, the content of each of selected binary bit locations in each word is shifted to an associated column IIII where for simplicity of programming it is inverted as already described. The programming for the inversion operation need not be adjusted in accordance with the input tag but is an invariant operation which can be accomplished no matter what input tag is selected in a manner to be described hereinafter. After the inversion operation is completed, each inverted binary bit is then transported back to the associated column II by means of pulses on H conductors.

Each column II in the logic portion at this juncture in the operation contains a binary word. However, only those words having a match tag which matches the input tag now include all binary one representations. The bit

representations in column II are rotated from type A to type B form in order to carry out MINOR AND operations between adjacent indications in columns II and between adjacent indications in columns III. Consecutive MINOR AND operations provide a domain, indicating a match, in a column III only if each cell in the corresponding column includes a domain. A match is indicated by a word of all binary one representations. When such words are rotated to the type B form column III includes no domains.

3. For each match between the match tag of a stored word and the input tag, a single domain is present in the associated column III of the logic portion in the cell C1 of, illustratively, the first bit location. Consecutive replication operations are then carried out via H conductors to generate domains in each cell of column III associated with the match tag. Naturally, each replicate operation is alternated (or concurrent) with suitable propagation fields for properly positioning the most recently replicated domain. When all cells are occupied in this manner, the sets of domains in columns III are propagated to associated columns III. It is important to note that each cell in the logic portion in columns III now includes a domain. Thus a continuous sequence of domains is provided in columns III of the logic portion associated with matched words in corresponding columns I of the storage portion.

The stored words in the storage portion are then replicated and moved to associated columns II of the logic portion to align with the match and mismatch indications. MINOR AND operations are then carried out between indications in cells in columns II and indications in corresponding cells in associated columns III. It is evident that all match words are preserved and all mismatch words are eliminated.

What is accomplished is that only those stored words which have matching tags are made available in the logic portion. This is accomplished in response to an external signal which specifies the input tag in a manner to effect inversion of appropriate bits of the match tag. The external signal, it is clear, controls the H conductors driven in this operation. This is the only time the operation is effected directly by external signals in the illustrative operation. No reading of the result of any operations is required and the remaining logic operations which result in the elimination of all mismatched words and the retention of all matched words occur on the basis of a preassigned program as is described hereinafter.

It is helpful at this juncture in the description to include a glossary of terms for easy reference in the succeeding description.

1. Block — an area in which a domain may be set up.

2. Bit location — a group of eighteen blocks

arranged in three adjacent columns of blocks as shown in Table I above.

3. Cell — nine blocks comprising one-half of a bit location.

4. Binary representation — a representation including both the presence and the absence of a domain at the cells of a bit location.

5. An indication — either the presence or absence of a domain tantamount to one-half of a binary representation.

6. Basic operational unit — three adjacent bit locations in a row.

7. Intermediate position — refers collectively to two blocks, in a column of blocks, separating corresponding indications in two binary representations spaced apart by that column of blocks.

8. Intermediate block — a block spacing apart first and second corresponding indications in first and second spaced apart binary representations.

#### *Illustrative Operation*

FIG. 23 shows a portion of sheet 111 of FIG. 1 in which each of first and second binary words is represented by consecutive "dominoes" (first bit locations of corresponding basic operational units) arranged from top to bottom in the type A configuration of FIG. 2. Only two words are indicated and only the match tags of those words are shown. Specifically, the first (top) three bits of each word are taken to be the match tag of each of those words. It will be assumed that single word domains are provided initially and then moved to the positions shown.

FIG. 2 shows a row of bit locations where each bit location is arranged in a column of bit locations. The columns are designated I, II, and III and then the designations repeat from left to right as has been discussed before. Adjacent binary words as shown in FIG. 23 are stored in consecutive bit locations, from top to bottom as viewed, along only columns I. Thus, next adjacent stored binary words occupy bit locations in columns of bit locations spaced two columns apart in accordance with our assumed basic operational unit.

FIG. 23 shows only the match characters of each word hereinafter referred to collectively as the match tag. It is important to understand, however, that the remainder of each word is present also. The match tags are 001 and 100 reading downward in each column I, first the left-hand column and then the right-hand column as viewed.

The various logic operations are illustrated in terms of the domino symbol of FIGS. 2 and 3 in the discussion of the illustrative content addressing operation.

The pulses for performing the various logic operations are provided via the Y and X drivers 12 and 13 of FIG. 1 under the control of control circuit 16. To this end, propagation conductors PY1...PY<sub>n</sub>, and PX1...PX<sub>m</sub> of FIG. 1 may be seen to correspond to the pro-

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pagation conductors of FIG. 2. The designations for those conductors described in connection with FIG. 1 permit ready comparison with the description in the aforementioned copending application No. 36777/67. The designations used in connection with FIG. 2 permit a simple description of the present illustrative organization.

#### *Replicate Operation*

The first logic operation in the illustrative content addressing operation is to replicate all stored words. The result of such an operation on the match tag of word one and word two is shown in FIG. 24. It is seen from the figure that the match tag is repeated in the column II to the right next adjacent the initial storage column I as viewed in FIG. 24.

The pulse program for replication is as follows: First a pulse is applied to conductor V3P2 causing the presence and absence of domains (i.e., the indications) in the initial binary representations in column I of FIG. 23 to move one block to the right as viewed in FIG. 2. Second, a pulse is applied to each conductor V2P2 and V4P2 in the storage portion of the memory resulting in the actual replication and the return of one set of indications to the initial position in corresponding columns I as shown in FIG. 24. Third, a pulse is applied to conductor V5P2 to move the newly generated indications to the proper positions in the centre column of blocks of column III in accordance with the illustrative scheme for binary representations, as shown in FIG. 24. These three consecutive field patterns complete the replicate operation.

#### *Move to Logic Portion*

FIG. 25 shows the duplicate of the representative match tags in the absence of the original binary representations. It is convenient, but not essential to move the duplicate representations to a different logic portion of sheet 11. The movement of information is carried out merely by pulsing conductors V5P1, V5P3, V5P2, V5P1... consecutively operating columns II of the sheet as (vertical) shift register channels. The integrity of the information is maintained as disclosed in the aforementioned copending application No. 36777/67. FIG. 25 then, may be considered to represent a logic portion of sheet III positioned with respect to the position of the initial information so that it can be reached by the shifting pulse program just described.

#### *Invert Operation*

The next operation is to invert all bits in match tags in positions corresponding to the relative positions of zeros in an assumed input tag. It will be assumed that 001 is the input tag in order to illustrate a match and a mismatch in the illustrative content addressing operation. The first and second bits of the match tag of each word in memory are inverted accordingly in response to an external signal which determines, via control circuit 16 of

FIG. 1, which H conductors are driven for this operation.

The first step in the invert operation is to move to the right, from column II to column III, the binary representation in each of the first two bit locations of the match tag of every stored word in the logic portion of the memory. FIG. 26 shows the results of such an operation for the representative stored words in response to the assumed input tag. The first word, to the left as viewed, includes two zeros in the first two bit locations. Consequently, the domains and associated absence of domains representing those zeros are moved one column to the right to column III there again representing zeros as shown in the figure. The second word, on the other hand, includes a one and a zero in the first and second bit locations respectively. Therefore, the domains represent those binary values when moved to column III.

The pulse program for shifting the binary representations of the first two bit locations from column II to column III, in the logic portion, changing the disposition of domains from that shown in FIG. 25 to that shown in FIG. 26 is as follows: First, conductor H2P3 is pulsed. Each domain in a block H2P2 in column III moves one block to the right in response. Next the H5P3 conductor is pulsed. In response, each domain in a block H5P2 in column III moves one block to the right. Sequentially (or concurrently), conductors H2P1, H5P1, and then H2P2, and H5P2 are pulsed completing the movement of such domains from column III positions to corresponding positions in column III as shown in FIG. 26. Now the information is in a column where it can be inverted without disturbing other stored information which is not to be inverted.

The actual invert operation then is performed only on information now in column III in the logic portion and consists of exchanging the positions of domains and absence of domains in the one and zero representations in each bit location one for the other. Thus if a domain is in a position to represent a one in a particular bit location, that domain is moved to the "zero" position and the absence of a domain in that zero position is simultaneously moved to the "one" position. This operation is indicated by the broken arrows in FIG. 26.

The result of the invert operation is shown in FIG. 27. The pulse program for achieving that result comprises consecutive pulses on conductors H2P3, H5P1, V9P3, V7P1, V9P1, V7P3, V9P2, V7P2, H2P2, and H5P2. A comparison of FIGS. 26 and 27 indicates the inversion of information in column III.

The information in column III is then moved back into corresponding columns II as shown in FIG. 28. (This operation is accomplished by a pulse program comprising pulses

on conductors H2P1, H5F1, H2P3, H5P3, H2P2, and H5P2. The inversion operation is now complete.

#### *Type A to Type B Conversion*

5 It is next desired to perform MINOR AND operations between the indications in corresponding cells in next adjacent binary representations in a column of bit locations. In order to do so, it is convenient to change the form of the information from type A as shown in FIG. 2 to type B as shown in FIG. 3. A simple "rotation" of the indication in one cell about the indication in the other of each binary representation accomplishes the change as is indicated for each representation by the broken arrows in FIG. 28. The resulting type B form is shown in FIG. 29, the domino symbol being completed with broken lines for ready reference. It is to be recognized that the broken lines in FIG. 29 are imaginary and intended only to associate the presence and absence of domains in pairs. The broken lines indicate an area somewhat smaller than that encompassed by type A symbols. In practice, those areas are equal, however, and the indicated difference in areas is to be ignored herein. The pulse program for accomplishing this result comprises consecutive pulses on conductors H2P3, H2P1, H2P2, V8P3, V8P1 and V8P2.

#### *Consecutive MINOR AND operations*

FIG. 29 shows the disposition of the illustrative stored match tags when a MINOR AND operation is initiated. A comparison between FIG. 29 and FIG. 2 shows that the indications in the representations in FIG. 29 are in blocks H5P2. First, the indications in the third (from the top as viewed) binary representations in each match tag are moved, upwards as viewed, to blocks H3P2 spaced one position apart from the corresponding indications in the second binary representations as shown in FIG. 30. The pulse program for carrying out this operation comprises consecutive pulses on conductors H6P2, H1P2, H2P2, and H3P2. Only the H conductors coupled to positions associated with the third binary representations are pulsed at this time.

The MINOR AND operation comprises first a pulse on conductor H4P2 corresponding to the intermediate position as shown in FIG. 30. The disposition of domains as a result of that pulse is shown in FIG. 31. It is assumed illustratively that the third binary representation (domain) in word one moves into the intermediate position to the exclusion of the second binary representation (domain). It is noted that for the second and third binary representations in word two, no domain is so excluded and the result of this operation is that a domain from each representation moves to the intermediate position as shown in FIG. 31. Thereafter, a pulse, of a polarity to annihilate domains in corresponding blocks H4P2, is applied to the appropriate conductor H4P2.

Next, a pulse is applied to conductor H4P2 moving any remaining domains into block H4P2.

It is evident that MINOR AND operations are carried out concurrently on corresponding indications of the second and third binary representations. The results of the operations are shown in FIG. 32. For word one, a domain remains; for word two, none remains. The first binary representation in each word is unchanged by the operation as also shown.

The concurrent MINOR AND operations are now repeated between the indications in the first binary representation of each stored match tag and the corresponding result of the previously described MINOR AND operations. Again, the operation requires the movement of the representation resulting from the previous AND operations upward to a position spaced apart one position from that of the first binary representation. The disposition of indications at various stages during this operation is shown in FIGS. 33 and 34. Only a single representation remains, as a result of the operation, as shown in FIG. 35. The pulse program to achieve the second illustrative concurrent MINOR AND operations is entirely analogous to that shown to carry out the first and accordingly is not described in detail.

Only if a stored match tag matches the input tag will a domain appear in the position in a column III illustrated in FIG. 35.

It is apparent that the MINOR AND operations require, for example, fields in second and third bit locations but not in the first bit locations and vice versa. For complete flexibility in this respect, an individual driver is provided illustratively for each H conductor. As will be discussed more fully hereinafter, more economical organizations are possible. Importantly, the MINOR AND operations between corresponding indications in next adjacent binary representations in each match tag are carried out until a single representation or no representation remains for each stored match tag as shown for words one and two in FIG. 35, respectively.

Illustratively, if a representation remains, a match is indicated. If a representation is absent, a mismatch is indicated.

If a representation is present, a domain is positioned in the corresponding block H5P2 in the associated column III. Accordingly, the information indicating all matches in memory is also made available in memory.

Before proceeding, it must be recognized that the choice of an illustration has been fortuitous. Had a stored word been chosen which was the inverse of the input tag including all zeros in its match tag, for example, a zero representation (a domain in a column III) would be left in the position associated with that word in FIG. 35. This is, of course, of no consequence in the present operation because the presence of domains in columns III

is not representative of matches and may be annihilated simply by applying to conductors V8P2 a pulse of polarity to annihilate the domains in corresponding blocks.

#### 5 *Eliminating Mismatched Words*

An indication has been obtained in a column II, corresponding to each match tag in memory which matches the applied input tag. A procedure for eliminating the mismatched words in memory is now given.

10 The domain shown in column III of FIG. 35 is replicated five times in a manner discussed in connection with FIG. 5 to fill all cells in the bit locations of the stored match tag. (In practice, as many domains are generated as there are cells in a stored word.) As the additional domains are generated they are moved downward as viewed in FIG. 35 to positions shown in FIG. 36 for the first two additional domains and in FIG. 37 for five additional domains as well as for the original domain. The pulse program for achieving this result is consistent with that described in connection with FIG. 5 appropriately applied along with the basic propagation pulse sequence for moving each additional domain downward as each domain is generated.

Next, the match information in column II as shown in FIG. 37 is propagated, in parallel, to column III as shown in FIG. 38. The pulse program for this is completely in keeping with the operation described in the aforementioned application No. 36777/67.

Each word in memory is next replicated as described in connection with FIG. 24 regenerating the binary representations shown in that figure for the match tags only. Thereafter, the words, as shown in columns III of FIG. 24, are moved again to a logic portion of the sheet as shown in FIG. 25 in a manner discussed in connection with that figure. The resulting disposition of domains is shown in columns II of FIG. 39 for the match tag of each word. The pulse programs for realizing these operations are entirely analogous to those described above and are not described further at this juncture.

Now, a replication of each match tag (and associated word) in memory exists in a column II of the logic portion as shown in FIG. 39. In adjacent columns III a continuous series of domains or alternatively no domains exist as an indication of whether or not each stored match tag matches the input tag.

Now a MINOR AND operation is carried out between the indications in the cells of each of the match tags in columns II and the corresponding match indications (domains) in next adjacent columns III. There is no necessity for a preliminary type A to type B transformation, as shown in FIGS. 28 and 29, in this instance because the information to be operated upon is in next adjacent columns of blocks rather than arranged vertically in one column of blocks as was the case earlier.

FIG. 40 shows the representations in column III moved one column of blocks to the right preliminary to the actual MINOR AND operation. FIG. 41 shows the result of the MINOR AND operation. The disposition of domains in FIG. 41 is identical to that representing the match tag of word 1 as shown in FIG. 23. No representation of word 2 remains as shown in FIG. 41. Accordingly, only matched words appear in the logic portion of sheet 11. Mismatched words are eliminated. Of course, as each binary representation in a match tag is generated, so is the entire corresponding stored word generated making available only the information associated with the stored match tags corresponds to the input tag.

The basic logic operations and the use of those operations to effect the familiar content addressing function have now been described. The use of information in the form provided by those operations is also familiar. For example, it may be desired to update information associated with a particular match tag. The updating information, then, may be introduced into the logic portion of the sheet as described in the aforementioned application No. 36777/67. That information is moved along columns of bit locations in the logic portion of sheet 11 of FIG. 1 to positions corresponding to that portion of the match words that is to be changed. The changes are effected in a manner consistent with that described above again using sequences of logic operation in accordance with well understood considerations. Alternatively, the match words may be considered stored in parallel in shift register channels for propagation to output positions by utilization circuit 18 of FIG. 1 which may be a printer. The latter read out alternative is implemented by means of conductors coupled to those output positions as indicated by the inputs to utilization circuit 18 as shown in FIG. 1.

#### *Hardware Versus Software*

The basic structure of an arrangement such as has been described requires the magnetic sheet and propagation conductors described in the aforementioned application No. 36777/67 along with input and output arrangements entirely consistent with the teachings of that application. What is taught further herein is that a complete set of logic operations may be achieved in that structure in response to corresponding pulse programs on the propagation conductors. Further, it is also taught herein that consecutive pulse programs permit the realization of various familiar functions as indicated by an illustrative content addressing operation. It should be apparent to one skilled in the art that the realization of a complete set of logic operations also permits the realization of all computer operations.

It might be thought that structural simplicity has been gained at the expense of drive

circuit complication. This is not the case. Sheet 111 is perfectly capable of storing micro-programs or subroutines in a portion thereof. Such a micro-program may take the form of consecutive binary words stored in parallel shift register channels operated entirely as described in the last-mentioned application. As will become clear, there is no necessity to read out, by external means, the information stored in these programs. Programming then would necessitate essentially only the ordering of such micro-programs responsive to input signals. Not only is ordering of micro-programs a relatively simple programming effort but a driver circuit responsive to such a program may be relatively simple also.

Returning to FIG. 2 for a moment, basically, six H conductors and nine V conductors are required for achieving all the described operations. Each of those conductors has three phases. Consequently, forty-five separate conductors couple the blocks of each basic unit in the arrangement. The like designated V conductors are used in common. Assuming that each H conductor requires a separate driver, FIG. 42 shows a simple scheme for programming the drivers for achieving the illustrative operation.

FIG. 42 shows a portion of sheet 111, or alternatively a separate sheet, comprising a part of control circuit 116 of FIG. 1 in which a plurality of shift register channels are defined. Such shift register channel includes propagation means for advancing domains therealong from left to right as viewed. For this parallel propagation operation, additional propagation conductors may be utilized along with appropriate drivers (not shown). Such elements, however, are entirely analogous to those elements disclosed in the aforementioned application No. 36777/67. Domain patterns are stored in parallel in the several channels in a manner consistent with the teaching in that application.

Conductors AH1P1...AV9P3 are coupled to output positions in corresponding channels each responsive to the passage of a domain for activating the correspondingly designated propagation conductor via associated amplifiers A indicated.

The corresponding domains in each channel are advanced to the output positions simultaneously and so constitute a binary word in a stored micro-program. The micro-program for the replicate operation is illustrated. The operation comprises first a pulse on conductor V3P2 followed by pulses on conductors V2P2 and V4P2 and finally a pulse on conductor V5P2. The replicate program, then, comprises simply three consecutive binary words each including a domain or domains corresponding to the propagation conductors to be pulsed. These domains are represented again by encircled plus signs in FIG. 42.

Means (not shown) are provided to rewrite domains into the corresponding channels after they are read out. Such means are entirely consistent with the teaching of application No. 36777/67 and include, conveniently, an electrical or optical pickup at the output end of each channel for reproviding a domain at the input end of each channel each time a domain arrives at an output position.

An additional propagation channel is provided, as shown in FIG. 42, for advancing an additional domain in each binary word for controlling the polarity of the pulse applied to selected propagation conductors as is required for performing a MINOR AND operation for example. The additional channel is coupled by a control conductor CHV1. Conductor CHV1 is connected via an amplifier A<sup>1</sup> to each of amplifiers A. To this end, a switch is provided in each amplifier A responsive to an indication of the presence of the additional domain for determining the state of the switch and thus the pulse polarity provided in selected propagation conductors. The operation may be thought of as a pulse inversion operation where a domain in a pulse inversion channel, PIC, effects an inversion of the normal polarity of the pulse simultaneously applied to selected propagation conductors.

Various of the illustrative logic operations require augmented drive currents. For example, the replicate operation requires a pulse having an amplitude greater than the pulse required for simply moving a domain. An additional pulse augmenting channel, PAC, is conveniently provided as shown in FIG. 42. An output conductor CHV2 coupled to such a channel responds to the passage of a domain to activate an amplifier A<sup>11</sup>. Amplifier A<sup>11</sup>, in turn, is connected to each of the amplifiers A of FIG. 42 to, for example, increase the gain of any amplifier A concurrently activated. Amplifier circuits operable in this fashion are considered straightforward.

The micro-program for the invert operation (not shown) conveniently includes domains for pulsing H conductors corresponding to all bits in a match character. The external signal indicating the bits to be inverted inhibits all but the desired H conductors.

If next consecutive micro-programs are programmed in the same manner to pulse the propagation conductors as required to perform the illustrative operation, all that is required to perform the illustrative multiple match operation is to initiate the advance of domains to the right as viewed in FIG. 42 in response to a first signal, conveniently the activation of an input to control circuit 16 of FIG. 1.

The program may be terminated conveniently by providing a domain in an additional channel (not shown) to inhibit further propagation, via control circuit 16 of FIG. 1, when the presence of that domain is detected at the

corresponding output position. Alternatively, an "end-of-program" micro-program may be included in existing channels.

Of course, the programs may be rewritten and/or rearranged to perform different functions. It is clear then that the sequence of various logic operations determines the function performed and that various sequences may be stored separately in the manner shown in FIG. 42 for selection in response to an associated signal input to control circuit 16.

FIG. 43 shows the system organization of sheet 11 of FIG. 1 into storage and logic portions as described and including a control portion as shown in FIG. 42 in detail. The column indications of FIG. 2 are repeated as well as the control portion outputs, as shown in FIG. 42, for consistency. The logic portion is shown including outputs to circuit 18 of FIG. 1.

As described, the basic unit into which the memory of FIG. 1 is organized requires forty-five drive conductors and these are, ideally, shared with each other basic unit. Some operations may, and indeed complete flexibility does, require that various basic units be pulsed while others are not as is clear from the illustrative operation. Accordingly, the illustrative implementation calls for the H conductors to have separate drivers. It is, of course, economical to minimize the number of drivers. This may be accomplished by keeping the number of H conductors low, ideally to a small number related to the number of bits in a word. Alternatively, the logic operations may be programmed in a manner to permit common driving of like designated H conductors. Such considerations may lead to the reorganization of the memory into basic operational units of different numbers of blocks. In any case, the most economical organization is determined in accordance with well known considerations and not discussed fully herein. It is important to note, however, that it is not necessary to change the propagation circuitry geometry in order to change the basic operational unit. All that is necessary is that the existing conductors be programmed differently.

The invention, also, has been exemplified in terms of an information representation wherein a domain is present in a prescribed position in a bit location and a domain is absent simultaneously in another prescribed position in the same bit location. The representation appears to be redundant; a binary one and a binary zero may be represented by the presence and absence of a domain in only one position in a bit location. It would seem that packing densities would be increased if the latter representation were used. This would be so of course. But the various logic operations would be implemented less easily with the simple uniform coupling configuration for propagation conductors as shown in FIG. 2. Indications are that even further redundancy permits addi-

tional simplicity in performing logic functions. Various tradeoffs between packing densities and simplicity in logic operations, accordingly, are contemplated. The structure shown in FIGS. 1 and 2 permits a great deal of latitude in this respect. Again, it is necessary only to change the propagation pulse program to change the entire operation and/or basic operational unit.

Further simplicity in operation may be realized without changing the basic operational unit already described. For example, the match indications could be generated more simply if the zero representations were annihilated before rotation from type A to type B form was carried out. In fact, in this instance, A to B rotation is unnecessary. The described operation permits the illustration of a greater number of logic operations, however. Again, no structural changes are necessary to implement the simpler operation. Only a change in the program discussed in connection with FIG. 42 is necessary.

An embodiment of the invention has been described in terms of propagation conductors having a loop configuration. Such a configuration is merely illustrative. The above-mentioned copending application No. 36777/67 describes an alternative configuration which permits increased packing densities.

As has been mentioned above, it is possible to relate the various logic operations to four basic physical steps. These steps have been indicated throughout the discussion of the logic operations. It is well to emphasize them here, however, because the considerations underlying various extensions of, as well as constraints to, the logic operations in accordance with this invention are also emphasized in this manner. The physical steps common to the illustrative logic operations are: (1) the movement of a domain, (2) annihilation of a domain, (3) splitting of a domain, and (4) collision between domains.

The movement of a domain has been described in, for example, the aforementioned application No. 36777/67. Typically, movement is effected by providing a field of an oersted or two offset from the position of the single wall domain and of a polarity corresponding to the domain. The domain, then, "sees" a potential well and moves to its new least energy position. The propagation field need only exceed a propagation threshold characteristic of the material in which the domain is moved.

The annihilation of a domain requires a field again of only an oersted or two, typically no more than ten oersteds, generated at the position of a domain. The field, however, is of a polarity appropriate to cause collapse of the domain. For annihilation it is necessary only to exceed a stability threshold characteristic of the material.

Splitting of a domain into at least two other

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domains requires larger fields than are necessary to move or annihilate domains. This is because the operation entails the pinching of a domain into two. The pinching step requires that two walls be driven together, necessitating a field approaching  $4\pi M_s$ , where  $M_s$  is the saturation magnetization of the material, typically 100 oersteds.

Collision between domains as used merely prevents movement in response to a propagation field and thus necessitates no higher level field.

In one practical arrangement, drive conductors were arranged conveniently in orthogonal slots formed in a high permeability base plate rather than by a separate printed circuit. A sheet of erbium orthoferrite ( $\text{ErFeO}_3$ ) was positioned over the posts formed by the slots. The various physical steps were performed as described above in response to drive currents as follows:

|            |                   |
|------------|-------------------|
| Propagate  | +150 milliamperes |
| Annihilate | + 75 milliamperes |
| Split      | +500 milliamperes |
| Collision  | +150 milliamperes |

The domains had diameters of about 14 mils, slightly larger than the post size which was 10 mils on a side with five mil slots.

A recitation of packing density capability as well as other operating parameters provides a more meaningful appreciation of the memory arrangement of FIG. 1. Specifically, domains of the order of a half mil are moved via one-tenth mil printed circuitry of the type described in the last-mentioned application permitting a packing density of more than  $10^8$  domains per square inch. Drive currents of about 50 milliamperes are employed. The arrangement is capable of providing all matches in memory in about one millisecond.

The logic operations described form a complete set with which all computer operations may be realized. Some of those operations, such as the replicate operation where splitting of a domain is required, necessitate that the area of the domain be enlarged. In other operations such as the MINOR AND operation the domain area is not enlarged. A complete set of logic operation in which some operations are carried out without enlarging domain area and in which other operations require such enlargement are called mixed sets.

A complete set of logic operations may be formed however, without ever enlarging the area of a domain. In such cases, a reservoir of domains is provided, for example, in each bit location with an attending reduction in the packing density of any given memory. Of the basic physical steps, only movement and collision need be used. The physical splitting and the annihilate steps need not be employed in this instance. Rather, domains are conserved and operations such as the replicate and an-

nihilate operations are carried out on a logic basis where domains are borrowed from and returned to a reservoir.

A typical operation in this mode may employ the collision interaction between two domains. For example visualize two rows of three blocks forming three columns. Each block in the first column is occupied by a domain. The block in the first row, third column is also occupied by a domain. The object is to try and move the two domains in the first column to corresponding blocks in the second by generating propagation fields in those corresponding blocks. If the domain in the third column is made stationary, only the domain in the first column, second row moves to its corresponding block. The repulsion force between domains in the first row prevents such movement there. The operation in the first row enables us to form an AND operation. The operation in the second row enables us to form an OR operation.

The wiring geometry, field intensities, coercivity, etc., determine whether the collision interaction is effective over a single domain position (block) or two (or more) positions.

Operation with domains that retain their shape is possible over an operating range which is characteristic of the magnetic material employed. The multishaped domains existing in, for example, orthoferrite sheets, heated to the Curie point and then cooled to room temperature, are a familiar sight. When a bias field is applied in a (negative) direction normal to such a sheet, the domain shapes change. At a particular bias field each domain becomes circular (actually cylindrical) having a radius which is a function of the material and the geometry of the sheet. Further increases in bias eventually exceed a stability threshold causing the circular domains to collapse. A pure set of logic operations where domains retain their shape and are neither replicated nor annihilated employ background bias fields in a range to maintain the domains circular. A bias field for this purpose is provided conveniently by means of a permanent magnet not shown.

A complete set of logic functions may also be performed in a magnetic sheet wherein the domains may not be circular. The magnetic sheets in which operations of this type are carried out, however, are coercive force dominated. That is to say, the material is characterized by a preselected coercivity to domain wall motion. A domain in coercive force dominated sheets, then, takes any form required by the applied fields and remains in that form when the fields are removed. The geometry of the various conductors is controlling in this connection. Some background bias may be present also. Domains are not conserved in such a mode.

The mixed set of logic operations described requires both a preselected coercivity of, for example, 1.0 oersted, and a background bias

of 8 oersteds. The coercivity and bias for providing optimum margins is easily obtainable by experimentation for each magnetic sheet.

5 The illustrated embodiment of the invention has been described in terms of single wall domains having a preferred direction of flux substantially normal to the plane of the sheet in which those domains are moved. Single wall domains are also formed in anisotropic magnetic sheets in which a preferred direction of flux is in the plane of the sheet. Neighbouring domains in such a sheet exhibit repulsion forces only when they are situated along the hard axis of such materials with respect to one another. Neighbouring domains situated along the easy axis exhibit attractive forces.

10 Logic may be performed with single wall domains in such anisotropic sheets also. All that is required is that the domain wall encompassing the single wall domain close on itself to form a boundary for the domain independent of the boundary of the magnetic sheet in which the domain is moved.

#### WHAT WE CLAIM IS:—

25 1. Information storage apparatus comprising a sheet of magnetic material having an information representative pattern of presences and absences of single wall domains (as defined herein) at some of a plurality of possible positions, or blocks, for such domains, and means for controlling generation in the sheet of successive patterns of magnetic fields to effect a logic operation between the blocks of at least part of said information representative pattern.

30 2. Information storage apparatus comprising a sheet of magnetic material capable of having single wall domains (as defined herein) established therein at any of a plurality of possible positions or blocks, thereof, means energizable to introduce domain for forming an information representative pattern of presences and absences of single wall domains at some of said blocks, and means for controlling generation in the sheet of successive patterns of magnetic fields effective to manipulate at least part of a said information representative pattern established in the sheet so as to accomplish a logic operation between the blocks of that part.

3. Apparatus according to claim 1 or 2, wherein a said magnetic field is either a first magnetic field effective to move an established domain to an adjacent block or a second magnetic field effective to annihilate an established domain.

4. Information storage apparatus comprising a sheet of magnetic material having an information representative pattern of presences and absences of single wall domains (as defined herein) at some of a plurality of possible positions, or blocks, for such domains, and means for controlling generation in the sheet of successive patterns of first and second magnetic fields for selectively moving and annihilating, respectively, said domains in a manner to perform a logic operation between the

blocks of at least part of said information representative pattern.

5. Apparatus according to any preceding claim, wherein the means for controlling is operative to generate a sequence of said patterns of fields wherein the contents of at least two of the blocks of said part are caused to be separated by a vacant block; a domain, if present adjacent said vacant block, is moved into said vacant block; any domain moved into said vacant block is removed therefrom; and another domain, if present adjacent said vacant block, is then moved into said vacant block so that the contents thereof represents the result of an AND operation on the contents of said at least two blocks.

6. Apparatus according to any preceding claim, wherein the means for controlling is operative to generate a sequence of said patterns of fields wherein the contents of at least two of the blocks of said part are caused to be separated by a vacant block; a domain, if present adjacent said vacant block is moved into said vacant block; and another domain, if present adjacent the originally vacant block is removed so that the contents of the originally vacant block represents the result of an OR operation on the contents of said at least two blocks.

7. Apparatus according to claim 5 or 6, with claim 3 or 4, wherein said removal is effected by annihilation.

8. Apparatus according to claim 5 or 6, wherein said removal is effected by moving any such domain to a block in a portion of the sheet reserved as a reservoir of domains.

9. Apparatus according to any preceding claim, wherein the means for controlling is operative to generate a sequence of said patterns of fields wherein the contents of a block of said part is caused to have two vacant blocks each adjacent thereto; and a domain, if present, is caused to move simultaneously into those two adjacent blocks so that their contents represent a replicate operation on the contents of said block of said part.

10. Apparatus according to claim 8, wherein the means for controlling is operative to generate a sequence of said patterns of fields wherein, for each domain of said part, a domain from said portion is moved to a corresponding block in said part so that the contents of the corresponding blocks represent a replicate operation with respect to said part.

11. Apparatus according to any preceding claim wherein storage of a binary bit requires the presence and absence of a said domain at different prescribed locations.

12. Apparatus according to claim 11, wherein said prescribed locations are, for each binary bit, in different associated cells together constituting a bit location and each comprising a plurality of the blocks, the binary bit value being determined by which cell of a bit location contains a said domain.

of 8 oersteds. The coercivity and bias for providing optimum margins is easily obtainable by experimentation for each magnetic sheet.

- 5 The illustrated embodiment of the invention has been described in terms of single wall domains having a preferred direction of flux substantially normal to the plane of the sheet in which those domains are moved. Single wall domains are also formed in anisotropic magnetic sheets in which a preferred direction of flux is in the plane of the sheet. Neighbouring domains in such a sheet exhibit repulsion forces only when they are situated along the hard axis of such materials with respect to one another. Neighbouring domains situated along the easy axis exhibit attractive forces.

- 10 Logic may be performed with single wall domains in such anisotropic sheets also. All that is required is that the domain wall encompassing the single wall domain close on itself to form a boundary for the domain independent of the boundary of the magnetic sheet in which the domain is moved.

#### WHAT WE CLAIM IS:—

- 25 1. Information storage apparatus comprising a sheet of magnetic material having an information representative pattern of presences and absences of single wall domains (as defined herein) at some of a plurality of possible positions, or blocks, for such domains, and means for controlling generation in the sheet of successive patterns of magnetic fields to effect a logic operation between the blocks of at least part of said information representative pattern.

- 30 2. Information storage apparatus comprising a sheet of magnetic material capable of having single wall domains (as defined herein) established therein at any of a plurality of possible positions or blocks, thereof, means energizable to introduce domain for forming an information representative pattern of presences and absences of single wall domains at some of said blocks, and means for controlling generation in the sheet of successive patterns of magnetic fields effective to manipulate at least part of a said information representative pattern established in the sheet so as to accomplish a logic operation between the blocks of that part.

- 45 3. Apparatus according to claim 1 or 2, wherein a said magnetic field is either a first magnetic field effective to move an established domain to an adjacent block or a second magnetic field effective to annihilate an established domain.

- 50 4. Information storage apparatus comprising a sheet of magnetic material having an information representative pattern of presences and absences of single wall domains (as defined herein) at some of a plurality of possible positions, or blocks, for such domains, and means for controlling generation in the sheet of successive patterns of first and second magnetic fields for selectively moving and annihilating, respectively, said domains in a manner to perform a logic operation between the

blocks of at least part of said information representative pattern.

5. Apparatus according to any preceding claim, wherein the means for controlling is operative to generate a sequence of said patterns of fields wherein the contents of at least two of the blocks of said part are caused to be separated by a vacant block; a domain, if present adjacent said vacant block, is moved into said vacant block; any domain moved into said vacant block is removed therefrom; and another domain, if present adjacent said vacant block, is then moved into said vacant block so that the contents thereof represents the result of an AND operation on the contents of said at least two blocks.

6. Apparatus according to any preceding claim, wherein the means for controlling is operative to generate a sequence of said patterns of fields wherein the contents of at least two of the blocks of said part are caused to be separated by a vacant block; a domain, if present adjacent said vacant block is moved into said vacant block; and another domain, if present adjacent the originally vacant block is removed so that the contents of the originally vacant block represents the result of an OR operation on the contents of said at least two blocks.

7. Apparatus according to claim 5 or 6, with claim 3 or 4, wherein said removal is effected by annihilation.

8. Apparatus according to claim 5 or 6, wherein said removal is effected by moving any such domain to a block in a portion of the sheet reserved as a reservoir of domains.

9. Apparatus according to any preceding claim, wherein the means for controlling is operative to generate a sequence of said patterns of fields wherein the contents of a block of said part is caused to have two vacant blocks each adjacent thereto; and a domain, if present, is caused to move simultaneously into those two adjacent blocks so that their contents represent a replicate operation on the contents of said block of said part.

10. Apparatus according to claim 8, wherein the means for controlling is operative to generate a sequence of said patterns of fields wherein, for each domain of said part, a domain from said portion is moved to a corresponding block in said part so that the contents of the corresponding blocks represent a replicate operation with respect to said part.

11. Apparatus according to any preceding claim wherein storage of a binary bit requires the presence and absence of a said domain at different prescribed locations.

12. Apparatus according to claim 11, wherein said prescribed locations are, for each binary bit, in different associated cells together constituting a bit location and each comprising a plurality of the blocks, the binary bit value being determined by which cell of a bit location contains a said domain.



13. Apparatus according to claim 11 or 12, wherein the means for controlling is operative to generate a sequence of fields wherein the contents of each prescribed location are simultaneously moved to vacant blocks, and then each moved so as to occupy the other prescribed location corresponding to that binary bit so as to accomplish an inversion operation. 70
14. Apparatus according to claim 13 with claim 12, wherein during an inversion operation, the contents moved remain within one or the other of the cells of a bit location. 75
15. Apparatus according to any one of claims 11 to 14 wherein, in order to perform an AND operation with respect to two binary bits, the means for controlling is operative to generate a sequence of said patterns of fields wherein an AND operation according to claims 5, 7 or 8 takes place with respect to the contents of the prescribed locations of said two binary bits that will be domains for binary "1" storage, and an OR operation according to claim 6, 7 or 8 takes place with respect to the other pair of corresponding prescribed locations of said two binary bits. 80
16. Apparatus according to any one of claims 11 to 15, wherein, in order to perform an OR operation with respect to two binary bits, the means for controlling is operative to generate a sequence of said patterns of fields wherein an OR operation according to claim 6, 7 or 8 takes place with respect to the contents of the prescribed locations of said two binary bits that will be domains for binary "1" storage, and an AND operation according to claim 5, 7 or 8 takes place with respect to the other pair of corresponding prescribed locations of said two binary bits. 85
17. Apparatus according to claim 12 or any one of claims 13 to 15 with claim 12, wherein there is associated with each said bit location a further plurality of blocks, and the means for controlling is operative to perform at least some logic operation on the contents of a said bit location within the associated further plurality of blocks. 90
18. Apparatus according to claim 17, wherein each said further plurality of blocks is equivalent to two bit locations. 95
19. Apparatus according to claims 17 or 18, wherein the means for controlling is operative to generate a sequence of said patterns of fields wherein the contents of one cell of a said bit location is moved to a block within the associated further plurality of blocks so as to represent a rotation operation with respect to the representation of the binary bit of that bit location. 100
20. Apparatus according to any preceding claim, wherein the means for controlling is operative to generate a sequence of said patterns of fields wherein, prior to at least some logic operation, the contents of blocks of said part are moved to a separate area of the sheet reserved for logic operations. 105
21. Apparatus according to claim 20, wherein, prior to removal to the logic area, the means for controlling is operative to cause a replicate operation according to claim 9 or 10 with respect to the contents of blocks of said part, the removal to the logic area being effective with respect to the replications. 110
22. Apparatus according to claim 11, or any one of claims 12 to 21 with claim 11, arranged as an associative memory for binary words each comprising a plurality of binary bits of which  $n$  constitute a tag portion, wherein the means for controlling is operative in response to an input tag portion to cause an inversion operation according to claim 13 or 14 to take place in respect of representations of those binary bits of stored tag portions that correspond to one binary value of the input tag so that those modified tag portions that originally corresponded with the input tag then consist only of representations of the other binary value. 115
23. Apparatus according to claim 22, wherein the means for controlling is operative to cause  $(n-1)$  AND operations according to claim 5, 7 or 8 to take place successively between representations of the binary bits of the modified tag portions so that only for those modified tag signals that originally corresponded with the input tag will said other binary value result thereby eliminating all mismatched tag portions. 120
24. Apparatus according to any preceding claim wherein said domains are substantially circular. 125
25. Apparatus according to any preceding claim, wherein the sheet has a preferred direction of magnetization normal to the surface of the sheet. 130
26. Apparatus according to any preceding claim wherein the material of the sheet has a coercive force sufficient to prevent movement of single wall domains therein in the absence of a said field. 135
27. Apparatus according to any one of claims 1 to 25, comprising means for generating a bias field in the sheet for maintaining single wall domains in a specified pattern. 140
28. Apparatus according to any preceding claim, wherein there is included in the means for controlling a control portion of the sheet constituting a plurality of channels for single wall domains, and means responsive to successive patterns of domains in the channels for causing generation of said successive patterns of fields. 145
29. Apparatus according to claim 28, wherein each said channel controls energization of a different one of a plurality of conductors coupled to the sheet so as to define said blocks, and comprising means for propagating the contents of the channels in parallel. 150
30. Apparatus according to claim 29, wherein said conductors are coupled to each of the blocks in like manner. 155
31. Apparatus according to claim 29 to 30, 160



with claim 3 or claim 4, comprising means responsive to domains at output positions in the channels for providing pulses on corresponding said conductors sufficient to generate the first fields.

32. Apparatus according to claim 31, comprising a further propagation channel located in said control portion and operable with said channels, and means responsive to a domain at an output position in the further channel for inverting said pulses so as to generate the second fields.

33. Apparatus according to claim 31 or 32 with claim 9, comprising an additional propagation channel located in said control portion and operable with said channels, and means responsive to a domain at an output position in the additional channel for augmenting said pulses so as to generate fields sufficient to cause simultaneous movement of a domain to two other blocks.

34. Apparatus according to any preceding

claim arranged automatically to perform the steps of a logic operation according to any one of claims 5 to 110, 113 to 16, or 19 or any combination thereof.

35. Storage and processing apparatus arranged substantially as herein described with reference to, and as shown in, FIGS. 1 and 2 of the accompanying drawings, and adapted to operate substantially as herein described with reference to FIGS. 4 to 7, and/or FIGS. 8 to 113, and/or FIGS. 14 to 18, and/or FIGS. 19 to 22 of the accompanying drawings.

36. An associative memory arranged and adapted to operate substantially as herein described with reference to, and as shown in, the accompanying drawings.

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