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<table style="width: 100%; border: none;"> <tr> <td style="width: 50%; vertical-align: top; padding: 5px;"> (21) International Application Number: PCT/US99/24753 (22) International Filing Date: 22 October 1999 (22.10.99) (30) Priority Data: 09/186,042 3 November 1998 (03.11.98) US (71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). (72) Inventor; and (75) Inventor/Applicant (for US only): STEVENS, William, A. [US/US]; 111 Econome Court, Folsom, CA 95360 (US). (74) Agents: MILLIKEN, Darren, J. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US). </td> <td style="width: 50%; vertical-align: top; padding: 5px;"> (81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published <i>With international search report.</i> </td> </tr> </table>			(21) International Application Number: PCT/US99/24753 (22) International Filing Date: 22 October 1999 (22.10.99) (30) Priority Data: 09/186,042 3 November 1998 (03.11.98) US (71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). (72) Inventor; and (75) Inventor/Applicant (for US only): STEVENS, William, A. [US/US]; 111 Econome Court, Folsom, CA 95360 (US). (74) Agents: MILLIKEN, Darren, J. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).	(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published <i>With international search report.</i>
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(54) Title: LEVELIZING TRANSFER DELAYS FOR A CHANNEL OF MEMORY DEVICES IN A MEMORY SUBSYSTEM				
(57) Abstract A method and apparatus for levelizing transfer delays for a channel of devices. One method disclosed determines a controller delay value by iteratively testing memory transfers to determine a largest transfer latency value using a subset of all available delays for at least one of a plurality of memory devices (100). Additionally, a memory device delay value for each of the plurality of memory devices is determined by testing memory transfers using at least one delay value for each of the plurality of memory devices (120).				
PHASE 1 PHASE 2 <pre> graph TD 100["DETERMINE CONTROLLER DELAY VALUE BY ITERATIVELY TESTING ONLY A SUBSET OF DELAY VALUES AVAILABLE FOR LARGEST TRANSFER LATENCY"] --> 110["STORE CHANNEL DELAY VALUE IN A CONTROLLER DELAY THAT ALLOWS THE CONTROLLER TO SUCCESSFULLY PERFORM TRANSFERS WITH A SLOWEST DEVICE SUPPORTED"] 110 --> 120["DETERMINE A DEVICE DELAY FOR EACH DEVICE BY TESTING ONE OR MORE DELAY VALUES FOR EACH DEVICE"] 120 --> 130["STORE THE DEVICE DELAYS IN THE DEVICES TO INSERT DELAYS EQUALIZING A CYCLE COUNT FOR TRANSACTIONS BETWEEN THE CONTROLLER AND THE DEVICES"] </pre>				