CLAIMS

What is claimed is:

1. A semiconductor structure comprising:

a buried power rail under a bottom source drain of a vertical transistor;

a dielectric bi-layer under the bottom source drain, the dielectric bi-layer is between the buried power rail and the bottom source drain;

a silicon germanium bi-layer under the bottom source drain, the silicon germanium bi-layer is adjacent to the buried power rail; and

a buried power rail contact, the buried power rail contact connects the bottom source drain to the buried power rail.

2. The semiconductor structure of claim 1, wherein the dielectric bi-layer comprises:

a first dielectric layer, the first dielectric layer is in direct contact with the bottom source drain; and

a dielectric liner, the dielectric liner surrounds the buried power rail.

3. The semiconductor structure of claim 2, wherein the dielectric liner isolates the buried power rail from the silicon germanium bi-layer.

4. The semiconductor structure of claim 1, wherein the silicon germanium bi-layer comprises:

a first semiconductor layer; and

a second semiconductor layer disposed on the first semiconductor layer, the second semiconductor layer is in direct contact with the first semiconductor layer.

5. The semiconductor structure of claim 4, wherein the first semiconductor layer includes 30% germanium and the second semiconductor layer includes 60% germanium.

6. The semiconductor structure of claim 1, further comprising:

a third semiconductor layer, the third semiconductor layer is directly below the bottom source drain, the third semiconductor layer is made of silicon.

7. The semiconductor structure of claim 1, further comprising:

a top source drain;

a fin, the fin is between the top source drain and the bottom source drain; and

a metal gate, the metal gate is adjacent and in direct contact with the fin.

8. The semiconductor structure of claim 1, wherein the buried power rail is made of tungsten or ruthenium.

9. A semiconductor structure comprising:

a buried power rail under a bottom source drain of a vertical transistor;

a dielectric bi-layer under the bottom source drain, the dielectric bi-layer is between the buried power rail and the bottom source drain; and

a buried power rail contact, the buried power rail contact connects the bottom source drain to the buried power rail.

10. The semiconductor structure of claim 9, wherein the dielectric bi-layer comprises:

a first dielectric layer, the first dielectric layer is in direct contact with the bottom source drain; and

a dielectric liner, the dielectric liner surrounds the buried power rail.

11. The semiconductor structure of claim 9, further comprising:

a top source drain;

a fin, the fin is between the top source drain and the bottom source drain; and

a metal gate, the metal gate is adjacent and in direct contact with the fin.

12. The semiconductor structure of claim 9, further comprising:

a semiconductor layer, the semiconductor layer is directly below the bottom source drain, the semiconductor layer is made of silicon.

13. The semiconductor structure of claim 9, wherein the buried power rail is made of tungsten or ruthenium.

14. A method comprising:

epitaxially growing a silicon germanium bi-layer on a substrate, the silicon germanium bi-layer includes a first semiconductor layer and a second semiconductor layer;

epitaxially growing a third semiconductor layer on the silicon germanium bi-layer;

forming one or more vertical fins and one or more bottom source drains within the third semiconductor layer, the one or more bottom source drains are below the one or more vertical fins;

laterally etching portions of the silicon germanium bi-layer and the third semiconductor layer to form one or more first indentations;

forming a first dielectric layer within the one or more indentations, the first dielectric layer is directly below the one or more bottom source drain;

laterally etching portions of the first semiconductor layer to form one or more second indentations;

depositing a dielectric liner within the one or more second indentations; and

forming one or more buried power rails within the one or more second indentations, the one or more buried power rails are directly below the one or more bottom source drains.

15. The method of claim 14, wherein the dielectric liner separates the one or more buried power rails from the first dielectric layer.

16. The method of claim 14, further comprising:

forming a shallow trench isolation between the one or more vertical fins; and

forming one or more bottom source drain contacts, the one or more bottom source drain contacts connects the one or more bottom source drains with the one or more buried power rails.

17. The method of claim 16, wherein the shallow trench isolation extends through the third semiconductor layer, the silicon germanium bi-layer, and a portion of the substrate.

18. The method of claim 14, further comprising:

forming one or more top source drains on top of the one or more fins;

forming a metal gate between the one or more fins;

forming one or more top source drain contacts; and

forming one or more gate contacts.

19. The method of claim 14, wherein the first semiconductor layer includes 30% germanium and the second semiconductor layer includes 60% germanium.

20. The method of claim 14, wherein the third semiconductor layer is made of silicon.