ABSTRACT

A memory device includes a first memory group including plural first non-volatile memory cells capable of storing multi-bit data, and a second memory group including plural second non-volatile memory cells capable of storing single-bit data. A program operation controller builds the multi-bit data based on data inputted from an external device, performs a logical operation regarding partial data among the multi-bit data to generate a parity, programs the parity in the second memory group after programming the partial data in the first memory group, perform a verification operation regarding the partial data after a sudden power-off (SPO) occurs, recovers the partial data based on the parity and a result of the verification operation, and programs recovered partial data in the first memory group.

FIG. 1