SG 9705229-4
RTMP
COPY

**PCT** WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04L 7/00 — A1

(11) International Publication Number: WO 96/41443

(43) International Publication Date: 19 December 1996 (19.12.96)

(21) International Application Number: PCT/US96/09663

(22) International Filing Date: 7 June 1996 (07.06.96)

(30) Priority Data:
08/486,935 7 June 1995 (07.06.95) US

(71) Applicant (*for all designated States except US*): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventor; and
(75) Inventor/Applicant (*for US only*): YOUNG, Ian, A. [US/US]; 3181 N.W. 114th Terrace, Portland, OR 97229 (US).

(74) Agents: BEREZNAK, Bradley, J. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).

(81) Designated States: AL, AM, AT (Utility model), AU, AZ, BB, BG, BR, BY, CA, CH, CN, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TR, TT, UA, UG, US, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
*With international search report.*

(54) Title: CLOCK DISTRIBUTION NETWORK UTILIZING LOCAL DESKEWING CLOCK GENERATOR CIRCUITRY

(57) Abstract

A clock signal distribution network for a high-speed microprocessor includes a clock synthesizer (30) coupled to receive an externally generated clock signal. The clock synthesizer (30) deskews the external clock to generate an internal clock signal, which is then distributed about the semiconductor die by a conductivity tree. A set of local deskewing clock generators (40 a-d) are coupled to branch interconnects (31, 33 a-b, 34 a-d) of the tree and function as a zero-delay buffers for driving proximally located circuitry.

