MANUFACTURING PROCESS OF A STRUCTURE OF SEMICONDUCTOR ON INSULATOR TYPE, WITH REDUCED ELECTRICAL LOSSES AND CORRESPONDING STRUCTURE

The present invention relates to a manufacturing process of a structure of semiconductor type on insulator, with reduced electrical losses. It also relates to such a structure.

Technical field of the invention

The invention thus focuses on the general context of manufacturing a structure of semiconductor on insulator type (SOI) by the SmartCut process (registered trademark). This process is described in detail for example in the patent US 5 374 564.

Prior Art

A structure of this type generally comprises a support layer, generally made of silicon monocrystalline having high resistivity, an insulating oxide layer, and a thin layer of semiconductor material.

This thin layer is designed to take up components, typically electronic components.

In particular in applications in which use is made of radio-frequencies, for example in the field of radiophony, part of the waves emitted can be absorbed by the support substrate, despite the presence of the insulating layer, resulting in electrical losses.

To combat this difficulty, it has been proposed to boost resistivity of the support substrate to over 500 Ω.cm, or even over a few thousand Ohms.cm, though this does not prove to be sufficient.

It was then proposed to deposit on the upper face of the support substrate (that is, the one

receiving the insulating layer and the thin layer), a layer of material whereof the density of charge-carrier traps is high.

A polycrystalline silicon layer is adapted in particular to ensure this function. Its structure is formed by a multitude of crystalline grains having defective boundaries (grain joint) forming traps, which makes the ensemble particularly low-conductive. This reduces leakage currents and losses in resistivity at the level of the support substrate.

The technique carried out consists of depositing a polycrystalline silicon layer on the support substrate, then applying the usual steps of the SmartCut process.

This type of method is described in particular in document US 2007/032 040.

But, in conducting tests on resulting structures which would exhibit high resistivity according to the teachings of said document, the present applicant noticed that the technique in question did not reduce electrical losses satisfactorily.

The present invention aims to resolve this problem by providing a manufacturing process of a structure of semiconductor on insulator type, with reduced electrical losses, in which the polycrystalline silicon layer which is placed on the support substrate has the expected resistive character.

Explanation of the invention

This is a manufacturing process of a structure of semiconductor on insulator type, with reduced electrical losses, which successively comprises a support substrate made of silicon, a oxide layer and a thin layer of semiconductor material, a polycrystalline silicon layer being interleaved between the support

substrate and the oxide layer, this process comprising the following steps:

a) oxidation of a donor substrate made of semiconductor material to form an oxide layer at the surface;

b) implantation of ions in the donor substrate to form an embrittlement zone therein;

c) adhesion of the donor substrate to the support substrate, the oxide layer being located at the adhesion interface, said support substrate having undergone thermal treatment capable of giving it high resistivity, that is, a resistivity greater than 500 Ω.cm, its upper face which receives the donor substrate being coated by said polycrystalline silicon layer;

d) fracture of the donor substrate according to the embrittlement zone to transfer to the support substrate a thin layer of semiconductor material;

e) conducting of at least one stabilisation process of said resulting structure.

This process is remarkable in that said treatment capable of conferring high resistivity to said support substrate is carried out prior to formation of the polycrystalline silicon layer, and in that step e) comprises at least one long thermal step, carried out at a temperature not exceeding 950°C, for at least 10 minutes.

The polycrystalline silicon is thus deposited after treatment capable of giving the support substrate high resistivity, such that high temperatures utilised during this treatment do not affect the polycrystalline character of the polycrystalline silicon layer.

Similarly, the thermal budget used during thermal treatment of the final structure is not sufficient to modify this polycrystalline character.

According to other advantageous and non-limiting characteristics:

- the resistivity of said support substrate is greater than 1,000 Ω.cm, preferably greater than 2,000 Ω.cm, still more preferably greater than 3,000 Ω.cm;

- the long thermal step is carried out for several hours;

- it comprises brief treatment conducted for less than 10 minutes, at a temperature greater than 1,000°C, advantageously for one to two minutes, at a temperature of the order of 1,200°C;

- said thermal treatment capable of conferring high resistivity to the support substrate comprises at least one step brought to a temperature of between 500 and 1,200°C, for 30 minutes to 20 hours;

- said thermal treatment capable of conferring high resistivity to the support substrate is an annealing treatment in three steps, the second step being brought to a temperature less than that of the other two steps;

- said three steps are carried out respectively at a temperature of between 1,000 and 1,200°C for 1 to 10 hours, 600 to 900°C for 1 to 10 hours, and 900 to 1,200°C for 1 to 48 hours;

- in step e), said stabilisation comprises at least one thermal stabilisation treatment and one thermal thinning treatment of the thin layer;

- in step c), prior to depositing of the polycrystalline silicon layer, a semiconductive decoupling layer of crystalline network, that is, having a mesh parameter different to that of monocrystalline silicon is deposited onto the receiver substrate;

- said decoupling layer contains polycrystalline silicon;

- said decoupling layer also contains silicon-based and another atomic species-based semiconductor material;

- said silicon-based conductive material is SiC or SiGe;

- depositing of said decoupling layer and of the polycrystalline silicon layer is carried out continuously, that is, in the first instance, by simultaneous feed from two gas sources, respectively polycrystalline silicon and the other atomic species, then by feed only from the polycrystalline silicon source;

- a new decoupling layer is also deposited onto the polycrystalline silicon layer;

- at least one stack constituted by a polycrystalline silicon layer and a decoupling layer are then deposited onto said new decoupling layer;

The invention also relates to a structure of semiconductor on insulator type, with reduced electrical losses, which successively comprises a support substrate made of silicon, an oxide layer and a thin layer of semiconductor material, a polycrystalline silicon layer being interleaved between the support substrate and the oxide layer and is remarkable in that the polycrystalline silicon layer has a resistivity greater than 5,000 Ohms.cm.

Preferably, it has an average resistivity greater than 10,000 Ohms.cm, or even greater than 50,000 Ohms.cm.

Brief description of the figures

Other characteristics and advantages of the present invention will emerge from the following description of certain preferred embodiments. This

description will be given in reference to the attached diagrams, in which:

- Figures 1A to 1G represent the different steps of the process according to the invention;
- Figure 2 is a detailed view of part of the structure into which a decoupling layer is interleaved;
- Figure 3 is a variant of Figure 2 in which an additional decoupling layer is formed on the polycrystalline silicon;
- Figure 4 is a sectional view of a structure according to the invention whereof the resistivity is proposed to be tested;
- Figures 5A and 5B are graphics respectively illustrating according to the prior art and according to the invention resistivity measured via a structure such as that of Figure 4, utilising the "SRP" method.

Description of particular embodiments of the invention

As pointed out earlier, the process according to the invention is of the SmartCut type.

Figure 1A accordingly illustrates a donor substrate 1 in silicon (Si), preferably monocrystalline, covered by a layer 10 of silicon dioxide (SIO_2). This corresponds to Figure 1B.

This oxide layer can result from thermal oxidation of the donor substrate 1 or has been formed by conventionally depositing by chemical depositing techniques in vapour phase well known to the person skilled in the art under the abbreviations CVD and LPCVD (for "Chemical Vapor Deposition" and "Low Pressure Chemical Vapor Deposition").

With reference to Figure 1C, said donor substrate is subjected to implantation of atomic or ionic species via the oxide layer 2.

"Implantation of atomic or ionic species" is understood as any bombardment of these species capable of introducing them to the donor substrate with maximal concentration to a predetermined depth of the substrate relative to the bombarded surface, with a view to creating an embrittlement zone 13. This type of implantation is done according to the process known by the name SmartCut.

The embrittlement zone 13 delimits a thin layer 11 from the rest 12 of the donor substrate 1.

The implantation of atomic or ionic species can be simple implantation, that is, implantation of a single atomic species such as for example implantation of hydrogen, helium or noble gas.

Implantation can also be co-implantation of atomic or ionic species.

A receiver substrate 2 is illustrated in Figure 1D, and is a solid substrate made of silicon.

A characteristic of this support substrate is having undergone thermal treatment capable of giving it an other resistivity, that is, a resistivity greater than 500 Ω.cm, or even greater than 1,000, preferably still greater than 2,000, or even still more preferably greater than 3,000 Ω.cm.

This treatment can have been carried out since fabrication of the substrate or later on, within the scope of the present process.

This thermal treatment capable of giving the support substrate 2 high resistivity is a thermal treatment for example, comprising at least one step brought to a temperature of between 500 and 1,200°C for 30 minutes to 20 hours.

In another embodiment, this treatment comprises annealing treatment in three steps, the second step being brought to a temperature less than that of the other two steps.

Advantageously, these three steps are carried out respectively at a temperature of between 1,000 and 1,200°C for 1 to 10 hours, 600 to 900°C for 1 to 10 hours and 900 to 1,200°C for 1 to 48 hours.

The function of the first step of this advantageous and optional treatment, also known as "High-low-High treatment", is to remove oxygen from a superficial zone of the substrate, by a phenomenon known as "exodiffusion" to produce denuded zone, that is, a zone without oxygen precipitates. This is therefore a zone having fewer defects than at the outset, an advantage for subsequent depositing of polysilicon.

The aim of the second step of this process is to enable nucleation, that is, the creation of "embryos" of interstitial oxygen precipitates.

Finally, the function of the third step of this process is to enable growth of precipitates created in the preceding step, that is, constitute oxide clusters. This translates via an increase in resistivity of the material.

In any case, this augmentation treatment of the resistivity of the substrate 2 is carried out prior to depositing, on the latter, of a polycrystalline silicon layer 20.

Proceeding with this effectively retains the polycrystalline structure of the layer 20.

After the donor substrate 1 is reversed, it is then put in contact with the layer 20 of the support substrate 8, such that the oxide layer 10 regains contact with the polysilicon layer 20.

Adhesion between the two substrates is completed in a preferred but non-obligatory manner, by molecular adhesion.

Disbonding annealing is carried out, followed by detachment from the rest 12 of the donor substrate 1, at the level of the embrittlement zone 13, so as to

transfer the layer 11 to the support substrate 2, more precisely on the polysilicon layer 20.

This produces a substrate 3 of semiconductor on insulator type which is in semi-finished state.

Stabilisation of the resulting structure 3 is then carried out.

In keeping with the invention, this stabilisation comprises a long thermal step, carried out at a temperature not exceeding 950°C for at least 10 minutes, and optionally a brief treatment carried out for less than 10 minutes at a temperature greater than 1,000°C.

The long thermal step is preferably carried out for several hours, whereas the brief treatment is carried out for 1 to 2 minutes at a temperature of the order of 1,200°C.

More precisely, these finishing steps comprise at least one of the following treatments:

a) thermal stabilisation treatment before polishing, consuming the zone of the donor substrate damaged by separation at the level of the interface 13;

b) mechanical and chemical polishing treatment (CMP) for consuming the material of the layer 11 to arrive at the preferred thickness;

c) final thermal thinning treatment to attain the final preferred thickness.

In respecting the temperature and duration conditions indicated earlier, thermal budgets carried out are inadequate for recrystallised polysilicon which loses its beneficial effects.

But, limiting the duration and/or temperature of the treatments during stabilisation of the structure causes embrittlement of the interface created such that it is highly useful to carry out intermediate treatments for reinforcing cohesion of the structure. A particular treatment is carried out prior to adhesion using plasma.

In accordance with a preferred embodiment of the process according to the invention, the polycrystalline silicon layer is formed on a layer 21 known as "network crystalline decoupling", that is, a layer having a concentration gradient with a mesh parameter different to that of silicon formed by the support substrate.

This difference in mesh parameter is for example greater than 5%.

This decoupling layer advantageously contains polycrystalline silicon, but in no case pure monocrystalline silicon.

According to a preferred embodiment, it also contains a silicon-based and another atomic species-based semiconductor material.

This can be SiC or SiGe for example.

The advantage of this gradient layer between the support substrate 2 and the polysilicon layer is that it prevents the polysilicon from recrystallising from the layer 11.

This gradient layer opposes recrystallisation of polysilicon. Via its cavities and grain joints, the polysilicon layer:

- traps the contaminants generating a drop in resistivity (B, P, Ca, Na, etc.);
- forms a barrier to electrical charges contained under the oxide 10;
- prevents diffusion of interstitial oxygen contained in the oxide 10 (diffusion causing poor trapping, such as a "gettering" effect).

The decoupling layer 21 as well as the polysilicon layer 20 are preferably manufactured in the same depositing step, continuously, meaning that the layer 21 is first formed by injecting a first gas to constitute polysilicon and a second gas to constitute the other atomic species; then, once the preferred

thickness is attained the arrival of the second gas is cut off by continued injecting of the gas to form the polysilicon layer.

As shown in Figure 3, a new decoupling polysilicon layer can also be constituted, which prevents the latter from recrystallising from the thin layer of semiconductor material 11.

Optionally, a stack comprising decoupling layer 21/polysilicon layer 20/decoupling layer 21/polysilicon layer 20, etc. can be formed.

Advantageously, the total thickness of the polysilicon layer and of the decoupling layer or decoupling layers is between 3,000 and 10,000 Å, with a ratio 10 between the thickness of the polysilicon layer and the decoupling layer.

Figure 4 proposes testing the resistivity of a structure obtained according to the invention.

This characterisation is done by means of the well-known method called "4PP" (for "four points probe"), specifically by using 4 electrodes passing through the entire structure.

A second method known as "SRP", also well known, traces the evolution of resistivity as a function of the depth, by means of a mitre, as shown by said abovementioned figure.

Irrespective of the method used, it is evident that the structure treated according to the process according to the invention retains high resistivity, compared to the same structure which would not have undergone the process according to the invention.

Using the method known as 4PP and by conducting comparative tests, average resistivity rises from 4 to 5,000 Ω.cm to over 70,000 Ω.cm.

Furthermore and as shown in Figures 5A and 5B, the method known as "SRP" tested on a structure according to the prior art cited at the outset of the

description (Figure 5A), comparatively to the invention (Figure 5B), shows that according to the invention the polysilicon layer has very high resistivity, contrary to the structure according to the prior art.

This is due to the fact that the polysilicon has retained its polycrystalline structure.

Finally, tests were conducted by "injecting" an electrical signal in a component.

The power of harmonics as a function of the principal signal is then measured.

When components used in the field of radio-frequencies are operating, parasite signals can be generated by the electrical signals which pass through them at different frequencies. These are known as harmonic waves.

In the case of a glass substrate, almost no harmonic is generated, and the more the substrate on which the component electronic is made is high-performing, the less is the power of the harmonics.

In the case of a support substrate 2 made of high-resistivity silicon, without the presence of a polycrystalline silicon layer under the Box, the harmonics are high.

With the presence of such a layer, though without modifying thermal treatments, electrical performance is improved, but thermal budget causes partial recrystallisation or even total recrystallisation of the poly-Si and eliminates significant electrical traps.

Finally, the presence of polycrystalline silicon under the Box considerably improves electrical performance, since the manufacturing process is applied according to the invention and/or a decoupling layer (21) is introduced which prevents recrystallisation of the silicon.

It is evident, finally, that depositing a gradient layer between the support substrate and the polycrystalline silicon can also be carried out within the scope of manufacturing a structure of SOI type, other than by the SmartCut technique.

Claims

1. A manufacturing process for a structure of semiconductor on insulator type (3), with reduced electrical losses, which successively comprises a support substrate made of silicon (2), an oxide layer (10) and a thin layer of semiconductor material (11), a polycrystalline silicon layer (20) being interleaved between the support substrate (2) and the oxide layer (10), this process comprising the following steps:

a) oxidation of a donor substrate (1) made of semiconductor material to form an oxide layer (10) at the surface;

b) implantation of ions in the donor substrate to form an embrittlement zone (13) therein;

c) adhesion of the donor substrate (1) on the support substrate (2), the oxide layer (10) being located at the adhesion interface, said substrate (2) support having undergone thermal treatment capable of conferring thereto high resistivity, that is, a resistivity greater than 500 Ω.cm, its upper face which receives the donor substrate (1) being coated by said polycrystalline silicon layer (20);

d) fracturing of the donor substrate (1) according to the embrittlement zone (13) to transfer to the support substrate (2) a thin layer (11) of semiconductor material;

e) conducting of at least one thermal stabilisation event of said resulting structure (3),

characterised in that said treatment capable of conferring high resistivity to said support substrate (2) is carried out prior to formation of the polycrystalline silicon layer (20), and in that step e) comprises at least one long thermal step, carried out at

a temperature not exceeding 950°C, for at least 10 minutes.

2. The process as claimed in Claim 1, characterised in that the resistivity of said support substrate (2) is greater than 1,000 Ω.cm, preferably greater than 2,000 Ω.cm, still more preferably greater than 3,000 Ω.cm.

3. The process as claimed in Claim 1 or 2, characterised in that the long thermal step is carried out for several hours.

4. The process as claimed in any one of Claims 1 to 3, characterised in that it comprises brief treatment carried out over less than 10 minutes, at a temperature greater than 1,000°C, advantageously for one to two minutes, at a temperature of the order of 1,200°C.

5. The process as claimed in any one of the preceding claims, characterised in that said thermal treatment capable of conferring high resistivity to the support substrate (2) comprises at least one step brought to a temperature of between 500 and 1,200°C for 30 minutes to 20 hours.

6. The process as claimed in any one of the preceding claims, characterised in that said thermal treatment capable of conferring high resistivity to the support substrate (2) is an annealing treatment in three steps, the second step being brought to a temperature less than that of the two other steps.

7. The process as claimed in Claim 6, characterised in that said three steps are conducted

respectively at a temperature of between 1,000 and 1,200°C for 1 to 10 hours, 600 to 900°C for 1 to 10 hours, and 900 to 1,200°C for 1 to 48 hours.

8. The process as claimed in any one of the preceding claims, characterised in that in step e), said thermal stabilisation comprises at least one thermal stabilisation treatment and one thermal thinning treatment of the thin layer (11).

9. The process as claimed in any one of the preceding claims, characterised in that in step c), prior to depositing of the polycrystalline silicon layer (20), a semiconductive layer (21) known as decoupling of network crystalline, that is, having a mesh parameter different to that of silicon monocrystalline, is deposited on the receiver substrate.

10. The process as claimed in Claim 9, characterised in that said decoupling layer (21) contains polycrystalline silicon.

11. The process as claimed in Claim 10, characterised in that said decoupling layer (21) contains also silicon-based and another atomic species-based semiconductor material.

12. The process as claimed in Claim 11, characterised in that said silicon-based material conductor is SiC or SiGe.

13. The process as claimed in Claim 11 or 12, characterised in that depositing of said decoupling layer (21) and of the polycrystalline silicon layer (20) is carried out continuously, that is, in the first instance, by simultaneous feed from two gas sources,

respectively polycrystalline silicon of the other atomic species, then by feed only from the source of polycrystalline silicon.

14. The process as claimed in any one of Claims 9 to 13, characterised in that a new decoupling layer (21) is also deposited on the polycrystalline silicon layer (20).

15. The process as claimed in Claim 14, characterised in that at least one stack constituted by a polycrystalline silicon layer (20) and a decoupling layer (21) is deposited on said new decoupling layer (21).

16. A structure of semiconductor on insulator type (3), with reduced electrical losses, which successively comprises a support substrate made of silicon (2), an oxide layer (10) and a thin layer of semiconductor material (11), a polycrystalline silicon layer (20) being interleaved between the support substrate (2) and the oxide layer (10), characterised in that the polycrystalline silicon layer (20) has a resistivity greater than 5,000 Ohms.cm.

17. The structure as claimed in Claim 16, characterised in that it has an average resistivity greater than 10,000 Ohms.cm, or even greater than 50,000 Ohms.cm.