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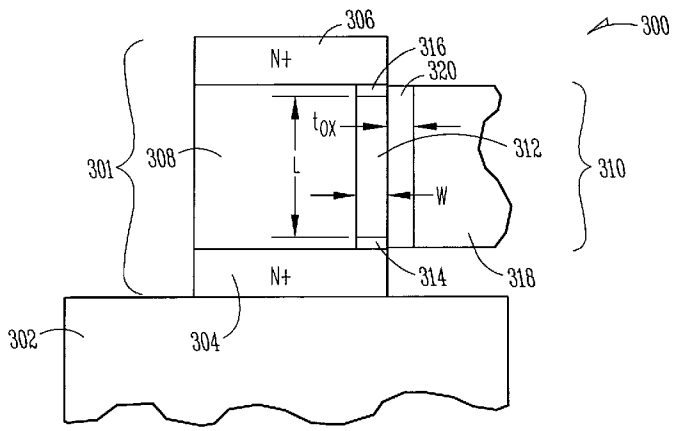
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(54) Title: OPEN BIT LINE DRAM WITH VERTICAL ULTRA-THIN BODY TRANSISTORS



(57) Abstract: Structures and method for an open bit line DRAM device are provided. The open bit line DRAM device includes an array of memory cells. Each memory cell in the array of memory cells includes a pillar (840) extending outwardly from a semiconductor substrate (810). The pillar (840) includes a single crystalline first contact layer (812) and a single crystalline second contact layer (816) separated by an oxide layer (814). In each memory cell a single crytalline vertical transistor is formed along side of the pillar (840). The single crystalline vertical transistor includes an ultra thin single crystalline vertical first source/drain (851) region coupled to the first contact layer (812), an ultra thin single crystalline vertical second source/drain (852) region coupled to the second contact layer (816), an ultra thin single crystalline vertical body region (853) which opposes the oxide layer (814) and couples the first and the second source/drain regions, and a gate (842) opposing the vertical body region and separated therefrom by a gate oxide (825). A plurality of buried bit lines (802) are formed of single crystalline semiconductor material and disposed below the pillars (840) in the array memory cells for interconnecting with the first contact layer (812) of column adjacent pillars in the array of memory cells. Also, a plurality of word lines (842) are included. Each word line (842) is disposed orthogonally to the plurality of buried bit lines (802) in a trench between rows of the pillars for addressing gates (842) of the single crystalline vertical transistors that are adjacent to the trench.

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