IMPROVEMENTS FOR A MICROPROCESSOR WITH PIPELINE SYNCHRONIZATION

ABSTRACT

A system and method for improving microprocessor computer system out of order support via register management with synchronization of multiple pipe-lines. When processing a sequential stream of instructions by a first processing element (200,200',200") it becomes beneficial to have a second processing element (202,202',202") begin processing the same instruction stream then the first (200,200',200") and second (202,202',202") processing elements process the instructions but only one processing element is permitted to change the overall state of said computer system. The second processor (202,202',202") will have more pipeline stages than the first (200,200',200") in order to feed the first processor (202,202',202") and reduce the finite cache penalty and increase performance. In an alternative embodiment both processors may forward and store state changes for future use.

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